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A ΣΔ micro accelerometer with 6 μg/√Hz resolution and 130 dB dynamic range

Uğur Sönmez · Haluk Külah · Tayfun Akın

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Abstract This paper reports the implementation of a low noise, high dynamic-range ΣΔ readout for low cost capacitive Micro-Electro-Mechanical Systems (MEMS) accelerometers. The readout circuit sets the bandwidth of the ΣΔ loop through an extra feedback path, and hence allows the closed loop system to operate with the low noise characteristics similar to a second-order ΣΔ analog-to-digital converter. A thorough noise analysis of the proposed accelerometer shows that the mechanical noise is the most significant source and quantization noise is mostly eliminated. Dynamic range (DR) of the system is improved by minimizing the circuit noise and increasing the full scale range (FSR) by high-voltage pulse feedback. Utilization of these techniques allows the implementation of low cost, low noise, and high DR navigation-grade accelerometers, by eliminating the need for large proof mass, large area MEMS sensors. The proposed system can achieve a minimum of 6.0 μg/√Hz noise floor, 3.2 μg bias instability, and a maximum of 130 dB DR at 1 Hz. A FSR of ±20 g is reported for 6.2 μg/√Hz noise floor. This range can be increased up to ±40 g at the cost of noise performance and DR.

Keywords Microaccelerometers · ΣΔ Modulation · Capacitive readout · Switched-capacitor circuit · Inertial sensors · Navigation grade accelerometer

U. Sönmez · H. Külah (✉) · T. Akın
METU-MEMS Center, Ankara, Turkey
e-mail: kulah@metu.edu.tr

U. Sönmez · H. Külah · T. Akın
Department of Electrical and Electronics Engineering, METU, Ankara, Turkey

Present Address:
U. Sönmez
Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands

1 Introduction

Due to the recent advancements in their noise performance, Micro-Electro-Mechanical Systems (MEMS) capacitive accelerometers have evolved to be critical components of inertial navigation systems. However, dynamic range (DR) of the low noise accelerometers is limited, and hence they can only be used in applications requiring low DR. In the recent years, researches have been focused on high order closed loop ΣΔ accelerometers, which are desirable for their high DR, inherent linearity, and spontaneous A/D conversion. These accelerometers are generally compact, provide a direct digital output; but the additional quantization noise can impact the resolution. Increasing the order of these electro-mechanical ΣΔ modulators can improve the quantization noise; however these high order modulators are plagued with stability problems [1].

Even though there have been reports of low noise, high resolution, and large DR capacitive ΣΔ accelerometers in the literature [2, 3]; such accelerometers generally use large proof masses to minimize noise, and therefore their full scale range (FSR) is limited. Furthermore, large proof mass requirement may introduce process complexity [3] while increasing the overall cost. In addition, for high order ΣΔ accelerometers, sensitivity to process variations and mismatches may become critical due to stability concerns. Leaving a safe margin for stability in the design will tend to decrease noise transfer function (NTF) gain, and can degrade the quantization noise [4].

Recently, the necessity for high performance configurable electro-mechanical modulators have led to the development of unconstrained ΣΔ (UΣΔ) structures [5], which can be designed systematically to optimize quantization noise and loop stability. Compared to standard ΣΔ modulators, the unconstrained electro-mechanical (EM)

ΣΔ architecture uses the sensor as the first two integrators and adds an extra feed-forward path to compensate the missing velocity feedback. Thus, when compared to classical EM ΣΔ modulators, the stability requirements of the UΣΔ are more relaxed despite removing the lead compensator. Hence, the modulator's NTF can be designed like an electronic modulator, and performance can be improved significantly. However, since the NTF depends on the mechanical sensor parameters, the system can only be optimized for a specific sensor.

In this work, a new readout electronics is proposed to implement and augment of the unconstrained architecture for a micro accelerometer. The proposed readout can be adjusted digitally, and optimized for use with an arbitrary accelerometer. This way, noise versus stability trade-off of a ΣΔ accelerometer system can be optimized, improving the accelerometer performance significantly. In addition, such a system can also be optimized for light proof mass MEMS sensors packaged under atmospheric pressure, and hence the navigation grade accelerometer cost can be reduced as well.

This paper starts with the analysis of the ΣΔ modulator architecture to be used in the readout ASIC. In Sect. 3, the circuit architecture and individual components are discussed. Section 4 analyzes mechanical, electrical, and quantization noise sources and discusses how the acceleration-equivalent noise can be minimized. Section 5 presents the experimental results obtained from the readout itself and a complete MEMS accelerometer system.

2 ΣΔ Modulator

Electro-mechanical closed loop operation is achieved by a ΣΔ modulator system composed of a capacitive MEMS sensor and the electronic readout circuit. Figure 1 shows the structure of the MEMS sensor with varying finger-electrode gaps, that translate the acceleration into a differential capacitance change of $C_{RIGHT} - C_{LEFT}$.

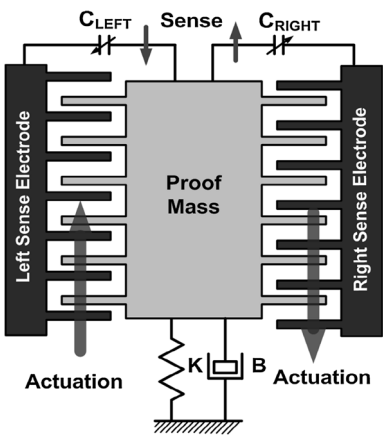

Fig. 1 Structural diagram of the differential capacitive MEMS sensor

Figure 2(a) shows the functional block diagram of the closed loop accelerometer system. The MEMS accelerometer is a differential capacitive accelerometer, so a change in proof mass position due to input acceleration translates as a differential change in capacitance, which is converted by the readout circuit into a voltage difference. This voltage difference is evaluated by the forward noise shaping block $H_F(z)$, and added with the output of the electronic feedback modified by $H_B(z)$. Figure 2(b) shows the combined block diagram of $H_F(z)$ and $H_B(z)$, which have been combined into a single filter implementation. The combined output of $H_F(z)$ and $H_B(z)$ blocks are fed to a 1-bit quantizer, which is modeled as variable gain and additive noise blocks [6]. Finally, the resulting 1-bit output is fed back to acceleration input as EM actuation force.

The closed loop architecture in Fig. 2 is constructed from the modified EM unconstrained ΣΔ architecture [4]. The unconstrained ΣΔ architecture does not need a differentiator (or compensator) stage that is necessary for stabilization of standard ΣΔ accelerometers. Instead, the stability problem is simplified by the addition of an electronic feedback path and can be ultimately guaranteed by limiting the NTF gain. Since the architecture does not need a differentiator, it avoids the quantizer overload and electronic noise shaping problems usually associated with this differentiator [3, 4].

Most importantly, the quantization NTF of this ΣΔ modulator can have arbitrary poles and zeros depending on the gain coefficients A–E inside $H_F(z)$ and $H_B(z)$. This pole-zero assignment should be optimized to minimize the quantization noise for the low frequency bandwidth, since navigation grade accelerometers are susceptible to positional errors due to low frequency noise sources and DC errors [7]. The optimization problem of the 4th order EM NTF simplifies to a 2nd order electronic modulator for a mechanical sensor with light proof mass and moderate resonance frequency [4, 8]. For 2nd order electronic modulators, it is well known that two NTF zeros should be placed at $z = 1$ in order to suppress low frequency noise, DC errors, and idle tones [9, 10]. For this reason, two electronic NTF zeros are fixed in design to $z = 1$. This approach also simplifies the circuit design by preventing the use of gain coefficients with grossly different orders of magnitude, where such a wide range of gain coefficients would be sensitive to even minor circuit mismatches. For this simplified system, the two additional NTF zeros due to the mechanical sensor do not affect the system performance significantly [4]. Hence, the programmable electronic circuit determines the bandwidth, DC gain, quantization noise floor, and other first-order characteristics of the ΣΔ modulator. The mechanical sensor's impact on the performance of the accelerometer system is reduced.

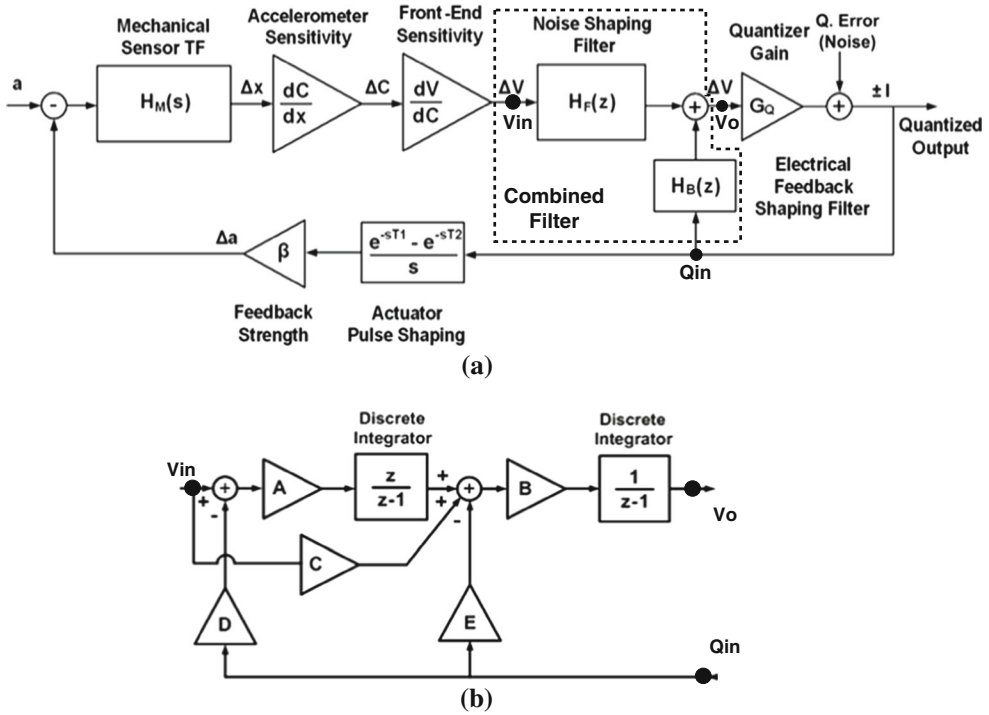

Fig. 2 Block diagram of the EM ΣΔ modulator. **a** Block diagram of the linearized fourth order ΣΔ accelerometer. **b** Block diagram of $H_F(z)$ and $H_B(z)$ combined into a single filter

Optimization problem of the NTF poles concerns the modulator stability. In order to guarantee modulator stability, NTF gain should be suppressed by moving the NTF poles closer to DC. However, locating the NTF poles closer to DC degrades the quantization noise performance [9, 10]; and hence a trade-off between stability and noise performance exists. The goal of the reconfigurable architecture is to optimize this trade-off, and minimize quantization noise by controlling the NTF poles while keeping the modulator stable.

For a more detailed look into noise performance, it is necessary to derive and analyze the NTF of the modulator in Fig. 2. From Fig. 2(b) transfer functions $H_F(z)$ from Vin to Vo and $H_B(z)$ from Qin to Vo are derived as,

$$H_F(z) = B\frac{(C+A)z-C}{(z-1)^2}; H_B(z) = B\frac{(DA+E)z-E}{(z-1)^2} \quad (1)$$

Variables A–E are gain coefficients that can be adjusted to shape $H_F(z)$ and $H_B(z)$ as desired. Note that both of the transfer functions have double poles at $z = 1$, and variable zeros. For the complete system, the quantization NTF is,

$$NTF(z) = \frac{1}{1+G_Q H(z)} \quad (2)$$

where G_Q is the quantizer gain and H(z) is the combined loop transfer function with,

$$H(z) = H_C(z)H_F(z) + H_B(z) \quad (3)$$

Here, $H_C(z)$ is the discrete-time combination of the pulse actuator, feedback strength, $H_M(s)$, capacitance sensitivity, and readout sensitivity blocks. By sampling this combination with the readout's discrete sampling period T, $H_C(z)$ can be derived as: [4]

$$H_C(z) = \beta\frac{\partial V}{\partial x}\frac{1}{K}\left[e^{-j\theta}\frac{e^{-s_M\tau_1}-e^{-s_M\tau_2}}{2j\sin\theta}\frac{z_M}{z-z_M} - e^{j\theta}\frac{e^{-s_M^*\tau 1}-e^{-s_M^*\tau 2}}{-2j\sin\theta}\frac{z_M^*}{z-z_M^*}\right] \quad (4)$$

In Eq. 4, τ_1 is the time when force feedback begins (for 50 % force feedback, set as T/2), τ_2 is T, K is the spring constant of the MEMS sensor, and θ is the damping angle defined as $\cos^{-1}(B^2/(K*m))$, where B is the damping coefficient and m is the accelerometer proof mass. The mechanical poles denoted by s_M and s_M^* are known as,

$$s_M = -\omega_0 e^{j\theta}; s_M^* = -\omega_0 e^{-j\theta} \quad (5)$$

where ω_0 is the resonance frequency of the MEMS sensor in rad/s units. Finally, z_M and its conjugate are derived from s_M and s_M^* by using the z-domain transformation $z_M = e^{-S_M T}$.

By changing the parameters A–E and varying ∂V/∂C, it is possible to alter the NTF and adjust the stability and

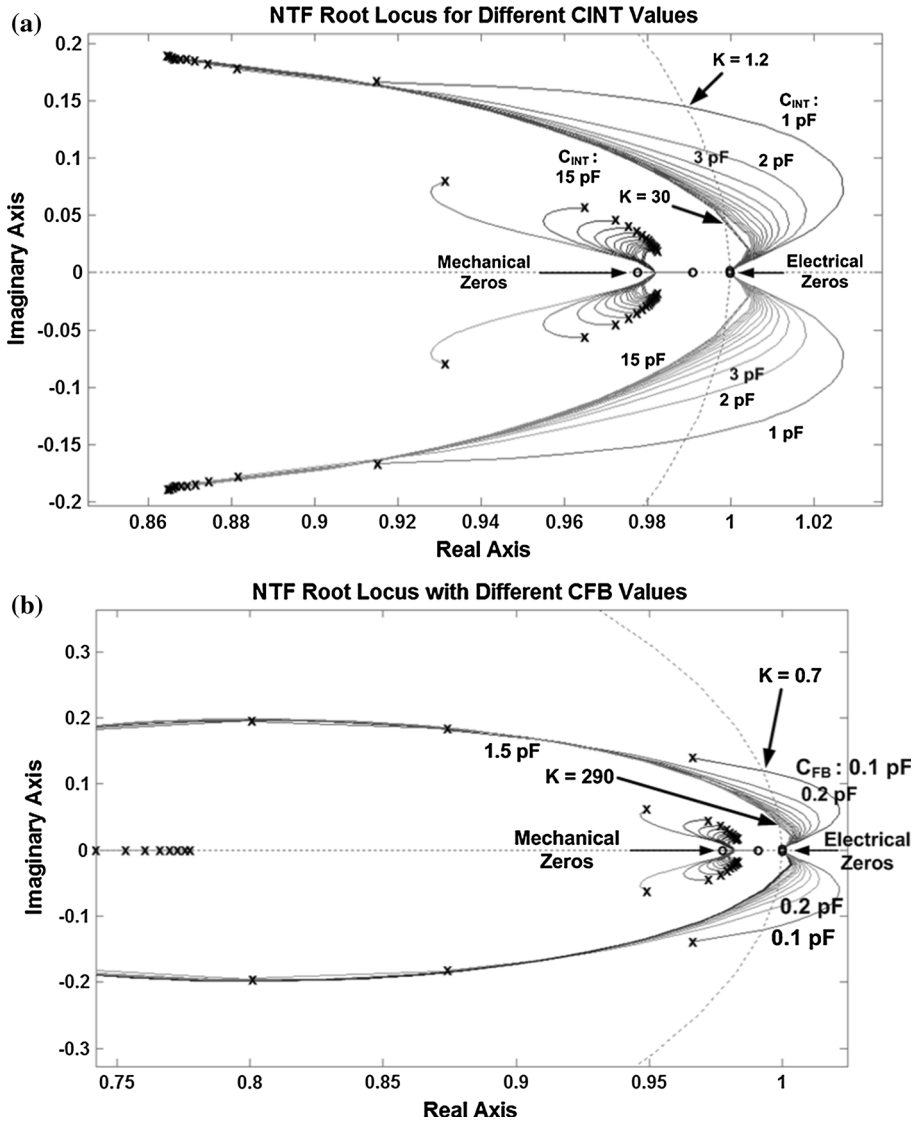

Fig. 3 **a** Z-domain root locus plots of the modulator NTF for different integration capacitance (C_{INT}) values, ranging from 1 to 15 pF. **b** Z-domain root locus plots of the modulator NTF for different feedback capacitance (C_{FB}) values, ranging from 0.1 to 1.5 pF

noise shaping characteristic of the modulator. By co-designing the sensor and readout, most of these parameters (A, B, C, and ratio of D to E) can be fixed and verified by simulation. The two important parameters of the mechanical element that can undergo significant mismatch during fabrication are the mechanical sensitivity (dC/dx) and mechanical resonance frequency. Any deviation in mechanical sensitivity can be corrected by readout gain ($\partial V/\partial C$), and any stability concerns due to variations in resonance frequency can be corrected by a tunable electronic feedback strength (D + E), which can be increased to guarantee stability. This way, a stable modulator which is close to the intended design can be obtained after implementation, with only two variables to be used in experimental calibration instead of six variables.

Figure 3(a, b) show root-locus plots that show how the designed modulator's stability changes with respect to two variables C_{INT} and C_{FB}, which directly correspond to the terms $\partial V/\partial C$ and D + E (see Sect. 3). While all configurations are only conditionally stable for limited feedback or NTF gain (K) values, the modulators with larger C_{INT} and C_{FB} values are stable for larger ranges of K, and hence can be assumed as more stable. This information can be inferred from the figures, where the values of K where the root-locus plots cross the z unit-circle are shown. Note that the effect of C_{FB} on improving stability range is an order of magnitude larger than C_{INT}.

3 Circuit design

The ΣΔ readout circuitry has been designed in a classic differential configuration made up from a front-end charge integrator, cascaded filters with voltage integrators, and a quantizer [3, 5]. Owing to the discrete sampling and integration requirements, switched-capacitor circuits were

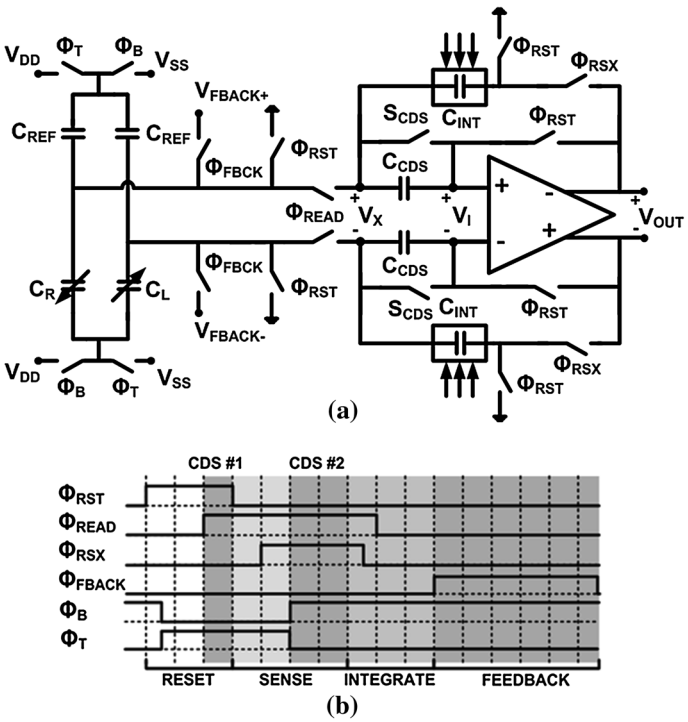

Fig. 4 Schematic of differential readout front-end. **a** The switched-capacitor charge integrator circuitry with CDS. **b** The timing diagram associated with the charge integrator showing the correlated double sampling periods in time domain

preferred in both charge and voltage integrators. Due to the high (160 dB) DC gain of the voltage integrators, a simple dynamic latch, similar to the latch in [11], is used to perform as a 1-bit quantizer. The following subsections discuss each circuit element.

3.1 Front-end charge integrator with correlated double sampling

Figure 4(a) shows the schematic of the sensor front-end. The sense and feedback multiplexed architecture, commonly used in the literature [2, 3, 5], is preferred for the sensor front-end to perform both charge integration and force feedback. In order to improve the FSR, high voltage force-feedback voltages (up to 14 V) are applied to the sensor. However due to performance and power consumption concerns, core readout transistors are designed for a maximum operation voltage of 3.3 V. Therefore, the sensor front-end also isolates the high voltage feedback physically from the rest of the circuitry during operation.

In this front-end architecture capacitance to voltage conversion is done by a charge integrator with correlated double sampling (CDS). A differential architecture is preferred since it increases the total sensitivity by a factor of 2, and suppresses common-mode noise sources. Since the OPAMP in the schematic drives only capacitive loads, it can be simplified into an OTA [5]. At the sensor interface, two identical programmable reference capacitances (C_{REF}) are added to convert the sensor capacitances, C_R and C_L, into a differential bridge.

Timing diagram of the front-end circuit is shown in Fig. 4(b). Note that operation of the sensor front-end is time multiplexed and follows a cycle of reset, sense, and feedback phases. In the reset phase, two integration capacitances (C_{INT}) are discharged, and the remaining charge on C_R and C_L from the previous feedback phase is dumped. Assuming S_{CDS} switches are always on, $V_{DD} = -V_{SS}$, and C_{REF} is set to $(C_R + C_L)/2$, when Φ_B and Φ_T phases switch, a differential charge of $(C_R - C_L)V_{DD}$ is evaluated. The OTA integrates this charge over C_{INT} and the output settles to,

$$V_{OUT} = \frac{V_{DD}(C_R - C_L)}{C_{INT}} + V_{OFFSET} \tag{6}$$

where V_{OFFSET} is the input referred offset of the OTA, which is prone to 1/f noise as well as drift. Correlated double sampling (CDS) can be used to eliminate this noise and drift source, by double sampling the OTA input offset, and subtracting the two measurements [2]. For CDS, S_{CDS} switches have to be opened during reset and charge integration phases.

Speed of this charge integrator is limited by the OTA transconductance (g_M) and capacitive loading at the output. Since the output is sampled by two discrete integrators (see Sect. 3.3), the discrete integrator's input sampling capacitances tend to dominate this capacitive loading. Improving the charge integrator's speed is important to achieve a high

sampling frequency at system level, hence a fast, low noise, and power efficient OTA is needed to boost g_M.

3.2 Recycling folded cascode OTA with NCFF

While a fast and low noise OTA is needed for the charge integrator implementation, there is an additional concern in the design due to the circuit architecture used in the preceding subsection. Due to the operation principle of the charge integrator, the OTA has to be designed for operation for both low and high output capacitances. In Fig. 4, it can be seen that the OTA is driving only C_{CDS} while storing its input referred offset. Sampling by the later stages is off during this time, and the OTA is in a pseudo-buffer state with a low output capacitance. However, during charge integration, the OTA output drives both C_{INT} and any sampling capacitances at its output. Speed of the charge integrator is related with the settling time of the OTA during this high capacitance period, while stability and ringing requirements necessitate a solid phase margin during low capacitance CDS stage.

Moreover, since the switched-capacitor charge integrator aliases OTA wideband noise into the sampling band (see Sect. 4.3), OTA electronic noise is directly related with the sampling frequency, but is inversely related with quantization noise. In order to keep both electronic and quantization noise low, noise floor of the OTA must be kept low as well. In addition, 1/f noise of the OTA must also be kept low, despite using CDS, in order to suppress drift and noise at very low (<1 Hz) frequencies which were mentioned as important factors for navigation applications.

In order to solve these design problems, a multi-path OTA architecture, optimized for oversampled accelerometers and data converters, is presented. Figure 5 shows the schematic of the OTA based on the fast and efficient recycling folded Cascode OTA [12]. A common mode feedback circuit is also used, but is removed from the schematic for simplicity.

In order to analyze this OTA, let us first ignore the transistors M_{13} and M_{16}. In the recycling folded cascode OTA, input transistors are split into two pairs of identical differential transistors: $M_{3–4}$ and $M_{5–6}$ pairs. One transistor in each pair is crossed to one of the identical current mirrors $M_{9–12}$ and $M_{10–11}$. Each pair's gain is amplified by the current mirror gain K and each pair's total transconductance is $(1 + K)g_{M3}$, where g_{M3} is the transconductance of $M_{3–6}$ transistors. Therefore, the transconductance is improved by $(1 + K)/2$ over a standard folded cascode OTA, where the 1/2 factor is derived by the conversion of input quadruplet into an input pair [12].

Noise from the cascode pairs $M_{7–8}$, $M_{14–15}$, and $M_{17–20}$ are negligible since they all see a high degeneration resistance at their source nodes. $M_{1–2}$ contributes only

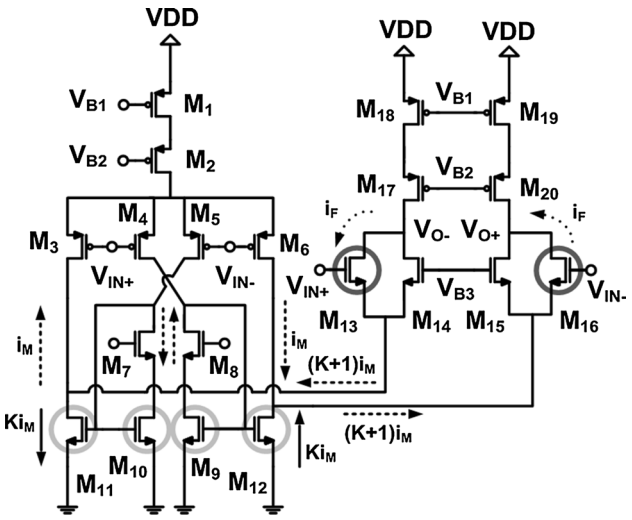

Fig. 5 Schematic of the recycling folded cascode OTA with no capacitor feed-forward compensation, along with typical differential small signal currents

common mode noise, and hence these transistors are ignored as well. The remaining transistors contribute a total input referred noise density of, [5, 12]

$$e_{OTA} = \sqrt{2\left(2e_{M3}^2 + e_{M9}^2\frac{g_{M9}^2}{g_{M3}^2} + e_{M12}^2\frac{g_{M12}^2}{g_{M3}^2}\right)}\frac{V}{\sqrt{Hz}} \tag{7}$$

where e_{M3}, e_{M9}, and e_{M12} are the noise in $V/\sqrt{Hz}$ generated by, and g_{M9}, and g_{M12} are the transconductance of these transistors. Noting g_{M12} is equivalent to $K \times g_{M9}$, and designing g_{M3} to be much larger than g_{M9}, it is possible for the input quadruplet to dominate the noise floor.

Even when the input quadruplet governs the noise floor, 1/f noise can be dominated by $M_{9–12}$ transistors if these transistors are kept small. A large $M_{9–12}$ pair will decrease 1/f noise, however this will move the tertiary pole (due to $M_{9–12}$ current mirror) closer to DC, and may degrade the OTA's phase margin [12]. This situation creates a trade-off between 1/f noise and the phase margin, and complicates the design.

For this implementation, it is more suitable to keep $M_{9–12}$ large to suppress 1/f noise and compensate for the phase margin by adding a high frequency zero. In this configuration, the pole due to M_9–M_{12} is deliberately placed inside the unity gain bandwidth (UGBW), and the tertiary pole at the folding node of M_{11} and M_{14} is pacified by an additional zero, as well as the zero due to the current mirror pair M_9–M_{12} at $(1 + K)$ times the frequency of the current mirror pole [12]. Figure 6 shows the bode diagram of such an amplifier with a UGBW of 371 MHz and phase margin of 57°. The zero is implemented by the no capacitor feed-forward (NCFF) transistors M_{13} and M_{16}, which provide a quick but weak path between the input and output [13].

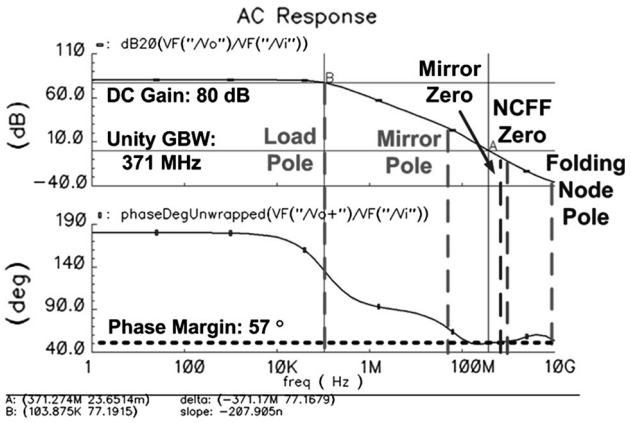

Fig. 6 Bode plot of the recycling folded cascode OTA in open loop, showing the important poles and zeros at frequency domain

Since the additional zeros can degrade the settling time, they are placed beyond UGBW to minimize impact to normal operation [13]. Moreover, the additional pole and zeros effects are diminished when the OTA output capacitance increases and OTA gain bandwidth product (GBW) decreases. The degradation in transient characteristic thus only occurs during the pseudo-buffer state of the OTA, where any settling error only adds a small factor of input offset and 1/f noise to the amplifier output. During charge integration, the zeros are placed well beyond the UGBW and their effect on settling can be neglected.

By selecting the current mirror transistors large, an architecture has been implemented where the OTA transconductance is separated into three paths and frequency bands. As can be seen from Figs. 4 and 5, the OTA has three transconductance paths with currents Ki_{M+}, i_M, and i_F with each path working on a different frequency band at low, mid, and high frequencies. In essence, the OTA behaves like a multi-path amplifier [14], when it is loaded by C_{INT}.

When K = 2.5, the designed OTA has a gain-bandwidth of 1.05 GHz at 1 pF load, UGBW of 371 MHz, 2.3 nV/$\sqrt{\text{Hz}}$ noise floor, 80 dB DC gain, and consumes of 2 mA from 3.3 V. Table 1 presents the transistor dimensions for the designed OTA.

3.3 Noise shaping filters and discrete voltage integrators with offset cancellation

In order to implement the forward and feedback noise shaping filters $H_F(z)$ and $H_B(z)$ at circuit level, a cascade of discrete filters composed of voltage integrators is implemented. Figure 7(a) shows the switched-capacitor implementation of the filter combining $H_F(z)$ and $H_B(z)$. The circuit implements the discrete filter by adding and subtracting charges proportional to input voltages, and stores the results in integration capacitances C_{INT1} and C_{INT2}.

Table 1 Transistor dimensions for the circuit given in Fig. 5

Transistors	W/L (μm/μm)
M1, M2	112/2.8
M3, M4, M5, M6	112/1.05
M7, M8	35/1.4
M9, M10	48/1.05
M11, M12	68/1.05
M13, M16	28/0.7
M14, M15	14/0.7
M17, M18	40/0.7
M19, M20	26/1.4

Electronic feedback from quantizer output is generated by using the complementary voltages V_{FB-} and V_{FB+}. These reference voltages are set to either 3.3 or 0 V, and the differential electronic feedback voltage ($V_{FB} = V_{FB+} - V_{FB}$) is either 3.3 or −3.3 V. This balanced configuration avoids integration of common mode voltages.

Figure 7(b) shows the timing diagram and operation of the circuit. The circuit starts sampling the charge integrator output when Φ_{SMP} and Φ_{SMP2} are both on. In this stage, the charge integrator output from the previous step is sampled on a total load capacitance of $C_{IN1} + C_{IN2}$. At the same time, OTAs are used in pseudo-buffer mode, and input capacitances C_{IN1} and C_{IN2} as well as feedback capacitances C_{FB1} and C_{FB2} store charges of,

$$\begin{aligned} Q_{IN1} &= (V_{IN} - V_{X1}[n-1])C_{IN1} \& Q_{IN2} \\ &= (V_{IN} - V_{X2}[n-1])C_{IN2} \end{aligned} \tag{8}$$

$$\begin{aligned} Q_{FB1} &= (-V_{FB} - V_{X1}[n-1])C_{FB1} \& Q_{FB2} \\ &= (-V_{FB} - V_{X2}[n-1])C_{FB2} \end{aligned} \tag{9}$$

where Q_{IN1}, Q_{IN2}, Q_{FB1}, and Q_{FB2} are the total differential charge on the corresponding capacitors, V_{IN} is $V_{IN+} - V_{IN-}$, and $V_{X1}[n-1]$ and $V_{X2}[n-1]$ are the input referred offsets of A1 and A2. When Φ_{SMP} and Φ_{SMP2} are off and Φ_{INT} is on, A1 integrates the charge on C_{IN1} and C_{FB1} over C_{INT1}. Assuming A1 has a very high gain, the differential charge stored on C_{INT1} is derived as,

$$\begin{aligned} Q_{INT1} = (V_{IN} + V_{X1}[n] - V_{X1}[n-1])C_{IN1} + (-V_{FB} \\ + V_{X1}[n] - V_{X1}[n-1])C_{FB1} \end{aligned} \tag{10}$$

where $V_{X1}[n]$ is the input referred offset of A1 during charge integration. Note that offset and low frequency components of V_{X1} are cancelled.

After A1, A2 performs integration during Φ_{INT2}, just before the feedback phase begins by sampling of the following comparator at Φ_{CMP}. A2 is sampled by the comparator during the feedback phase, and its output is stored for the next cycle.

The filter coefficients A–E in Fig. 2 can be adjusted by programming the ratio of capacitors in this circuit. Table 2

Table 2 Circuit level implementations of the $H_F(z)$ and $H_B(z)$'s coefficients A–E in Fig. 7(a)

Term	Gain	Description
A	C_{INT1}/C_{IN1}	First integrator gain
B	C_{INT2}/C_{FR}	Second integrator gain
C	C_{FR}/C_{IN2}	Feed-forward gain
D	$V_{FB}*C_{IN1}/C_{FB1}$	Feedback gain to first integrator
E	$V_{FB}*C_{FR}/C_{FB2}$	Feedback gain to second integrator

shows the link between gain coefficients A–E and circuit parameters. As mentioned in Sect. 3, all coefficients were set to predetermined values by fixing the capacitors except C_{FB1} and C_{FB2}, but including the ratio between them. The value of C_{FB1} is defined as C_{FB} and allowed to be modified from 0.1 to 1.5 pF. Modifying C_{FB} within this range gives enough room between the noise and stability trade-off. The next section discusses the noise analysis of the complete accelerometer system.

4 Noise analysis

The accelerometer system (MEMS sensor + readout) has three main noise sources: mechanical, quantization, and electronic [5, 15]. Mechanical noise is generated by the sensor, and gives the minimum noise floor achievable with an ideal readout. Quantization noise is largely dependent on the EM ΣΔ modulator architecture and readout sampling frequency. Electronic noise is separated into sense-related readout noise and feedback related voltage reference noise. The following subsections analyze each noise source and their contributions to total acceleration equivalent noise.

4.1 Brownian (mechanical) noise

Brownian or mechanical noise is due to the random movement of the MEMS sensor's proof mass. It is typically given in acceleration-equivalent noise as, [5, 16]

$$a_B = \frac{4Bk_BT}{m^2} \tag{11}$$

where B is the sensor's damping coefficient, k_B is the Boltzmann constant, T is the ambient temperature and m is the proof mass. It can be seen that this noise is only dependent on the mechanical sensor parameters and will tend to be dominant for small and light proof mass sensors. The Brownian noise of the MEMS sensor used with the designed readout is 4.6 $\mu g/\sqrt{Hz}$.

4.2 Quantization noise

Quantization noise can be evaluated through the NTF of the ΣΔ loop, by finding the in-band NTF gain and multiplying by the RMS quantization error of $\Delta/\sqrt{12}$ [9] where Δ is the FSR in acceleration(g). Since NTF is a complex equation and depends nearly on all parameters, including the input signal [9, 10], it is hard to determine the definite quantization noise. The solution of quantization noise through the NTF is rigorous and is best done in a computer assisted mathematical environment.

Other than changing the loop parameters, quantization noise can also be suppressed by increasing the sampling frequency to reduce the in-band noise density [5]. Similarly Δ, the FSR can be reduced to limit the quantization noise, although this will keep the DR constant. Therefore, quantization noise poses a fundamental limit on the DR of an ideal ΣΔ modulator [9].

According to simulations, acceleration equivalent quantization noise is at least 1.2 $\mu g/\sqrt{Hz}$, but it can be larger than 10 $\mu g/\sqrt{Hz}$ for high FSR and passive noise shaping settings (see Sect. 5).

4.3 Readout electronic noise

Critical blocks for in-band readout electronic noise are the charge integrator and the first voltage integrator. Both sources can be referred to the charge integrator's output and then converted into acceleration-equivalent noise. Front-end charge integrator's output referred noise is [15, 17]:

$$e_{OUT} = e_N\sqrt{\frac{(C_S + C_P)}{C_{INT}} * \frac{(2\pi f_U)}{f_S}}\frac{V}{\sqrt{Hz}} \tag{12}$$

where e_N is the input referred noise of the OTA (in $V/\sqrt{Hz}$), C_S is the sense or accelerometer rest capacitance, C_P is the parasitic capacitance at the OTA input and f_U is the OTA UGBW. A noise floor of 103.4 $nV/\sqrt{Hz}$ is found when C_{INT} is 15 pF, e_N is 2.3 $nV/\sqrt{Hz}$, and f_U is 371 MHz.

The charge integrator's noise will be added to the noise contribution of the first integrator. By looking at Fig. 7(a), it can be seen that voltage noise at the OTA inputs will cause charge to fluctuate from the input capacitances ($C_{FB1} + C_{IN1} + C_{P1}$) to C_{INT1}. This charge can be referred back to the input by the integrator gain (C_{IN1}/C_{INT1}). Therefore, the input-referred voltage noise (e_{INI}) of the first integrator takes a very similar form to Eq. 12 and will be,

$$e_{INI} = e_{NI}\sqrt{\frac{(C_{FB1} + C_{IN1} + C_{P1})}{C_{IN1}} * \frac{(2\pi f_{UI})}{f_S}}\frac{V}{\sqrt{Hz}} \tag{13}$$

where e_{NI} is the input referred noise in $V/\sqrt{Hz}$ of A1, C_{P1} is the parasitic capacitance at the OTA input and f_{UI} is the unity gain bandwidth of A1. For $C_{FB1} = C_{IN1} = 1.5$ pF, $e_{NI} =$ 4 $nV/\sqrt{Hz}$ and $f_{UI} = 80$ MHz, a noise floor of 126 $nV/\sqrt{Hz}$ is expected. Combining Eqs. 12 and 13, the total electronic noise is obtained as,

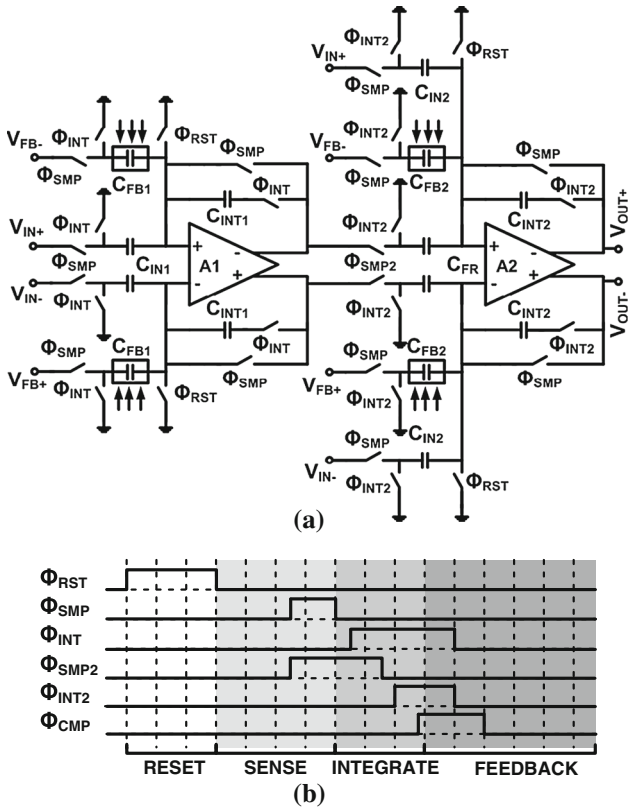

Fig. 7 Implementation of combined noise shaping blocks $H_F(z)$ and $H_B(z)$. **a** Schematic of the cascaded discrete voltage integrators with offset cancellation. **b** The timing diagram associated with the cascaded integrators

$$e_{TOTAL} = \sqrt{e_N^2 \frac{(C_S + C_P)}{C_{INT}} * \frac{(2\pi f_U)}{f_S} + e_{NI}^2 \frac{(C_{FB1} + C_{IN1} + C_{P1})}{C_{IN1}} * \frac{(2\pi f_{UI})}{f_S}} \frac{V}{\sqrt{Hz}} \tag{14}$$

This noise can be referred to acceleration by dividing with the readout front-end sensitivity V_{DD}/C_{INT}, accelerometer capacitive and mechanical sensitivities $\partial C/\partial x$ and $\partial x/\partial g$. These terms can be combined to obtain $\partial V/\partial g$, which can be derived as: [15]

$$\frac{\partial V}{\partial g} = 9.8 \frac{V_{DD}}{C_{INT}} \left(\frac{1}{2\pi f_R}\right)^2 \frac{\partial C}{\partial x} \tag{15}$$

where f_R is the MEMS sensor's resonance frequency, and $\partial C/\partial x$ is the capacitance sensitivity of the sensor. Since the electronic noise sources e_{OUT} and e_{IN1} contribute roughly the same order of noise, the acceleration equivalent noise is expected to increase with increasing C_{INT}. For the highest C_{INT} case of 15 pF and $\partial C/\partial x = 3.5$ μF/m; the acceleration equivalent noise is 2.34 μg/$\sqrt{\text{Hz}}$, weaker than the Brownian noise floor of 4.6 μg/$\sqrt{\text{Hz}}$.

4.4 Force feedback reference voltage noise

Noise on the high-voltage force feedback reference voltage will be directly converted into acceleration during actuation. The gain from this voltage to acceleration is related with the range and sensitivity of the accelerometer. For a varying-gap type capacitive MEMS sensor, the sensitivity of actuation force to small variations on the reference voltage V_{FF} is, [18, 19]

$$\frac{\partial F}{\partial V_{FF}} = V_{FF} \frac{\partial C}{\partial x} \tag{16}$$

Uncertainty of V_{FF} is reflected to acceleration when it is mixed with the output of the quantizer at the sampling frequency. For this reason, noise on V_{FF}, denoted as e_{VFF}, is aliased down to sampling frequency and multiplied by the sensor's sensitivity. Hence, the total acceleration (g) equivalent noise in g/$\sqrt{\text{Hz}}$ due to e_{VFF} (in units of V/$\sqrt{\text{Hz}}$) will be:

$$e_{AEF} = \frac{e_{VFF} V_{FF}}{m * 9.8} \frac{\partial C}{\partial x} \sqrt{\frac{f_{FB}}{2 f_S}} \frac{g}{\sqrt{Hz}} \tag{17}$$

A very important conclusion can be made about the force feedback reference voltage noise: it is dependent on the bandwidth, amplitude, and total wideband noise of the reference voltage. Therefore, it is important to consider both the in-band value of e_{VFF} (which can be several 100 nV/$\sqrt{\text{Hz}}$) and its wideband noise distribution; which are dependent on the individual test setup used. Worst of all, e_{VFF} will also tend to increase with increasing V_{FF}. Hence, the force feedback reference voltage noise is expected to follow a parabolic trend versus V_{FF} and can dominate the noise floor at high voltage configurations.

4.5 Sensor charging reference voltage noise

During charge integration, sensor capacitances are charged by a fixed reference voltage and the capacitance measurement is made by measuring this charge. Therefore, any noise on this reference voltage will also be reflected as noise at the front-end output. For a single-ended front-end, the spectral density of this noise is given as: [5]

$$e_{SCRV} = \sqrt{\frac{2 V_{NREF}^2 C_S}{f_S R_{SW} C_{INT}^2}} \frac{V}{\sqrt{Hz}} \tag{18}$$

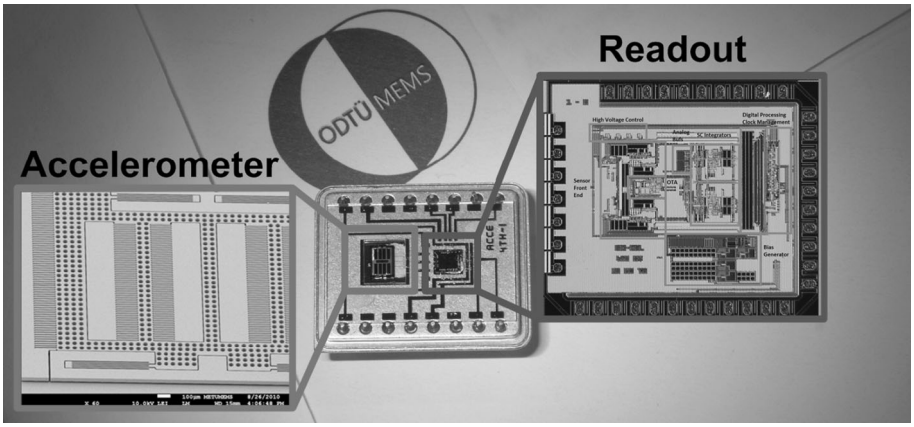

Fig. 8 Photo of the built single-axis accelerometer package with SEM photo of MEMS sensor and die photo of readout

where V_{NREF} is the wide-band noise on the reference voltage in V/$\sqrt{\text{Hz}}$, C_S is the sensor capacitance, f_S is the sampling frequency, R_{SW} is the total series resistance due to switches seen by C_S, and C_{INT} is the integration capacitance.

When the differential architecture in Fig. 4 is considered, the noise expression in Eq. 18 is eliminated for a perfect capacitive bridge structure. Assuming all sense and reference capacitors (C_R, C_L and C_{REF} in Fig. 4) are equal, any noise on the reference voltages VDD, VSS, and ground contribute equally to both branches of the integrator and are thus common-mode noise sources. Therefore, sensor charging reference voltage noise is not dependent on the total sensor (bridge) capacitance, but instead on the mismatch between the capacitors in the bridge. Equation 18 can be thus be modified by replacing C_S with the absolute capacitance mismatch term C_M:

$$e_{SCRV} = \sqrt{\frac{2V_{NREF}^2 C_M}{f_S R_{SW} C_{INT}^2}} \frac{V}{\sqrt{Hz}} \tag{19}$$

In closed loop, the difference between C_R and C_L is equal to zero due to feedback, thus the only contribution to C_M is from the mismatch of two on-chip C_{REF} capacitors, which is typically very small in modern CMOS processes. For 10-bit matched 10 pF C_{REF} capacitors with $C_M = 10$ fF, $R_{SW} = 100\ \Omega$, worst case integration capacitance of $C_{INT} = 1$ pF, and $f_S = 1$ MHz, the SCRV noise is only 3.5 times the wide-band noise on the reference voltage, which is typically suppressed by on-chip decoupling capacitors and is hence very small (10–50 nV/$\sqrt{\text{Hz}}$). The total acceleration equivalent noise due to SCRV noise is calculated to be 0.8 μg/$\sqrt{\text{Hz}}$ for the smallest integration capacitance.

5 Test results

The designed IC was fabricated in a 3.3 V core, 0.35 μm process with a high-voltage option up to 14 V. The IC consumes 4.8 mA from 3.3 V and 0.1 mA from force feedback reference voltage when charging the sensor capacitor during feedback; and the worst case power consumption is 16.7 mW. A sampling frequency of 1 MHz was applied during testing in order to obtain 250 Hz signal bandwidth.

The readout circuit is integrated with a MEMS varying-gap capacitive sensor [8] (Fig. 8), and tested under atmospheric pressure. Compared to most low noise accelerometers reported in the literature, the MEMS sensor employed in the system has a lighter proof mass (264 μg) [1, 2]. The mechanical sensor is a bulk micromachined capacitive accelerometer with structural thickness of 35 μm, finger-electrode gap of 2 μm, and sensitivity of 168 fF/g.

In order to obtain acceleration data in the low frequency signal band, 1 MHz accelerometer output is sampled by a commercial FPGA and decimated into 250 Hz band. Figure 9 shows the complete test setup with the sensor and ASIC package along with the FPGA and a power distribution PCB. Within this setup all the functional blocks, except the accelerometer, the power supplies, and a commercial low noise high voltage regulator to generate the feedback voltage, are implemented on-chip.

The implemented accelerometer is initially tested by comparing its wide-band noise distribution with the simulated and predicted results. Figure 10 shows that PSD of the accelerometer output matches with the simulated results throughout the whole band. A numerical estimation based on the quantization noise and the Brownian noise floor is also given in the Fig. 10 to show the accuracy of the model.

Figure 11 shows the decimated 250 Hz band accelerometer output. Noise power floor of the system is −104.5 dBg/Hz, corresponding to a noise density of 6 μg/$\sqrt{\text{Hz}}$. 1-h Allan Variance plot given in Fig. 12 shows that the long-term instability of the accelerometer is dominated by a trend line with a slope = 1, indicating that 1/f noise is not observed. This trend line is most likely to be determined by long-term

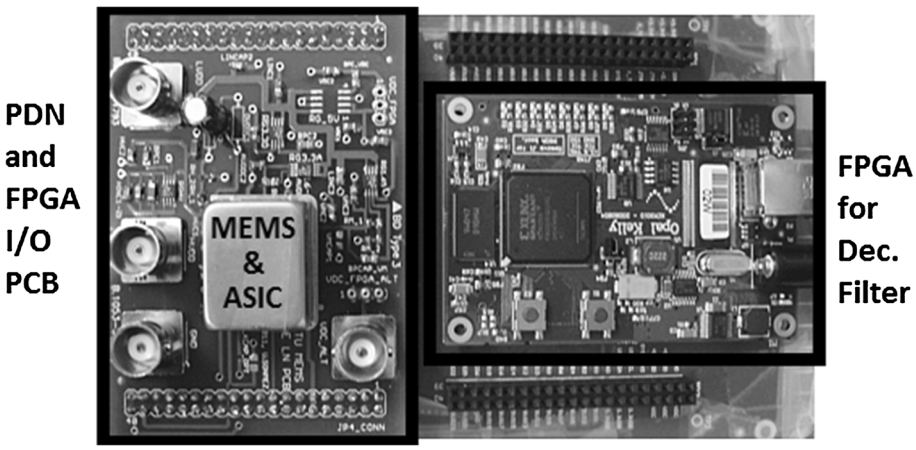

Fig. 9 Photo of the test setup with power distribution network (test) PCB and an FPGA

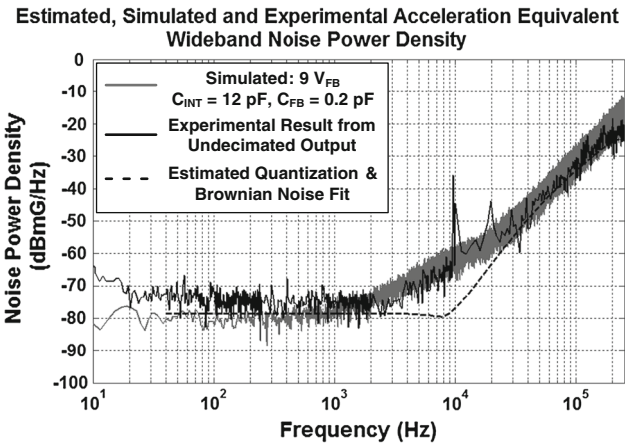

Fig. 10 Wideband power spectral density of the experimental, simulated and estimated acceleration equivalent noise sources. Estimation of wideband noise PSD is based on the mechanical noise floor and quantization NTF

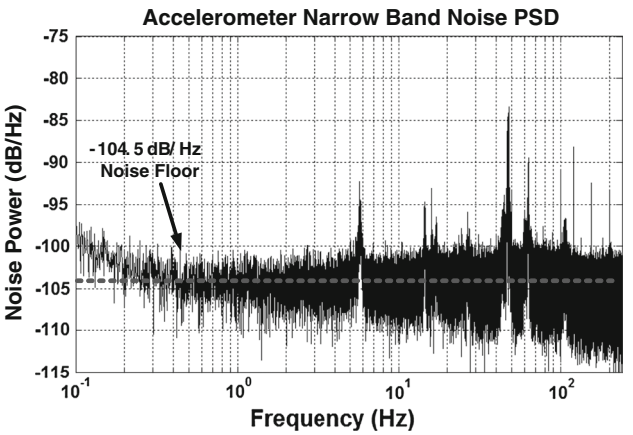

Fig. 11 Narrow (signal) band acceleration equivalent noise PSD from 0.1 to 250 Hz, with a noise floor of −104.5 dBg/Hz or 6.2 μg/$\sqrt{\text{Hz}}$

temperature variations as no temperature compensation is used in this design. Bias drift or instability of the system is 3.2 μg, and velocity random walk of the system, which is equivalent to the double sideband noise density [7], is 4.3 μg/$\sqrt{\text{Hz}}$.

Full scale range, non-linearity and long term stability of the accelerometer is tested in a rotating chamber up to the equipment's acceleration limit of ±20 g. For configurations beyond ±20 g, rest of the FSR is estimated from the performance of the accelerometer within this range. Operation beyond ±20 g could be observed by short-term vibrations or shock effects, but long term stability and nonlinearity beyond ±20 g could only be estimated. With these estimations, the maximum FSR is expected to be ±40 g for a feedback voltage of 12.9 V, while the stability is tested and guaranteed for up to ±20 g.

Figure 13 shows the ±20 g ramp and nonlinearity performance of the accelerometer under two configurations. In the first configuration, C_{INT} is set to 15 pF to minimize the noise floor. This setting has significant nonlinearity since front-end sensitivity is so low that the secondary (electronic) feedback causes the proof mass to oscillate at $f_S/4$ frequency, and hence makes the quantizer susceptible to overload near the acceleration limits of the ΣΔ modulator. When C_{INT} is reduced down to 4 pF, the readout gain increases and this nonlinearity source disappears as expected.

Linearity can also be improved by using a simple linear calibration of the accelerometer's scale factor, where the scale factor of the accelerometer can be further trimmed by a 3-point trim measuring the sensor's output values at 0, 0.5 and 1 g acceleration values on a rotating table setup. With these corrections, a nonlinearity figure of 0.2 % for ±20 g range can be found without affecting the resolution.

Since the designed IC is reconfigurable, it is possible to see how the modulator reacts to changes in C_{FB}, C_{INT}, and the force feedback voltage V_{FF}. Figure 14 shows the change in noise density (for ±20 g FSR) versus varying C_{FB}, i.e. the electronic feedback strength. Despite the simulation results and expectations, it is seen that the modulator is unstable for

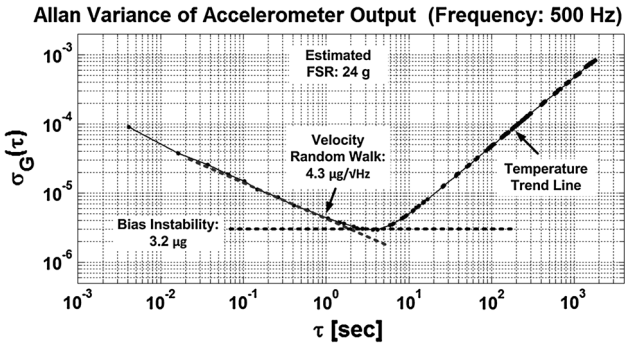

Fig. 12 Allan variance plot of the 1-h data gathered from the accelerometer showing a bias instability (drift) of 3.2 µg and velocity random walk of 4.3 µg/$\sqrt{\text{Hz}}$

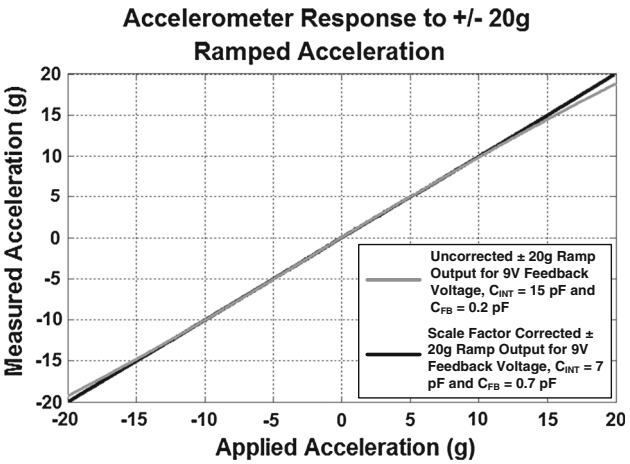

Fig. 13 Accelerometer response to ±20 g ramp input, showing the FSR and nonlinearity

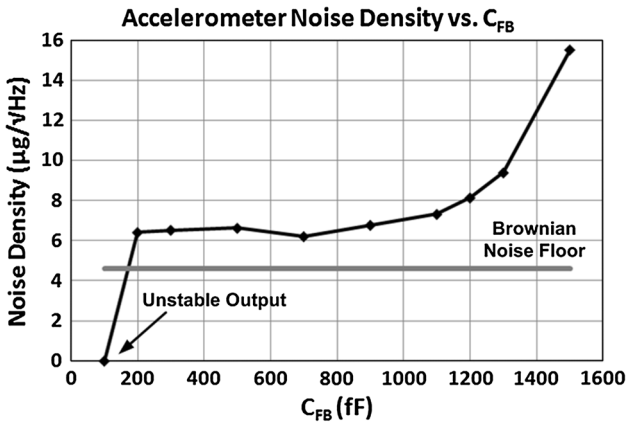

Fig. 14 Plot of noise density variation versus feedback capacitance C_{FB}. Increasing C_{FB} also increases the electronic feedback strength thorough the coefficients D and E

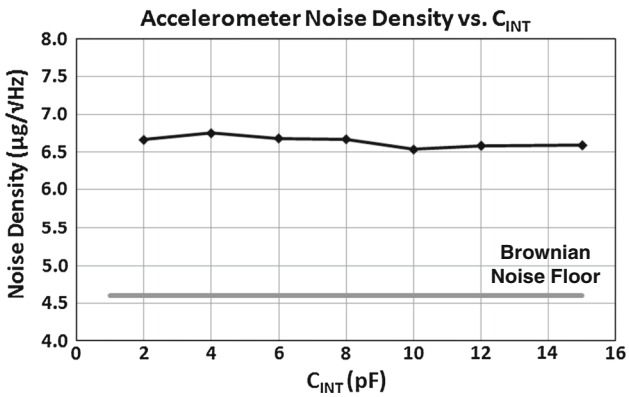

Fig. 15 Plot of noise density variation versus integration capacitance C_{INT}. Increasing C_{INT} is expected to increase electronic noise, but decrease the quantization noise; hence it can be derived that electronic noise is weaker compared to quantization noise

$C_{FB} = 100$ fF. This fact highlights the sensitivity of the modulator's stability on the circuit and MEMS sensor's non-idealities, and shows that a reconfigurable architecture can be preferred to avoid such mishaps.

As expected, when C_{FB} is increased, the modulator achieves stable operation. Further increase in C_{FB} tends to degrade the quantization noise suppression, and hence the noise floor increases. A minimum noise floor of 6.2 µg/$\sqrt{\text{Hz}}$ is observed at a local minimum when $C_{FB} = 700$ fF.

Figure 15 shows the change in noise density when the readout sensitivity is adjusted through C_{INT} when C_{FB} is set to 500 fF. The effect of C_{INT} is more subtle than C_{FB}, and can be only used to fine-tune the quantization and electronic noises. Since the noise floor stays relatively constant even when C_{INT} is maximized, it is seen that electronic noise is very low as expected.

Figure 16 shows the variation of noise floor and DR with respect to force feedback (pulse actuation) voltage. In this figure, both the experimental FSR (with a maximum of ±20 g), and estimated FSR values are provided. By comparing the variance of the estimated DR over V_{FF}, it is possible to determine which noise sources limit the DR. For this analysis, it is useful to keep in mind that increasing the force feedback voltage will increase the estimated FSR parabolically [19, 20]. Since the voltage to acceleration gain stays constant, both electronic and quantization noise sources will follow this increase in FSR, although mechanical noise will stay constant. Thus, it can be inferred that mechanical noise dominates for feedback voltages less than 9 V, since the DR is sharply increasing. From 9 to 11 V, the estimated DR stays around 131 dB and the noise floor is increasing linearly, so quantization and electronic noise sources are stronger. Beyond 11 V, DR sharply decreases due force feedback reference voltage noise. Maximum experimental DR of 130 dB @ 1 Hz band is achieved when $V_{FF} = 9.3$, $C_{FB} = 700$ fF and $C_{INT} = 12$ pF. The estimated DR and FSR at this configuration are 131.6 dB and ±24 g values, respectively.

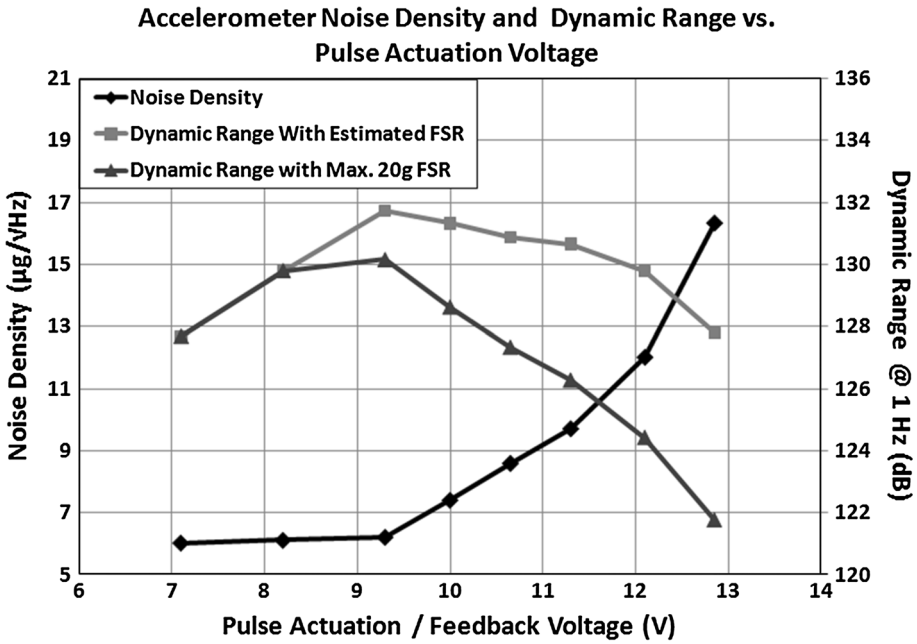

Fig. 16 Plot of noise density and 1 Hz DR variation versus force feedback reference voltage (V_{FF}). Two DR plots represent the DR obtained from FSR estimations, and from the maximum tested and confirmed FSR of ±20 g

Table 3 Performance parameters of the accelerometer interface ASIC

Device characteristic	Value
Process technology	0.35 µm CMOS
Chip area	5.5 mm^2
Power consumption	16.7 mW
Feedback voltage	6–14 V adjustable
Sampling frequency	1 MHz
Signal bandwidth	250 Hz
MEMS sensitivity	165 fF/g

Due to the flexibility of the designed circuit, the accelerometer achieves 6.2 µg/$\sqrt{}$Hz resolution, 3.2 µg bias instability, ±20 g FSR, and 130 dB DR; and a lower resolution of 6.0 µg/$\sqrt{}$Hz resolution is possible at the cost of FSR and DR. As a summary, Table 3 shows the performance parameters of the designed readout IC, and Table 4 compares the performance of the accelerometer with other results from the literature, including a comparison with a 2nd order ΣΔ accelerometer using a similar MEMS sensor. In order to show the power versus DR efficiency of the implemented accelerometer, a figure of merit is defined by regarding the ΣΔ accelerometer system as a typical analog to digital converter:

Table 4 Performance comparison of the accelerometer interface ASIC with the state-of-the-art literature

Readout IC	Feedback voltage (V)	Full scale range (g)	Noise floor (µg/$\sqrt{}$Hz)	Bias drift (µg)	Dynamic range (1 Hz) (dB)	Power (mW)	FoM[a] (nJ)
This work	7.1	±15	6.0	3.3	128	16.7	6.3 J
This work	9.3	±20 (24)	6.2	3.2	130 (131)	16.7	5.0 J
This work	12.9	±20 (40)	16.3	12.1	122 (127)	16.7	12.6 J
2nd order ΣΔ [20]	5	±18.5	74	86	107	16	68.5 J
[1]	±9	±11	1.1	–	139	12	1.3 J
[2]	–	–	4	2–8	108	4.5	17.2 J
[3]	5	–	150	–	–	13	–
[5]	5	±1.1	10	–	101	7.2	61.6 J
[21]	2.5	±2	12.7	–	104	6	36.3 J
[22]	3.3	±10	63.8	–	100	2.6	25.0 J

[a] FoM is defined as Power/(2^{ENOB}*1 Hz), where ENOB is the effective number of bits derived from DR

$$\text{FOM} = \text{Energy consumption per conversion} = \frac{\text{Power}}{2^{\text{ENOB}} * \text{BW}} \text{Joules} \quad (20)$$

For Eq. 20, ENOB is defined as the effective number of bits in terms of acceleration units (g) derived from the DR. The DR values in Table 4 are calculated for a 1 Hz conversion bandwidth (BW).

6 Conclusion

A reconfigurable ΣΔ interface IC for capacitive micro accelerometers is presented in this work. The proposed IC has been tested with a low cost simple MEMS sensor and a significant increase in DR has been reported with a value of 131.6 dB at 1 Hz. Minimum noise floor of the accelerometer system is determined as 6 $\mu g/\sqrt{Hz}$, and is shown to be mostly dominated by the mechanical noise floor of 4.6 $\mu g/\sqrt{Hz}$ at low FSR settings. Force feedback voltage reference noise dominates the noise performance at high FSR configurations, and both electronic and quantization noise sources are sufficiently suppressed. These results are promising for low cost inertial navigation sensor applications, and the designed IC can also be configured for use in both low noise and high FSR applications as well.

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Uğur Sönmez was born in Istanbul, Turkey on 3 April 1986, and graduated from the Uskudar American Academy high school in 2004. He obtained B.Sc. and M.Sc. degrees in electronics from Middle East Technical University, Ankara, Turkey in 2008 and 2011, respectively. His M.Sc. thesis was on readout circuits for capacitive MEMS accelerometers. In August 2011, he joined the Electronic Instrumentation Laboratory, where he is currently working towards a Ph.D. in the area of thermal-diffusivity-based frequency references and temperature sensors. His non-research interests currently include cycling, music and high fidelity music reproduction, history, mythology, and table-top RPGs.

Haluk Külah received the B.Sc. and M.Sc. degrees in electrical engineering with high honors from METU, Ankara, Turkey, in 1996 and 1998, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2003. From 2003 to 2004, he was employed as a Research Fellow at the Department of Electrical Engineering and Computer Science, University of Michigan. In August 2004, he joined the Electrical and Electronics Engineering Department of METU as a faculty member. His research interests include MEMS sensors, mixed-signal interface electronics design for MEMS sensors, BioMEMS, and MEMS-based energy scavenging. Dr. Külah is also working as the Deputy Director of METU-MEMS Center.

Tayfun Akın was born in Van, Turkey, in 1966. He received the B.S. degree in electrical engineering with high honors from Middle East Technical University, Ankara, in 1987 and went to the USA in 1987 for his graduate studies with a graduate fellowship provided by NATO Science Scholarship Program through the Scientific and Technical Research Council of Turkey (TUBITAK). He received the M.S. degree in 1989 and the Ph.D. degree in 1994 in electrical engineering, both from the University of Michigan, Ann Arbor. Since 1995, 1998, and 2004, he has been employed as an Assistant Professor, Associate Professor, and Professor, respectively, in the Department of Electrical and Electronics Engineering at Middle East Technical University, Ankara, Turkey. He is also the director of METU-MEMS Center, which has a 1,300 m^2 cleanroom area for 4″, 6″, and 8″ MEMS process and testing. His research interests include Micro-Electro-Mechanical Systems (MEMS), Microsystems Technologies, infrared detectors and readout circuits, silicon-based integrated sensors and transducers, and analog and digital integrated circuit design. He has served in various MEMS, EUROSENSORS, and TRANSDUCERS conferences as a Technical Program Committee Member. He was the co-chair of The 19th IEEE International Conference of Micro Electro Mechanical Systems (MEMS 2006) held in Istanbul, and he was the co-chair of the Steering Committee of the IEEE MEMS Conference in 2007. He is the winner of the First Prize in Experienced Analog/Digital Mixed-Signal Design Category at the 1994 Student VLSI Circuit Design Contest organized and sponsored by Mentor Graphics, Texas Instruments, Hewlett-Packard, Sun Microsystems, and Electronic Design Magazine. He is the co-author of the symmetric and decoupled gyroscope project which won the first prize award in the operational designs category of the international design contest organized by DATE Conference and CMP in March 2001. He is also the co-author of the gyroscope project which won the third prize award of 3-D MEMS Design Challenge organized by MEMGen Corporation (currently, Microfabrica).