Microwave Characterization of a Wafer-Level Packaging Approach for RF MEMS Devices Using Glass Frit Bonding

Ilker Comart, Kagan Topalli, *Senior Member, IEEE*, Simsek Demir, *Member, IEEE*, and Tayfun Akin, *Member, IEEE*

***Abstract*— This paper presents the microwave characterization of a wafer level packaging approach for RF MEMS devices, using glass frit as the bonding material. Coplanar waveguide transmission lines are packaged by silicon caps to carry out the RF characterization of the package structure. Prior to bonding of the cap on the transmission lines, cap wafers are bulk micromachined to form the cavities for housing the device to be packaged and pad windows to access the RF ports of the devices. Lateral feedthroughs are designed under the glass frit ring transitions in order to decrease the impedance loading effect of the silicon cap and the glass frit ring. The package is implemented using both high and low resistive silicon wafers in order to assess the microwave effects of cap wafer. A circuit model is used to extract the parameters of the feedthrough from the RF measurements. The loss of the feedthrough is measured to be 0.1 dB/transition at 10 GHz for high resistive silicon caps demonstrating the viability of glass frit in the packaging of RF MEMS devices.**

***Index Terms*— CPW, MEMS packaging, cap, glass frit, RF MEMS, microwave characterization, bonding.**

I. Introduction

RF MEMS technology have shown great potential in the recent years for the development of low loss, low power and low cost reconfigurable microwave components and antennas. RF MEMS devices have tunable functionality as they have sub-millimeter sized mechanically movable parts. The movement of these dynamic parts and the reliability of RF MEMS devices may be degraded due to fabrication related residues, dust, humidity and electromagnetic fields. Therefore, packaging is an essential part of RF MEMS device fabrication process. There are two packaging approaches: die-level and wafer-level packaging. Wafer level is an efficient approach to decrease the total cost of the fabrication since all the devices are packaged at the end of the process chain [1], [2].

There are two possible wafer level packaging methods. One of them is the thin film encapsulation and the other is bonding based packaging [3], [4], i.e. chip capping. Thin film encapsulation method utilizes a thin dielectric [5], [6] or metal layer [7], [8] for the sealing of MEMS devices. In chip capping method, a cap is bonded on the MEMS devices using either wafer bonding or flip-chip bonding techniques. Although anodic bonding and silicon-silicon bonding requires none, it is also possible to use a bonding interlayer between the device substrate and cap [9], [10]. The common adhesive interlayers are polymers [11], [12] and gold for eutectic or thermocompression bonding [13]–[15]. Glass frit bonding is a viable selection for a wide range of MEMS devices including MEMS resonators and RF MEMS switches [16]–[19]. Glass frit bonding provides hermetic package, cost and time effective fabrication process [1]. Glass frit also has the ability to cover a few micrometer surface steps. This ability allows simple planar feedthrough structures to be utilized [20].

The bonding method and bonding layer among these alternatives is selected considering particularly the feedthrough design of the RF MEMS device. Glass frit bonding enables the use of CPW transmission lines for planar feedthroughs and the process remains rather simple. Otherwise, vertical feedthroughs are required complicating the fabrication process.

In an RF MEMS device, the other constraint is the microwave performance of the package. The loading effects of the bonding layers and the cap wafer are important aspects of the package design. In order to minimize the effect of the package on the RF MEMS device performance, these effects should be taken into account during design. Moreover, the conductivity of the cap plays an important role in terms of the loss characteristics of the complete structure.

This paper focuses on the microwave characterization and modeling of a wafer-level package using glass frit bonding. The microwave characterization of the different feedthrough designs under the glass frit regions are carried out using a circuit model and RF measurements. In order to verify the significance of cap wafer conductivity in an RF MEMS device packaging process, the package is implemented using both low- and high-resistive silicon wafers. To the authors'

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I. Comart is with the MEMS Research and Application Center, Middle East Technical University, Ankara 06531, Turkey (e-mail: ilker.comart@metu.edu.tr).

K. Topalli was with the MEMS Research and Application Center, Middle East Technical University, Ankara 06531, Turkey. He is now with the Department of Electrical and Electronics Engineering, TED University, Ankara 06420, Turkey (e-mail: kagan.topalli@tedu.edu.tr).

S. Demir and T. Akin are with the Department of Electrical and Electronics Engineering, Middle East Technical University, Ankara 06531, Turkey (e-mail: simsek@metu.edu.tr; tayfuna@metu.edu.tr).

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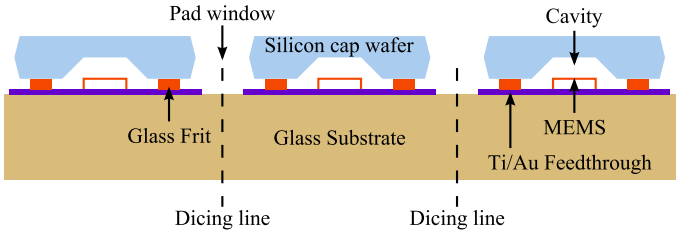

Fig. 1. The conceptual drawing of the wafer level packaging approach for the RF MEMS devices using glass frit bonding.

knowledge, this work is the first comprehensive microwave modeling of an RF MEMS package structure employing low- and high-resistive silicon as the cap wafers and glass frit as the bonding material. The following section of the paper gives the details of package structure and its realization through the process steps. Furthermore, third section presents the microwave characterization of the package together with the utilized circuit model. Third section also presents the measurement results and comparisons between these results and the utilized circuit model simulations.

II. Package Structure, Process Description and Its Realization

The packaging structure presented in this work is formed by bonding of a silicon cap wafer to the device wafer using glass frit as the adhesive bonding material. Fig. 1 shows the conceptual drawing of the package where the cap wafer is either a low-resistive (10 Ω.cm) or a high-resistive (4 kΩ.cm) silicon wafer. The device wafer and the cap wafer are processed independently and then bonded to each other by using glass frit as the adhesive layer in between them.

CPW transmission lines are commonly used in RF MEMS devices. They consist of a signal line and two ground planes. The characteristic impedance of CPW are specified by the width of the signal line and the gap between the signal line and the ground planes. CPW transmission lines are used to evaluate the effects of cap wafer and glass frit. Fig. 2 presents the layout structure of the CPW transmission line to be packaged with tapered transitions and direct transitions.

In order to reduce the effect of measurement errors such as the ones due to calibration, the transmission lines are encapsulated by a total of two cavities and four transitions. This provides a more accurate way for the extraction of low insertion losses particularly for the high-resistive silicon cap structure. The signal trace of the 50 Ω CPW transmission line is 180 μm wide and the gap between the signal trace and one of the ground planes is 20 μm wide. 220 μm ground to ground spacing of the RF probes at hand played a crucial role in the choice of the signal trace width and gap width of the packaged CPW transmission lines. The dielectric loading effect of the glass frit ring together with the silicon substrate on top of it, is calculated by conducting EM simulations using Ansoft HFSS and obtained information is utilized for determining the required tapering under the glass frit rings. The relative permittivity of the glass frit is taken as 4.6 during the EM simulations [20]. In order to minimize reflections due to

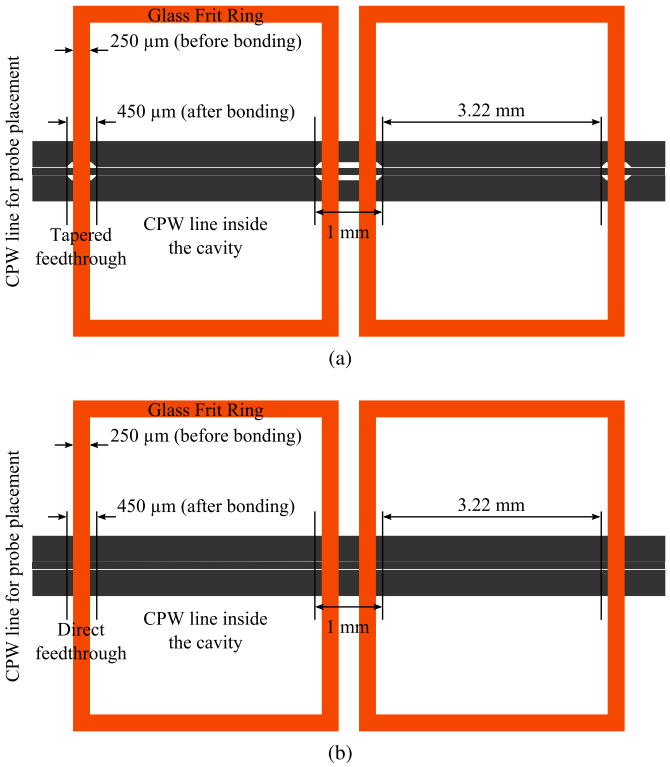

Fig. 2. The layout and dimensions of the structure to evaluate the microwave performance of the planar feedthrough. (a) Tapered feedthrough. (b) Direct feedthrough.

impedance mismatch, tapers in the ground planes were utilized to obtain smooth transition in the presence of the loading effect of the glass frit ring and cap wafer. The thickness of the screen printed glass frit layer is approximately 20 μm prior to bonding and measured to be about 12 μm after the bonding. The width of the glass frit ring is 250 μm which is consistent with the designs previous designs aiming a hermetic package [1]. A prior glass frit bonding is realized using a blank wafer in order to observe the amount of expansion during bonding. The length of the CPW transmission line under each of the glass frit rings are 3220 μm and the total physical length of the transmission line is 9224 μm.

4" silicon wafers with a thickness of 500 μm are utilized during the cap wafer fabrication. The process steps to fabricate the cap wafer is as follows: Silicon wafers are cleaned for removing the possible organic content on the surface of the wafers. Then a thermal dry oxidation process is applied to grow 1.2 μm SiO_2. The SiO_2 layer is patterned by photolithography followed by wet etching, which is used as the mask layer during the double side KOH anisotropic etching process. Both the cavities, which are encapsulating the packaged MEMS devices, and the pad windows, which are the window openings for the measurement probes to reach the CPW line ports, are opened during the KOH anisotropic silicon etching process. Doubled sided KOH process is crucial to obtain pad window openings, which is formed by etching the silicon wafer from two sides. There were no features on the backside of the cap wafer other than the pad window openings. The deoth of the cavities is 250 μm proving a sufficient height above the RF MEMS device without affecting

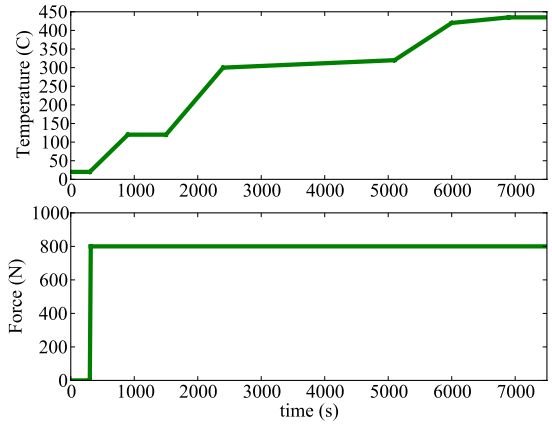

Fig. 3. Graphical representation of developed glass frit bonding recipe.

its characteristics. Following the KOH etching, remaining $Si\,O_2$ layer is stripped and then glass frit is screen printed on the cavity side of the wafer.

For the realization of CPW lines, a 0.5 μm-thick Ti/Au layer is sputtered and patterned on a 4" glass wafer with 500 μm thickness. The bonding process takes place at 430 °C under 800 N force and it take about 6 hours in total using EVG 510 Wafer Bonder. Fig. 3 shows the graphical representation of the developed glass frit bonding recipe. The longest period of the bonding belongs to the cooling. This is completed as a natural cooling process, which takes about four hours.

Then the bonded wafers are diced for the die singulation by making dicing cuts in between pad window openings. SEM images from one of the singulated dies, which are presented in Fig. 4, demonstrates the anisotropically etched pad window opening, the bonded glass frit layer and one of the two ports of the CPW transmission line. Furthermore, a close-up SEM image of glass frit material after the bonding process can be seen in Fig. 4(b) as well.

III. Microwave Modeling and Measurements

Following the realization of the glass frit packaging and the die singulation, RF measurements are carried out using Agilent E8361A vector network analyzer and Cascade Summit 9000 probe station. Fig. 5 shows the packaged transmission lines after dicing. Dicing has an important role in proper landing of the RF probes as shown in the conceptual drawing (inset). Dentate-shape edges are pad window openings formed prior to dicing, which enables the RF probes to access the CPW ports during measurements.

In addition to the RF measurement results, a circuit model for the packaged CPW transmission line structure is utilized to assess the effect of the package and transition. Fig. 6 shows the circuit model used in the microwave characterization. The model consists of CPW line segments (ports and the lines inside the cavities) and the transition sections under the glass frit rings. Characteristic impedances (Z_0, Z_t) attenuation constants (α_0, α_t) and effective permitivities ($\epsilon_{eff,0}$, $\epsilon_{eff,t}$) are the defining parameters of the CPW line segments. The CPW line section between two adjacent cavities are modeled with discontinuity inductances.

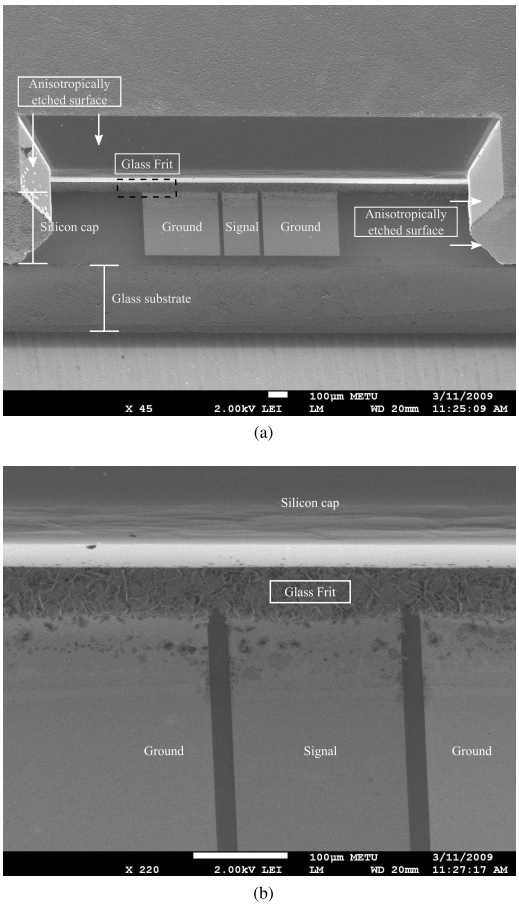

Fig. 4. The SEM photograph of the pad window region. (a) The general view. (b) Close-up view of bonded glass frit region on the feedthrough.

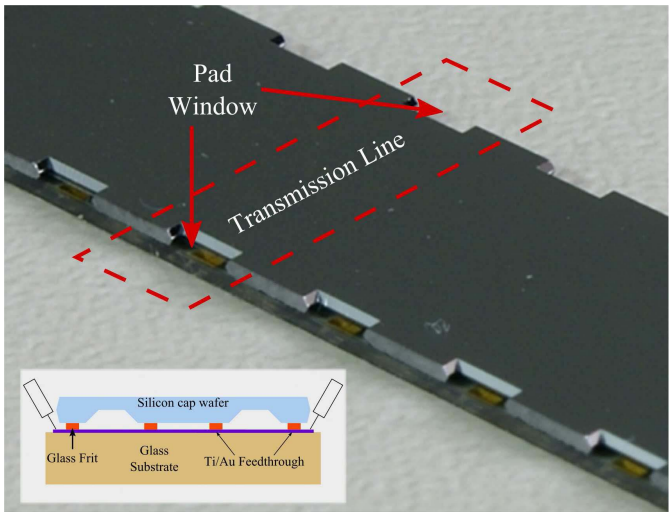

Fig. 5. Packaged transmission lines with the pad windows. Port to port distance is about 9.2 mm within the red dashed parallelogram. (inset: RF probes are used to access feeds of the transmission lines via pad windows).

The physical lengths and the characteristic impedances of the CPW line sections were the constant parameters in the model. By tuning the losses, L_d values in the model, a curve fitting with the measurement results is obtained for the direct feedthrough and the tapered feedthrough structures. In addition

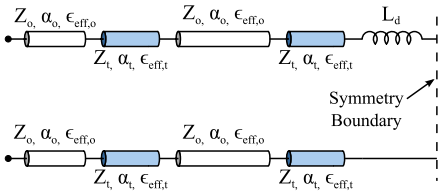

Fig. 6. The circuit schematics used to model the measurement results. (Only left half of the symmetric circuit is demonstrated).

TABLE I
OPTIMIZED CIRCUIT MODEL PARAMETER VALUES OF THE PACKAGED CPW LINES AT 10 GHZ FOR THE LOW-RESISTIVE AND HIGH-RESISTIVE SILICON CAPS WITH TAPERED SECTIONS

Parameters	Low-resistive	High-resistive
Z_0	49.17 Ω	49.17 Ω
α_0	103.8 dB/m	103.8 dB/m
$\epsilon_{eff,0}$	2.7	2.7
Z_t	36.25 Ω	42.55 Ω
α_t	3961 dB/m	221.7 dB/m
$\epsilon_{eff,t}$	10.15	7.36
L_d	33.12 pH	31.81 pH

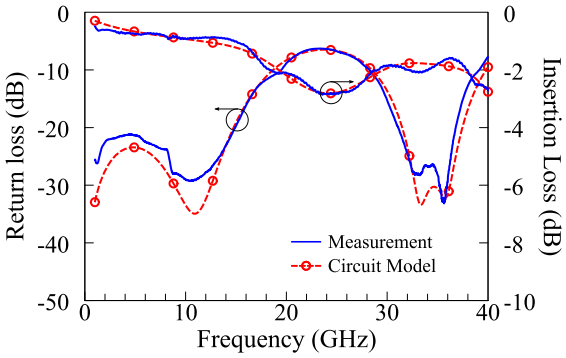

Fig. 7. Measured S-parameters of the unpackaged transmission line with tapered section.

to that, the measurements and circuit model simulations are done with the unpackaged transmission line structures both with direct feedthrough and tapered feedthrough structures. Table I presents the parameter values optimized for the circuit models of the packaged CPW transmission lines using low-resistive and high-resistive silicon caps.

The measurement and circuit model simulation results of the unpackaged and packaged tapered feedthrough CPW transmission lines are presented in Figs. 7 and 8, respectively. The good agreement of the circuit model and the measurement results for both unpackaged and packaged transmission lines indicates the reliability of the utilized circuit model.

As can be seen in Fig. 7, the worst return loss is around -7 dB and the insertion loss is around -2 dB at the higher edge of the frequency band. Fig. 8 demonstrates the results for the packaged CPW line structure using high-resistive silicon caps. The return loss for the structure is better than 15 dB up to 40 GHz and the insertion loss is about 2 dB around 40 GHz. In a comparison between the results of the unpackaged and

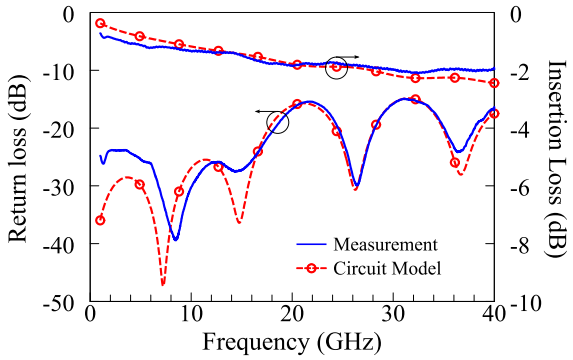

Fig. 8. Measured S-parameters of the packaged transmission line with tapered feedthrough and high-resistive silicon cap.

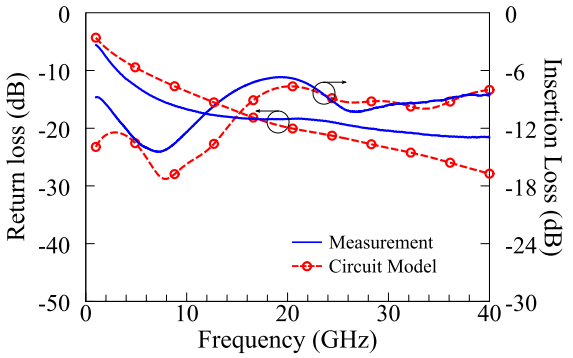

Fig. 9. Measured S-parameters of the packaged transmission line with tapered feedthrough and low-resistivity silicon cap.

packaged transmission lines, it is clear that there is a little increase in the insertion loss about 0.1 dB/transition at 10 GHz, which shows that the package structure does not contribute to the losses of the structure significantly. On the other hand, there is significant development in return loss performance in the packaged structure compared to the unpackaged one. The CPW transmission line is designed considering the loading effects of the glass frit ring and the silicon cap on the CPW line and this is easily deduced from the return loss characteristics.

The measurements are repeated for the CPW transmission lines packaged by low-resistive silicon caps are presented in Fig. 9. The measurement results shows a significant increase in the insertion loss characteristics, which is clearly due to the low-resistive silicon cap. It seems the signal significantly couples to the cap while traveling and the low-resistive silicon path add additional losses to the structure. Furthermore, the return loss is higher compared to the performance in Fig. 8.

In addition to the tapered CPW transmission line structure, the direct feedthrough CPW transmission lines are packaged with both high-resistive silicon caps and low-resistive silicon caps as well. Figs. 10 and 11 present the measurement results and the curve fitted circuit model transmission lines for the high-resistive silicon caps and the low-resistive silicon caps, respectively. As expected, the return loss and insertion loss characteristics are degraded due to the impedance mismatch, which arises from low impedance transmission line segments under the glass frit rings. The direct feedthrough transmission

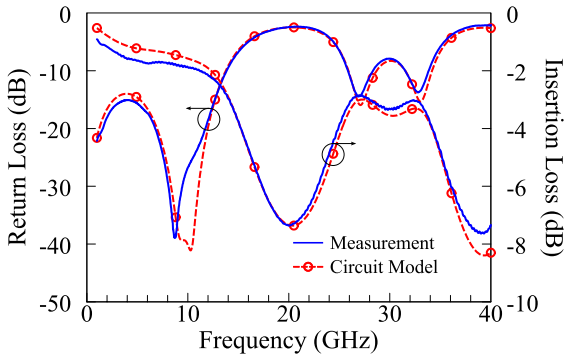

Fig. 10. Measured S-parameters of the packaged transmission line with direct feedthrough and high-resistive silicon cap.

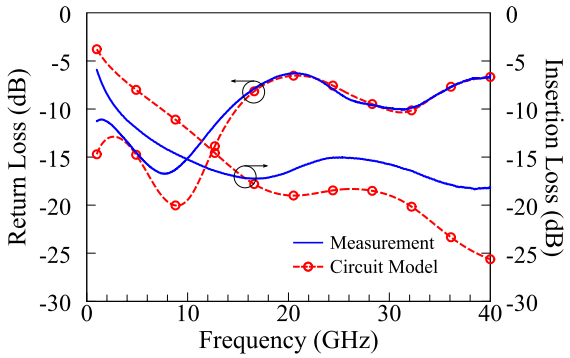

Fig. 11. Measured S-parameters of the packaged transmission line with direct feedthrough and low-resistive silicon cap.

line, which is packaged with low-resistive silicon cap has a characteristic similar to the one in Fig. 9. Since the cap wafer loads the transmission line and introduces the dominant loss mechanism, which is showing conductive properties rather than a dielectric, the effects of impedance mismatch is not clearly observed from the return loss characteristics. On the other hand, the change of dominant loss mechanism can be clearly deduced in Fig. 9 from the increased insertion loss characteristics, in comparison with the insertion loss characteristics in Fig. 8.

Use of high-resistive silicon for the caps should be preferred and carefully designed transitions for feedthrough regions are recommended. Otherwise, silicon caps may increase the loss from 0.1 dB/transition to 1.8 dB/transition at 10 GHz. The loss mechanism is different for the low-resistive silicon caps, however defining a loss factor over the transition region is useful. An imperfect design of the transition region will degrade the insertion and reflection performances. This also limits the flatness of the response as a function of frequency.

IV. Conclusion

Packaging is a significant part of the MEMS process, since the package plays a crucial role not only for the protection but also for the performance of the RF MEMS components. Although there are mature methods for other technologies, MEMS structures require special care due to their fragile mechanical parts. A wafer level packaging approach is introduced in this paper using glass frit as the adhesive material. In addition to being reliable and efficient, glass frit bonding enables the utilization of planar feedthrough structures, which makes it more convenient for RF MEMS devices. Moreover, this paper focuses on the microwave characterization of the packaged CPW transmission lines and it presents a circuit model for the package structure and the package itself. Also in this study, the effects of utilizing low-resistive and high-resistive silicon caps are examined. The feedthrough design with and without transition regions are investigated.

Comprehensive study of proposed packaging approach indicates that the resistivity of the cap wafer is significant having considerable effect on insertion loss performance. In this regard, use of high-resistive silicon caps is recommended. Moreover as expected, EM performance of the feedthrough transition regions are critical. With a little design effort, a satisfactory performance can be easily achieved. It should be noted that, there might be other topologies different than the one proposed in this study. The main effect of the cap is increasing the capacitance. Thus, a transition region introducing an inductive tuning may work efficiently.

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Ilker Comart was born in Tokat, Turkey, in 1983. He received the B.S. and M.S. degrees in electrical and electronics engineering from Middle East Technical University (METU), Ankara, in 2007 and 2010, respectively. He is currently pursuing the Ph.D. degree in electrical and electronics engineering at METU, where he was a Project Assistant from 2007 to 2008. He was a Research Engineer with METU-Microelectromechanical Systems (MEMS) Center from 2008 to 2012. He has been a member of the RF MEMS Group at METU since 2007.

His current research interests include microwave and millimeter-wave RF MEMS component design, process development, and RF MEMS packaging.

Kagan Topalli (S'99–M'08–SM'13) was born in 1979. He received the B.S. and Ph.D. degrees in electrical and electronics engineering from Middle East Technical University (METU), Ankara, Turkey, in 2001 and 2007, respectively. From 2001 and 2007, he has been a Research Assistant with the Department of Electrical and Electronics Engineering, METU. From 2007 and 2010, he has been a Research Engineer with the METU-Microelectromechanical Systems (MEMS) Center. He was a Post-Doctoral Researcher with the Electro-Science Laboratory, Ohio State University, from 2010 to 2012. He is currently an Assistant Professor with the Department of Electrical and Electronics Engineering, TED University, Ankara, Turkey. His current research interests include terahertz (THz) sensors, THz imaging systems, and microfluidics for antenna applications. He has also conducted research on the development, characterization, and integration of novel RF MEMS structures for RF front ends at microwave and millimeter-wave, reconfigurable antennas, phased arrays, microwave packaging, and microfabrication technologies. He is a recipient of the Thesis of the Year Award in 2007 for his Ph.D. dissertation from the METU Prof. Mustafa N. Parlar Education and Research Foundation, the Union of Radio Science-International Young Scientist Award in 2011, and the Research Incentive Award in 2013 from the METU Prof. Mustafa N. Parlar Education and Research Foundation.

Simsek Demir (S'91–M'98) received the B.Sc., M.Sc., and Ph.D. degrees in electrical and electronics engineering from Middle East Technical University (METU), Ankara, Turkey, in 1991, 1993, and 1998, respectively.

From 1991 to 1998, he was a Research Assistant with METU. From 1998 to 1999, he contributed to the atmospheric radar antenna design with IRCTR, TU-Delft, The Netherlands. Since 2000, he has been a Professor with the Electrical and Electronics Engineering Department, METU.

His current research interests include microwave and millimeter-wave active and passive component, and system design, analysis, and modeling. His research topics include the exploitation of RF MEMS technology toward industrial use, power amplifier design, modeling and implementation, and radar applications. He is a recipient of several awards including NATO A2 Fellowship, which supported him as a Visiting Researcher with the University of Massachusetts, Amherst, in 1995.

Tayfun Akin was born in Van, Turkey, in 1966. He received the B.S. (Hons.) degree in electrical engineering from Middle East Technical University (METU), Ankara, in 1987, and went to the USA in 1987 for his graduate studies with a graduate fellowship provided by the NATO Science Scholarship Program through the Scientific and Technical Research Council of Turkey. He received the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1989 and 1994, respectively. Since 1995, 1998, and 2004, he has been an Assistant Professor, an Associate Professor, and a Professor, respectively, with the Department of Electrical and Electronics Engineering, METU. He is the Director of the METU-Microelectromechanical Systems (MEMS) Center, which has a 1300-m2 clean room area for 4" to 8" MEMS processing. He raised and managed over 65M USD funding for several National and International projects, including EU FP6, FP7, NATO SfS, and NSF-USA Projects. His current research interests include MEMS, Microsystems Technologies, uncooled infrared detectors and readout circuits, inertial microsensors, silicon-based integrated sensors and transducers, and analog and digital integrated circuit design.

He has served in various MEMS, EUROSENSORS, and TRANSDUCERS Conferences as a Technical Program Committee Member. He was the Co-Chair of the 19th IEEE International Conference of Micro Electro Mechanical Systems (MEMS 2006) held in Istanbul, and he was the Co-Chair of the Steering Committee of the IEEE MEMS Conference in 2007. He is the Steering Committee Member of the 18th International Conference on Solid-State Sensors, Actuators, and Microsystems (Transducers 2015). He is the recipient of the First Prize in Experienced Analog/Digital Mixed-Signal Design Category at the 1994 Student VLSI Circuit Design Contest organized and sponsored by Mentor Graphics, Texas Instruments, Hewlett-Packard, Sun Microsystems, and Electronic Design Magazine. He is the co-author of the Symmetric and Decoupled Gyroscope project, which received the first prize award in the operational designs category of the International design contest organized by DATE Conference and CMP in 2001. He is also the co-author of the Gyroscope project, which received the third prize award of the 3-D MEMS Design Challenge organized by MEMGen Corporation (currently, Microfabrica).