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Plasma-activated direct bonding of diamond-on-insulator wafers to thermal oxide grown silicon wafers

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ABSTRACT

Diamond-on-insulator (DOI) wafers featuring ultrananocrystalline diamond are studied via atomic force microscopy, profilometer and wafer bow measurements. Plasma-activated direct bonding of DOI wafers to thermal oxide grown silicon wafers is investigated under vacuum. DOI wafer with chemical mechanical polishing (CMP) on the diamond surface makes a poor bonding to silicon wafers with thermal oxide. Our results show that plasma enhanced chemical vapor deposition of silicon dioxide on top of the DOI wafer, CMP of the oxide layer and annealing are essential to achieve very high quality direct bonding to thermal oxide grown on silicon wafers. Plasma activation results in the formation of high quality bonds without exceeding 550 °C in the direct wafer bonding process.

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1. Introduction

Diamond is an attractive alternate membrane material to silicon for microelectromechanical systems (MEMS) applications because of its superior mechanical, electrical and thermal properties [1]. High Young's modulus, low dielectric constant, very large thermal conductivity and high dielectric strength of diamond (see Table 1) are all in favor of diamond as a strong candidate to be used for electromechanical transducers. Because of its high radiation resistance, chemical inertness and extreme hardness, diamond is best suited for high temperature, high power and radiation-hard devices [1]. Therefore, diamond is a promising membrane material for improving performance and reliability of capacitive micromachined ultrasonic transducers (CMUTs) [2].

The CMUT cavity is formed with the patterned etch of the thermally grown SiO_2 insulation layer on the silicon wafer. The top surface of this patterned wafer is directly bonded to commercially available silicon-on-insulator (SOI) wafer under vacuum and single crystal silicon device layer of the SOI wafer becomes the membrane sealing the cavities following the removal of the bulk silicon and buried oxide [3]. Using diamond-on-insulator (DOI) wafer instead of SOI wafer can form diamond membranes with a similar process flow if the direct bonding of diamond and patterned silicon dioxide surfaces is successfully achieved. In this respect, the direct bonding potential between diamond and silicon dioxide surfaces should be explored for full wafer to wafer contact.

Although direct bonding of silicon and silicon dioxide surfaces is accomplished and readily employed in the production of silicon membranes [3], the bonding of diamond and silicon dioxide surfaces has not been explored yet. This is due to (1) lack of high quality diamond films with small grains and smooth surfaces, (2) extreme hardness of diamond surface reducing the smoothing performance of chemical mechanical polishing (CMP), and (3) plasma activation becoming less effective due to high chemical stability of carbon bonds in diamond. These facts make the direct wafer bonding of diamond to SiO_2 very challenging. The deposition of a SiO_2 interlayer is widely used to achieve the bonding of dissimilar materials or materials with surface irregularities such as roughness [4]. The wafer bonding of diamond and silicon surfaces is achieved with a high temperature oxide (HTO) deposited as an additional layer on diamond [5]. Complete direct bonding of diamond to silicon was achieved under a uniaxial mechanical stress of 32 MPa in a dedicated ultrahigh vacuum chamber at annealing temperatures above 1150 °C with some cracks on the diamond film [6]. Plasma-activated direct bonding of silicon and diamond-like-carbon (DLC) with an annealing temperature of 450 °C was used to fabricate silicon-on-diamond structure with hydrogen-induced layer transfer method [7].

Recently, ultrananocrystalline diamond (UNCD) has become commercially available on Si wafers, featuring smaller grain size and surface roughness (3–4 nm) than conventional diamonds (Advanced Diamond Technologies (ADT), IL, US). The surface roughness of UNCD is further reduced below 1 nm by CMP. In this work, we investigate the 4-in UNCD DOI wafers via atomic force microscopy, profilometer and wafer-bow measurements. We study the direct bonding of UNCD DOI wafers onto SiO_2 grown Si wafers which is a critical step to have diamond membranes over vacuum sealed cavities.

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Table 1
Material properties of Si, SiO_2, UNCD, and diamond at room temperature [1]: Young's modulus (E), density (ρ), Poisson's ratio (v), thermal conductivity (k), hardness (h), thermal expansion coefficient (α), dielectric constant (ϵ), and dielectric strength (E_{ds}) are shown for comparison.

	Si	SiO_2	UNCD	Diamond
E (GPa)	160	73	850	1050
ρ (kg/m^3)	2332	2200	3300	3520
v	0.29	0.17	0.1	0.2
h (kg/mm^2)	1000	1000	10000	10000
k ($W/m-K$)	151	1.4	1200	2000
α ($10^{-6}/K$)	2.5	0.5	0.8	0.8
ϵ	11.7	3.8	5.7	5.7
E_{ds} (10^5V/m)	3.7	100	100	100

2. Experiment

Silicon wafers with SiO_2 are realized via thermally oxidizing base prime <100> silicon wafers (4-in, 5–10 Ω cm, 525 ± 25 μm) at 1000 °C. The oxide thickness of 1.5 μm is achieved using a combination of wet and dry oxidation. Initial and final stages of the oxidation are performed with dry oxidation whereas in-between wet oxidation is employed. Oxidation temperature of 1000 °C is used to have good control over the thickness and uniformity of the oxide over the wafer. The average oxide thickness of 9-point measurements across the wafer using spectroscopic reflectometer (NanoSpec, Nanometrics, CA, US) is within %1 of the target thickness of 1.5 μm and the standard deviation of oxide thickness is less than 4 nm across the wafer. The wafers S_{1-4} and A_1 have these thermal oxide layers (see Table 2).

Commercially available DOI wafers feature UNCD layer with 300–350 MPa compressive stress and thickness variation of %20 over the whole wafer. A compressive stress in the membrane material will cause buckling of the membrane and will degrade device performance. Thickness variation will cause frequency shift from the intended frequency range of operation. Therefore, DOI wafers with custom deposited UNCD layer are used instead of the regular DOI wafers. Diamond-on-insulator wafers that are custom prepared by ADT feature 0.5 μm UNCD layer with minimum residual stress (-50 MPa$<S<$50 MPa), smallest grain size and surface roughness (R_a) below 1 nm over 1 μm thermal oxide grown <100> base silicon. The low surface roughness is achieved with the chemical mechanical polishing of the UNCD surface by ADT. The DOI wafer labeled B_1 is formed aforementioned.

The DOI wafers without the final CMP step are used to study the effect of deposited SiO_2 as an intermediate layer on direct bonding. In this respect, DOI wafers, C_1 and D_1, have additional SiO_2 deposited via plasma enhanced chemical vapor deposition (PECVD) at 300 °C (STS PECVD, Surface Technology Systems, Newport, UK). The initial deposited oxide thickness of 0.5 μm is reduced down to 0.1 μm, by properly adjusting the CMP duration based on the initial processing of the test wafers (<100> base silicon wafer with 0.5 μm PECVD oxide). Because of the multi-layer nature of the DOI wafers, the spectroscopic reflectometer measurements of the remaining oxide thickness are performed on the test wafers. The CMP is performed by Axus Technology (Chandler, AZ, US) using Semi-Sperse 25-E slurry (Cabot Microelectronics, IL, US) diluted with water (slurry:water) (1:1) on Westech Model 472 CMP System (Speedfam-IPEC, Japan). Wafer cleaning of the slurry remaining after the CMP is performed on OnTrack DSS-200 Post CMP Cleaner (OnTrack, CA, US). The wafer C_1 was kept as is whereas the wafer D_1 has been annealed at 400 °C under N_2 flow in Thermco furnace (Thermco Systems, West Sussex, UK) for 19 hours to densify the wafer (see Table 2). This annealing temperature higher than the oxide deposition temperature of 300 °C and longer duration of annealing are employed to ensure the extraction of trapped H_2 gas in the PECVD oxide layer [8]. The annealing is performed after the CMP in order to (1) facilitate the diffusion of the trapped gas through a thinner oxide layer, and (2) enhance the surface cleanliness with the better removal of small size slurry particles on the unannealed PECVD oxide surface rather than annealed oxide surface. Higher annealing temperatures are avoided to protect the diamond layer from reacting with present O_2 molecules in the open-ended atmospheric furnace and to release the trapped H_2 gas in the oxide layer in a slow, controlled process [8].

Table 2 summarizes all the wafers reported in this study and lists their constituent layers. The surface roughness and the wafer bow are measured for each wafer, and given in Tables 3 and 4, respectively. The wafer pairs of (S_1 and A_1), (S_2 and B_1), (S_3 and C_1), and (S_4 and D_1) are direct bonded to form A_1^1, B_1^2, C_1^3, and D_1^4, respectively. The quality and stability of these direct-bonded pairs are analyzed by scanning acoustic microscopy (SAM).

Table 2
Description of wafer pairs: IDs, bonded wafers, wafer constituents and processing steps.

ID	Bonded wafers	Wafer constituents on top of silicon wafer	Processing steps
A_1^1	S_1	1.5-μm thermal SiO_2	$Cleaning_1$
	A_1	1.5-μm thermal SiO_2	$Cleaning_1$
B_1^2	S_2	1.5-μm thermal SiO_2	$Cleaning^1$
	B_1	1-μm thermal SiO_2	CMP
		0.5-μm UNCD	and $cleaning_2$
C_1^3	S_3	1.5-μm thermal SiO_2	$Cleaning_1$
	C_1	1.-μm thermal SiO_2	CMP
		0.5-μm UNCD	and $cleaning_3$
		0.1-μm PECVD-SiO_2	
D_1^4	S_4	1.5-μm thermal SiO_2	$Cleaning_1$
	D_1	1-μm thermal SiO_2	CMP,
		0.5-μm UNCD	densification,
		0.1-μm PECVD-SiO_2	and $cleaning_3$

3. Results and discussion

3.1. Characterization

The atomic force microscopy (AFM) (5500 LS, Agilent Technologies, Santa Clara, CA, US) measurement of a 10×10 μm^2 thermal oxide surface gives a root-mean-square (RMS) roughness (R_q) of 1.5 Å and a roughness average (R_a) of 1.2 Å whereas that of PECVD SiO_2 surface after CMP gives R_q and R_a of 4.5 Å and 2.9 Å , respectively. PECVD SiO_2 was smoothened by CMP; however, the polished oxide was still rougher than the thermal grown SiO_2. AFM image of UNCD surface after CMP is given in Fig. 1, and surface roughness values for R_q and R_a are 16.5 Å and 10.7 Å, respectively. Surface roughness of DOI wafers (B_1, C_1, and D_1) is further studied across the 4-in wafers using Dektak 8 profilometer (Veeco, Plainview, NY, US) with 0.2 μm stylus attached.

Table 3
Surface roughness measurements of UNCD wafers: B_1, C_1, and D_1. R_q is the RMS roughness and R_a is the roughness average, given in the brackets. All units are in Angstrom (Å).

Wafer ID	B_1	C_1	D_1
Position (cm, cm)	$R_q(R_a)$ Å(Å)	$R_q(R_a)$ Å(Å)	$R_q(R_a)$ Å(Å)
A(0,0)	11.0(8.5)	9.8(7.9)	9.8(8.0)
B(−1,1)	13.2(10.2)	10.4(8.1)	13.4(11.0)
C(−2,2)	12.6(10.0)	8.5(10.7)	8.8(7.0)
D(−3,3)	12.7(10.1)	8.7(7.0)	10.3(8.3)
E(1,−1)	15.0(11.9)	10.0(8.0)	8.6(6.7)
F(2,−2)	16.0(13.1)	12.3(9.8)	10.6(8.5)
G(3,−3)	13.9(11.0)	9.6(7.6)	8.7(7.1)
K(0,−1)	16.3(12.6)	9.4(7.4)	15.1(12.4)
J(0,−2)	15.7(12.5)	9.0(7.2)	8.2(6.5)
I(0,−3)	13.2(10.4)	8.9(7.2)	8.6(6.8)
H(0,−4)	15.7(12.3)	12.2(9.8)	11.3(9.0)

Table 4
Wafer bow measurements of DOI and thermal oxide grown Si wafers: radius of curvature R_c and wafer bow.

Wafer ID	R_c (m)	Wafer bow (μm)
S_1	−190	5.38
A_1	−525	2.99
S_2	2501	−2.92
B_1	−18	43.10
S_3	197	−6.01
C_1	−214	3.42
S_4	125	−7.84
D_1	−225	5.15

Scan sites, labeled as A, B, C, D, E, F, G, H, I, J and K with their respective coordinates, are shown in Fig. 2. Line path of 50 μm was scanned with 15000 data points with 1 mg force at each location. Root-mean-square roughness (R_q) and average deviation (R_a) for each scan are summarized in Table 3. As seen from Table 3, wafer B_1 is slightly rougher than wafers C_1 and D_1 according to profilometer measurements. AFM results show that wafer B_1 is 3 times rougher than wafer C_1 and D_1. This is because the resolution of the profilometer is not as good as AFM to measure roughness values well below 1 nm. There are no significant surface roughness differences between wafers C_1 and D_1 showing that densification (composed of annealing at 400 °C under N_2 for 19 hours) does not affect the surface morphology of DOI wafers significantly.

Wafer bow is measured using FLX-2320-S thin film stress measurement system (Toho Technology Corporation, Nagoya, Japan). Table 4 summarizes the wafer bow data for both DOI and thermal SiO_2 grown Si wafers. Positive wafer bow (negative radius of curvature) represents a convex surface, meaning the center of the wafer makes the first contact to the ideal flat surface. All wafers except B_1 are fairly flat. High wafer bow of B_1 wafer is a result of the removal of back side thermal oxide.

3.2. Cleaning

Thermal SiO_2 atop wafers (S_{1-4}, A_1) were cleaned via a standard cleaning (cleaning$_1$) procedure composed of agitation with SC1 (NH_4OH:H_2O_2:H_2O) (1:1:5) at 75 °C for 10 min, brush scrubbing and megasonic cleaning, and agitation with SC2 (HCl:H_2O_2:H_2O) (1:1:6) at 75 °C for 10 min. UNCD atop wafer (B_1) was cleaned via another standard cleaning (cleaning$_2$) procedure composed of agitation with DHF (HF:H_2O) (1:10) at 75 °C for 10 min prior to SC1. PECVD SiO_2 atop wafers (C_1, D_1) were cleaned via SC1, brush scrubbing and megasonic cleaning only (cleaning$_3$). Different cleaning procedures were employed for wafers finished with thermal or PECVD SiO_2 and UNCD as cleaning chemicals (such as HF) attack the wafer end-materials (such as SiO_2). These different cleaning steps for different wafers prevent roughening the wafers' surface.

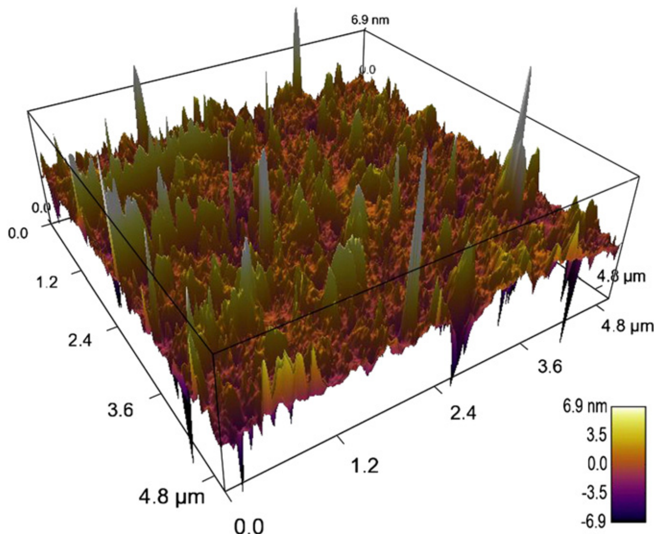

Fig. 1. (Color online) Atomic force microscopy image of UNCD surface after CMP (R_a = 10.7 Å, R_q = 16.5 Å (5×5 μm)).

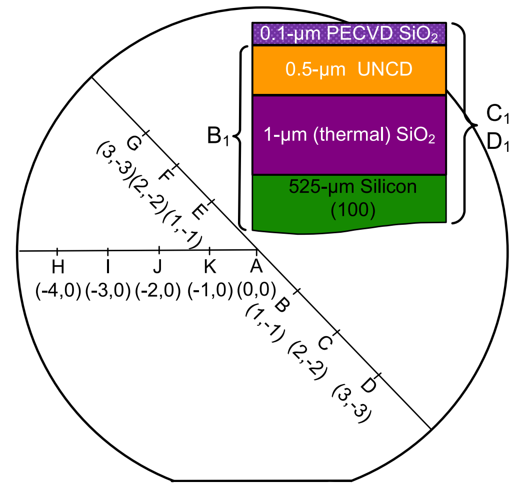

Fig. 2. (Color online) The locations of data acquisition (points A through H) across the 4-in wafer for uniformity studies. Inset shows the side sketch of the DOI layers.

3.3. Direct bonding

Direct wafer bonding forms molecular bonds between two smooth, clean surfaces. These molecular bonds hold for high temperature environments since no adhesive layer is used in the bonding process [9]. Because no voltage is applied during the formation of the direct bonds, the insulation layers are intact and the interface is virtually free of charges. These make direct wafer bonding an ideal process for CMUTs.

Direct wafer bonding requires high temperature anneal around 1000–1100 °C to form permanent bonds. High temperature anneal is not suitable for some materials and processes. It can introduce cracks in materials with large thermal expansion coefficient mismatch such as diamond and silicon [6]. Direct wafer bonding at a low temperature process (400–500 °C) requires either ultra high vacuum (UHV) conditions (~10^{-10} mbar) [10] or plasma activation of the mating surfaces [11]. Most commercially available wafer bonding systems employ high vacuum conditions (~10^{-5} mbar) and a maximum bonding temperature of 550 °C to be used with plasma activation systems for low temperature direct bonding applications.

In our bonding experiments, different wafer pairs are used as given in Table 2. Both contacting surfaces of the wafer pair are cleaned using EVG301 wafer cleaner (EVGroup, St. Florian am Inn, Austria), activated using EVG810LT plasma activation system (EVGroup, St. Florian am Inn, Austria) and bonded using EVG520IS wafer bonding system (EVGroup, St. Florian am Inn, Austria). N_2 plasma is used in all cases except the wafer (B_1) that was exposed to O_2 plasma. This is because O_2 plasma is much more effective on the activation of carbon compounds than N_2 plasma.

The wafer surfaces are contacted in high vacuum (10^{-4} mbar) at room temperature and the wafer pair is pressed with a piston force of 10 kN. Unlike direct bonding of smooth silicon surfaces, direct bonding involving rough surface requires high piston force for intimate contact of the bonding wafers [12]. The wafer pair is heated to 550 °C, kept at this temperature for 7 hours, and then cooled down to 75 °C before the

piston force is removed and the chamber is vented. Because plasma activation has an active lifetime of a few hours at room temperature, steps of cleaning, surface activation and bonding are performed consecutively without any delay [11]. Maximum bonding temperature of 550 °C for the wafer bonder is used to increase the surface energy of diamond-oxide bonding as much as possible, and the same bonding temperature is used in all bonding experiments for comparison, even though lower bonding temperatures may also result in similar surface energy for oxide–oxide bonding.

The bonded pairs are examined under scanning acoustic microscopy (SAM) (D9000, Sonoscan, Elk Grove Village, IL,US). The C-SAM micrographs of bonded wafers (A_1^1, B_1^2, C_1^3, and D_1^4) are shown in Fig. 3 (a–d). C-SAM micrograph of bonded wafer A_1^1 is shown in Fig. 3(a). Unbounded regions are shown in white. Good bonding is observed except the defective part closer to the flat side of the wafer. Possible reasons for the line void (observed in bottom left) could be surface scratch. The voids observed at three locations separated by 120° on the outer rim of the wafer correspond to bonding glass positions where no pressure is applied while bonding. The small voids observed could be due to surface defects or airborne particle due to wafer handling. This is the plasma-activated bonding scheme used for silicon membrane formation. Bubbles do not exist in the case of bonding of plasma-activated thermal oxide grown on Si wafers [11].

For the next bonding, the wafers were activated with O_2 plasma. Due to the high wafer bow of B_1 wafer, flags with 150 μm spacing are used instead of the standard flags with 50 μm spacing. The bonding of B_1^2 is observed around an approximate circular thin line (Fig. 3(b)). A large portion of the mating surfaces is not bonded. This shows that direct bonding of diamond onto SiO_2 is not very feasible. This poor bonding experience between SiO_2 and diamond surface could be due to (1) high surface roughness, (2) high wafer bow of B_1, and (3) insufficient plasma activation of diamond surface, which would not allow formation of a strong bond and would allow debonding over a large surface area after piston force release due to the elastic energy of B_1 wafer.

The bonding of wafer C_1^2 is good except small regions distributed over the surface (Fig. 3(c)). Comparison of Fig. 3(b) and (c) shows that employment of a thin SiO_2 layer improves the direct bonding significantly. The three unbonded locations separated by 120° are due to the bonding glass position whereas the slightly bigger white dots may be related to the released gas from the PECVD oxide layer on top of the diamond.

In the last bonded wafer pair D_1^4, the bonding quality is very good (Fig. 3(d)). The bonding glass positions are unbonded as usual; however, apart from the surface scratch/irregularity related unbonded line-like feature (at the bottom), the D_1^4 quality is as good as A_1^1. Comparison of Fig. 3(c) and (d) shows the importance of densification before the bonding process. Therefore, through employment of a thin SiO_2 layer and proper surface treatment, it is possible to achieve a successful direct bonding for DOI wafers (Fig. 3(d)).

The significance of densification is that the H_2 gas trapped inside the PECVD-grown SiO_2 during deposition is released via annealing

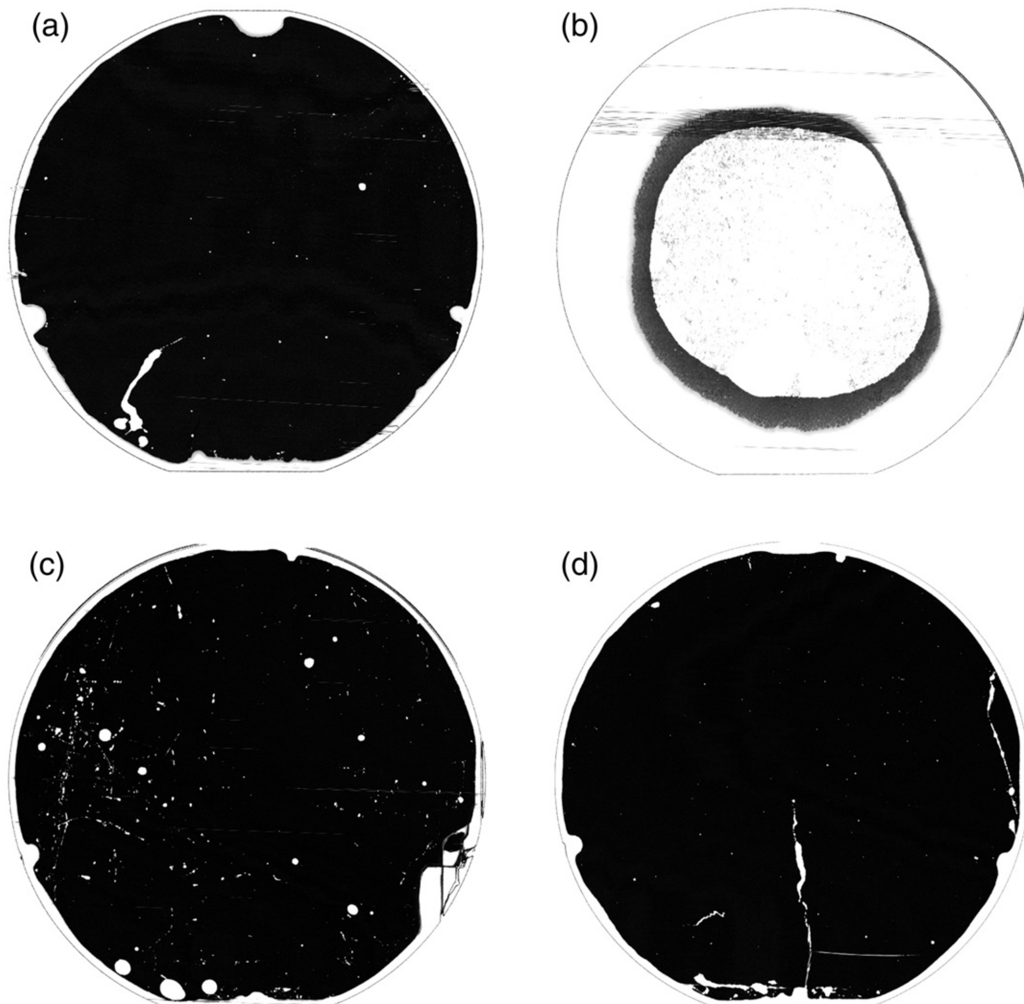

Fig. 3. C-SAM micrograph of direct bonded wafer pairs (a) A_1^1, (b) B_1^2, (c) C_1^3, and (d)D_1^4. Unbonded regions are shown in white whereas bonded regions are shown in black.

prior to direct bonding [8] so that the vacuum sealed cavities will not be filled with the released gas during bonding at 550 °C [9]. This explains the higher quality direct bonding of D_1^4 than C_1^3.

4. Conclusions

Diamond-on-insulator (DOI) wafers employing UNCD has been characterized via atomic force microscopy, profilometer and wafer-bow measurements. With an employment of a SiO_2 layer on top of diamond, direct wafer bonding of DOI and oxidized Si wafer is realized. Further densification of SiO_2 on DOI wafer via annealing under N_2 is shown to improve the uniformity and quality of the wafer bonding. Our results promise the fabrication of diamond membranes via direct bonding for microelectromechanical systems applications.

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