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Hybrid connection of RF MEMS and SMT components in an impedance tuner

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ABSTRACT

This paper presents a systematic construction of a model for a hybrid connected RF MEMS and SMT components in a reconfigurable impedance tuner. The double stub hybrid impedance tuner which employs a high number of MEMS switches is selected to demonstrate the feasibility of the connections. In the hybrid tuner, MEMS switches are actuated with DC bias signals, where SMT resistors de-couple RF from the DC lines. The hybrid tuner is realized in two steps, where the MEMS impedance tuner is fabricated on a glass substrate using an in-house surface micromachining process, and the SMT resistors are mounted on the glass substrate following the MEMS fabrication. The parasitics introduced by the SMT resistors and their connections in the hybrid tuner are modeled in 1–20 GHz band. The constructed model is used to simulate the hybrid impedance tuner, which is capable of matching 2^{10} points on the Smith Chart, covering a wide impedance range 1.5–393 Ω in the real and −210 to 220 Ω in the imaginary parts at 18 GHz. The hybrid impedance tuner is measured for 25 switch combinations to verify the model in which a good agreement is obtained. The comparison of the simulation and measurement results show that the constructed model is successful in terms of handling parasitics of a hybrid structure up to 20 GHz where the parasitics vitally affect the device performance.

1. Introduction

Micro-Electro-Mechanical Systems (MEMS) technology has been offering high-performance, low-cost, and reconfigurable components since the last decade for the RF applications. Among these components, reconfigurable antennas, phase shifters, filters, and impedance tuners are strong candidates for new generation, highly integrated, and reconfigurable RF front ends. Although the research on the RF MEMS technology focuses more on long-term reliability, power handling, and packaging; modeling and integration issues are also significant as RF MEMS components are strong alternatives of many passive components in a highly integrated RF front end. This integration is achieved with hybrid connection of active components, RF MEMS components, and any additional supporting SMT components; however, hybrid connection of all these components may drastically reduce the system performance if parasitic effects are not counted for. These effects should be investigated and modeled in detail for any circuits that use hybrid connections. One such a circuit is the hybrid connection of an RF MEMS impedance tuner with SMT resistors.

RF MEMS impedance tuners are one type of the promising components that can be integrated with a reconfigurable RF front end. Several MEMS impedance tuners and matching networks with different approaches have been presented so far [1–6]. All those tuners used a high number of MEMS switches, which inherently brought a high number of DC biasing controls. These DC biasing controls may affect the RF performance significantly; and these effects either should be set off carefully by the design, as in [5], or biasing resistors should be used, as presented in [7–9]. In [7–9], the biasing resistors are implemented with a SiCr resistive layer, which is a part of the MEMS fabrication process. However, even the biasing of the MEMS switches is supplied monolithically, the integration of MEMS components with the other active or passive components in the system is unavoidable since the system is not only composed of MEMS components. Thus, modeling the interaction between the MEMS and the other components becomes crucial in terms of having the desired system performance.

This paper presents a systematic approach for modeling a hybrid application in which RF MEMS and SMT components are used to implement a double stub impedance tuner. The hybrid tuner structure is intentionally selected as a demonstrator of the modeling approach since the tuner not only includes high number MEMS switches that necessitates the same high number of biasing resistors, but also possesses the parasitics of both types of components and the connections. This selection is also made to emphasize the effects of the parasitics as well because a high number of components are used. The hybrid tuner is fabricated in two steps, where the MEMS part is first fabricated using an in-house surface micromachining process on a glass substrate. Then, SMT resistors are mounted on the MEMS impedance tuner chip to de-couple the DC lines from the RF lines. At this point,

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a circuit model is constructed systematically in 1–20 GHz band by which the effects of each and every part of the structure, such as the parasitics of the MEMS and SMT components as well as the interactions among these components, can be observed. The simulations and measurement results are compared in 1–20 GHz band with a center design frequency of 18 GHz, where the effects of the parasitics can be more easily observed.

2. MEMS switch design

Fig. 1 shows the MEMS switch that is specifically designed for the hybrid impedance tuner. The designed switch is a capacitive, shunt MEMS switch which has three capacitances (C_{sb} and two C_{bg} capacitances) in contrast to a standard capacitive MEMS switch that has a single shunt capacitance [10,11]. This switch topology is selected because of the connection and the biasing requirements of the hybrid impedance tuner. Since each MEMS switch has to be biased independently, the bias voltages should be capacitively coupled as in [6]. Different than [6], the three capacitances of the MEMS switch are all tunable and implemented on the same MEMS bridge. The area of the MEMS switch is $350 \times 1024\,\mu m^2$.

Fig. 2 shows the circuit model of the designed switch. Additional components are inserted to the conventional *CLR* circuit model [11], which are crucial to estimate the performance of the hybrid connection between the SMT resistors and RF MEMS switches. *CLR* circuit model was used safely in order to simulate the RF MEMS switch considering the width of the MEMS bridge [12]. In the circuit model, C_{sb} and C_{bg}s are the conventional capacitances between the MEMS bridge and the CPW line. C_{pass} stands for the capacitance of the overpasses that are used to patch up CPW grounds which are delimited by the DC bias lines. *Line*1 and *Line*2 represent the metallic bias connections from the MEMS bridge to the suspended ground connection and from suspended ground connection to the end of the CPW grounds, respectively. These connections are modeled as CPW lines where the signal line is the metallic bias line and the grounds are the grounds of the main CPW line. As for the circuit model introduced in Fig. 2, Table 1 presents the values of the parameters used in the MEMS switch design, which are all calculated using closed form formulas. It should be mentioned here that the impedance of

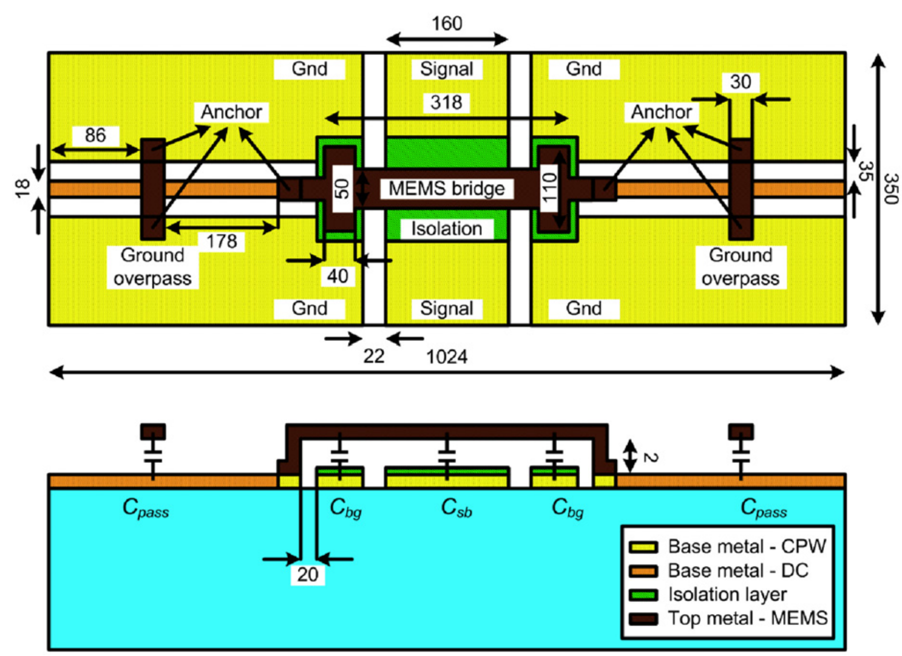

Fig. 1. The top and side views of the designed MEMS switch.

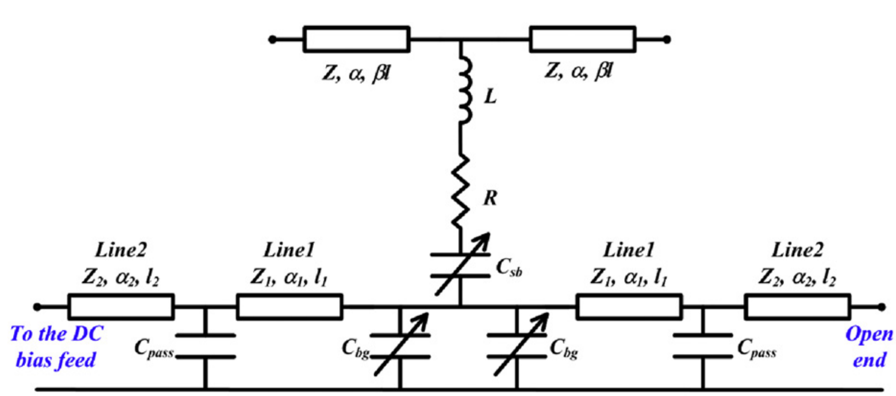

Fig. 2. The circuit model of the designed MEMS switch.

*Line*1 and *Line*2 are selected as high as possible, and it is not feasible to increase this value further because the line impedance starts to be very sensitive to the lithographic tolerances.

The proposed MEMS switch is designed using Microwave Office and verified by full-wave electromagnetic (EM) simulations in HFSS v9.2. During the circuit simulations, all the fringe effects of the MEMS capacitances are included using the closed form interlayer fringe capacitance formulas taken from [13]. With this method, the design cycle is accelerated, and fewer full-wave simulations are required. The simulation results of the design are given in Section 5 compared with the measurements.

3. SMT-RF MEMS hybrid impedance tuner design

Fig. 3 shows the schematic of the designed SMT-RF MEMS hybrid impedance tuner. The hybrid tuner has a double stub structure with 5 MEMS switches on each stub, which makes a total of 10 MEMS switches. The double stub structure is specifically chosen for the hybrid tuner since it includes a high number of MEMS switches each of which requires an independent biasing resistor. In order to demonstrate the hybrid use with MEMS components, SMT resistors are used as the biasing resistors. The SMT components have comparably large dimensions, and their parasitics as well as the connections to the MEMS components vitally affect the RF performance of the circuit. The aim of this work is to make a hybrid design that includes these effects, and therefore, the center design frequency is chosen as 18 GHz where the parasitic effects are notably observable.

Together with the MEMS switches and the SMT resistors, the hybrid tuner also contains CPW line sections that connect the MEMS switches, a CPW interconnection line between the stubs, and two CPW T-junctions that connect the stubs to the interconnection line. The design parameters of all of these components are very effective and should be chosen carefully for obtaining desired impedance coverage from the hybrid tuner. The design parameters of the hybrid tuner are the number of MEMS switches, the lengths and the characteristic impedances of the CPW lines. The parameters that are used in the hybrid tuner design are given in Table 2. The wide spread impedance coverage of the hybrid tuner enables observation of the parasitics at different impedance ranges. Microwave Office is used for the simulations by cascading the circuit models of each part of the hybrid impedance tuner.

Full-wave EM simulation of a MEMS structure with a high number of switches is usually not feasible because of the

Table 1
The designed and the extracted MEMS switch parameters.

	Simulated		Extracted	
	Up-st.	Down-st.	Up-st.	Down-st.
C_{sb} (fF)	44	636	35	643
C_{bg} (fF)	25	354	20	358
C_{pass} (fF)	5	5	4	4
L (pH)	6.7	6.7	6.7	6.7
R (Ω)	0.14	0.24	0.14	0.24
Z (Ω)	55		55	
l (μm)	175		175	
ε_{eff}	2.78		2.78	
α (dB/m)	0.86 at 20 GHz		1.4 at 20 GHz	
Bridge height	2 μm		2.6 μm	
Z_1 and Z_2 (Ω)	105		105	
$\alpha_{1,2}$ (dB/m)	1.37 at 20 GHz		2.2 at 20 GHz	
$\varepsilon_{eff1,2}$	2.83		2.83	
l_1 (μm)	186		186	
l_2 (μm)	77		77	

Table 2
The design parameters used in the MEMS impedance tuner design.

Number of stubs = 2, Number of MEMS switches = 10		
Interconnection line		
Z_{int} (Ω)	L_{int} (μm)	α_{int} (dB/m)
47	1090	91
CPW Gap/Signal/Gap (μm)		
35	138	39
Lines between MEMS switches		
Z_s (Ω)	L_s (μm)	α_s (dB/m)
60	380	70
CPW Gap/Signal/Gap (μm)		
19	178	19

All of the loss parameters are calculated at 20 GHz.

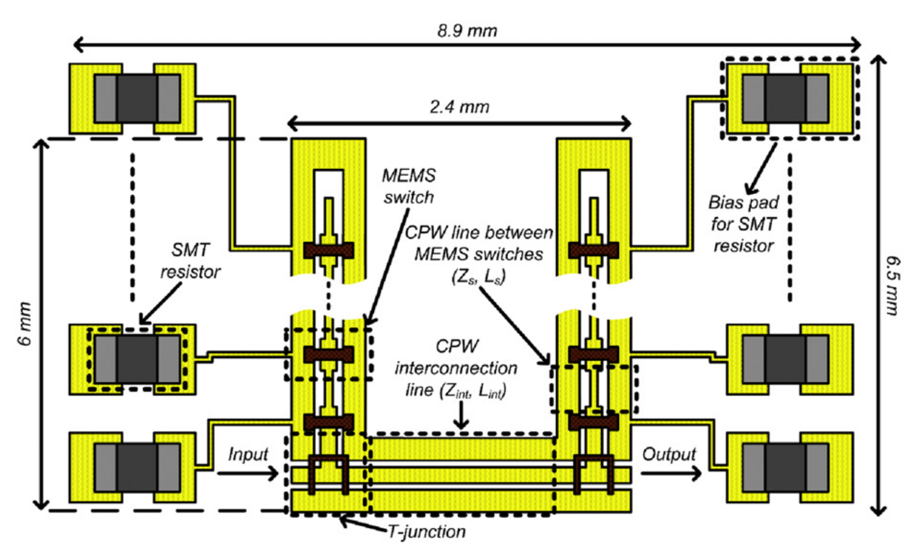

Fig. 3. The schematic of the designed hybrid MEMS impedance tuner.

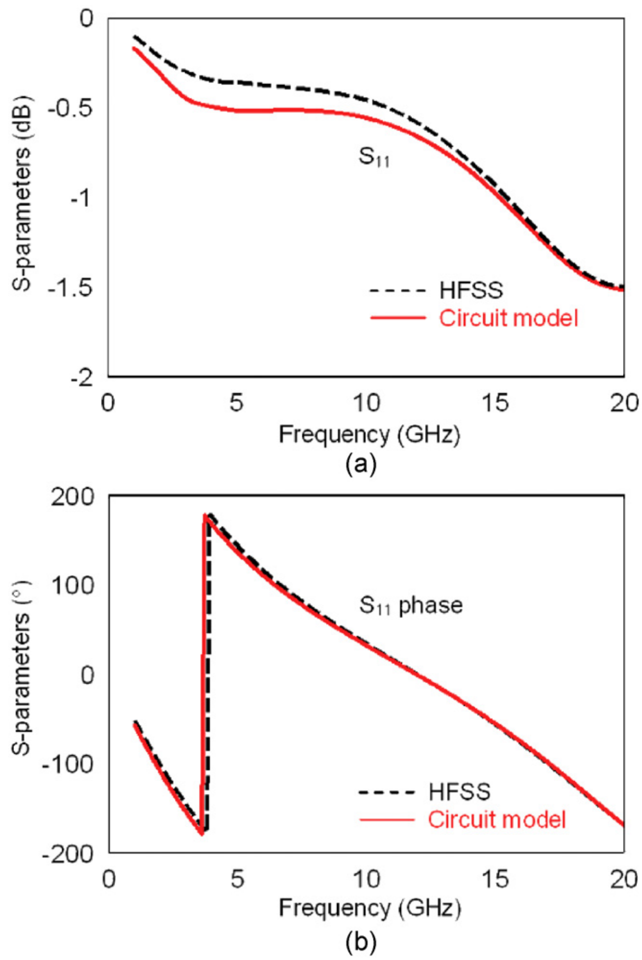

Fig. 4. The comparison of the full wave EM (HFSS) and the cascaded circuit model simulations of a single MEMS stub with 5 MEMS switches where the fourth MEMS switch is in down state: (a) S_{11} magnitude and (b) S_{11} phase.

processing power and memory limitations. Moreover, such a simulation will not give a complete insight. However, as confronted in [14], accuracy of the simulations obtained by cascading the circuit models might be questioned. In this paper, this point is elaborated, and it is shown that careful modeling yields sufficiently good agreement. As a case study, a stub with five MEMS switches, where the fourth MEMS switch is in down-state, is examined. The comparison given in Fig. 4 shows that both techniques are in agreement, especially in higher frequency band including the center frequency of the design.

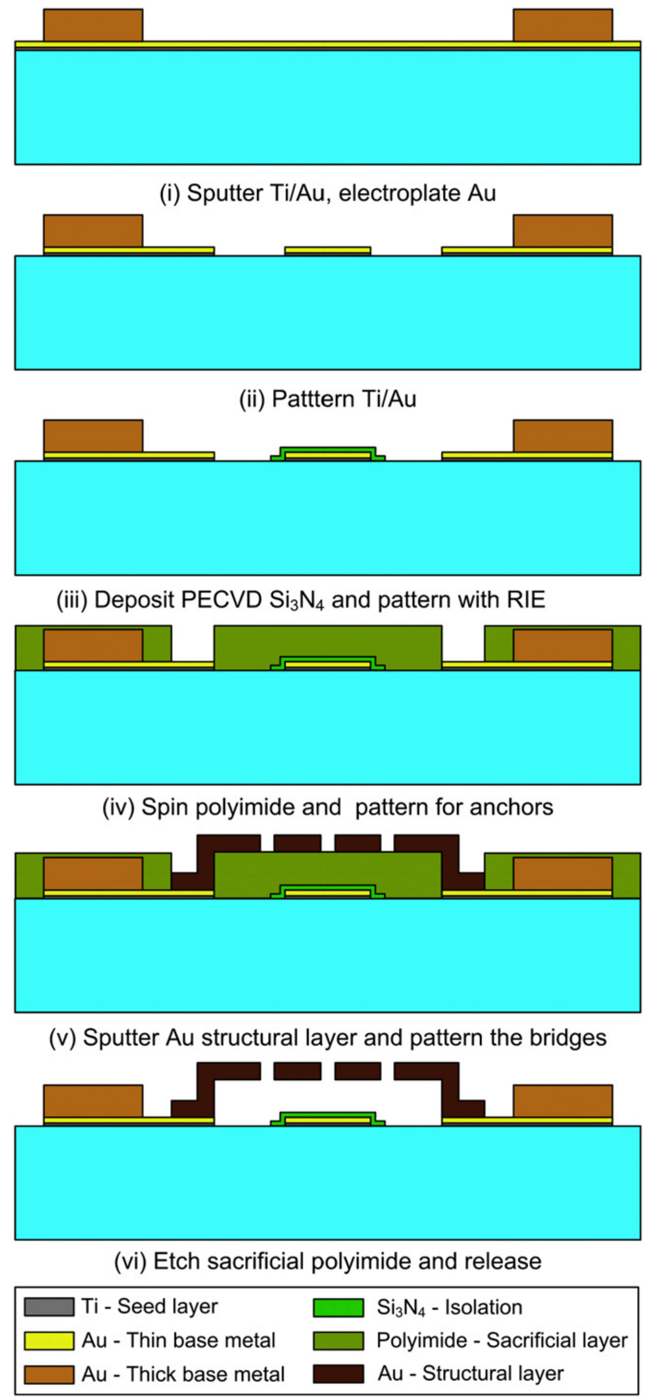

Fig. 5. The process flow of the METU RF MEMS process.

4. Fabrication

The fabrication of the hybrid impedance tuner is composed of two parts, which are the MEMS fabrication and mounting the SMT resistors. The MEMS impedance tuner is first fabricated using an in-house surface micromachining process, which is composed of three metal layers, a sacrificial layer, and a dielectric layer. The process is implemented on Pyrex 7740 glass substrates, which have relative permittivity of $\varepsilon_r = 4.6$ and loss tangent of tan $\delta = 0.005$. Fig. 5 summarizes the process flow. This process starts with 200/2000 Å-thick Ti/Au sputtering, which is the seed layer for gold electroplating. This layer is also the first metal layer for both RF and DC lines. A 2 μm−thick gold layer is electroplated on top for thick CPW lines (Mask 1). The remaining Ti/Au seed layer is wet-etched (Mask 2). A 3000 Å-thick Si_3N_4 layer is deposited as the DC isolation layer using plasma enhanced chemical vapor deposition (PECVD) and patterned by reactive ion etching (RIE) (Mask 3). The next step is the spincoating and patterning of the 2 μm−thick sacrificial polyimide layer (Mask 4). Then, a 1.2 μm−thick gold layer is sputter-deposited and patterned as the structural layer for the suspended MEMS bridges (Mask 5). The sacrificial layer is wet-etched and the MEMS structures are released in supercritical point dryer.

After the MEMS fabrication is completed, the 0603 package 100 kΩ SMT resistors are mounted on the MEMS tuner by nonconductive epoxy, and the connections of the resistors are made by means of conductive epoxy. This connection method

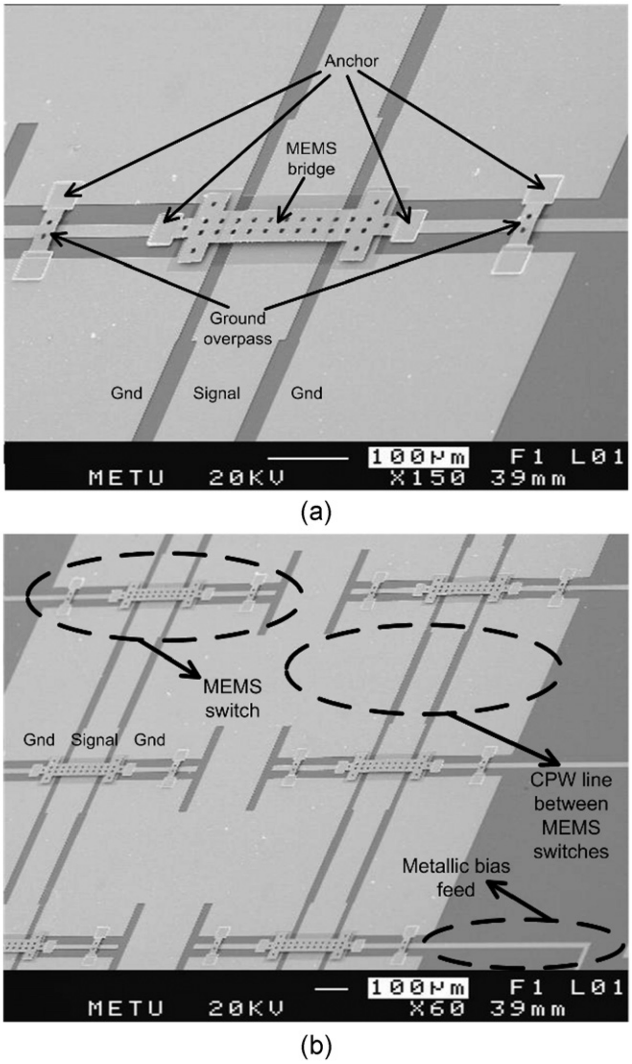

Fig. 6. The SEM pictures of (a) the fabricated MEMS switch (b) the fabricated MEMS impedance matching network – close view to one of the stubs.

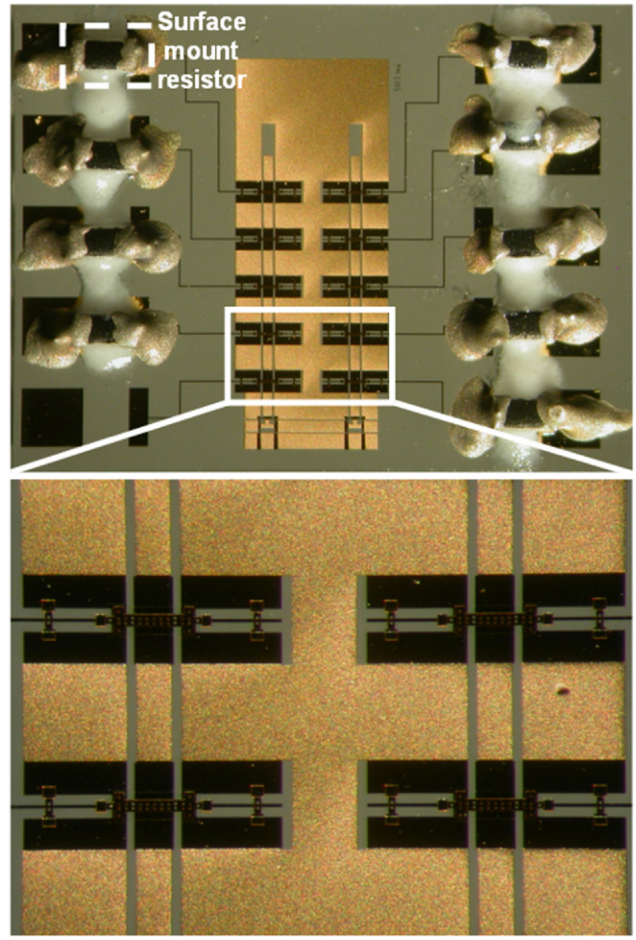

Fig. 7. The photograph of the fabricated MEMS impedance tuner with external resistors mounted.

eliminated the necessity of additional wire bonds to a PCB with a resistor array. Fig. 6 shows the SEM pictures of the fabricated MEMS switch and the impedance tuner. Fig. 7 presents the photograph of the fabricated hybrid impedance tuner.

5. Measurement results

The fabricated MEMS switch and the hybrid impedance tuner are measured using Agilent 8720D vector network analyzer and Cascade Summit 9000 manual probe station in 1–20 GHz frequency band with SOLT calibration.

5.1. MEMS switch measurements

The circuit model parameters of the fabricated MEMS switch are extracted from the *S*-parameter measurements. The extracted parameters are given in Table 1 compared with the design values. The extracted parameters are all close to the design values except the up-state capacitances and the losses of the CPW lines. The up-state capacitances are decreased due to the increase in the MEMS bridge height, which is verified by optical profiler measurements. The loss values, α and $\alpha_{1,2}$, are extracted as 1.4 and 2.2 dB/cm, respectively, which is due to the decrease in the conductivity of gold in the first metal layer and increase in the loss tangent of the Pyrex wafers. More details are given in Section 5.3.

5.2. SMT-RF MEMS hybrid impedance tuner measurements

The *S*-parameters of the hybrid impedance tuner are measured in 1–20 GHz band for 5×5 switch combinations. RF probes obstructed landing the DC probes on the first switches on each stub; therefore, these switches are kept in upstate for all switch combinations.

Fig. 8 shows the measured *S*-parameters of the hybrid tuner for some sample switch combinations compared with the simulations. The connection of the SMT resistors also requires additional components in the circuit model as shown in Fig. 9. In this figure, L_{bias} is used to model the thin metallic connection from the end of the CPW grounds to the pad of the resistor. R_{res} and C_{res} are associated with the SMT resistor, where R_{res} is the value of the resistor itself and C_{res} is the stray capacitance between the pads of the resistor. The series inductance, which also exists in the generic model of the surface mount resistor, does not significantly affect the performance; and hence, it is ignored. C_{end} is the fringe capacitance at the open end. The values of the additional parameters of the modified circuit model are given in Table 3.

R_{res} in Table 3 is the value of the SMT resistor, and C_{res} is the stray capacitance of a standard 0603 package. C_{end} is extracted from the HFSS simulations, and L_{bias} is found by curve fitting. The extracted value of the L_{bias} models a 1000 μm–long and 20 μm–wide line, and its value is 830 pH. This value is physically

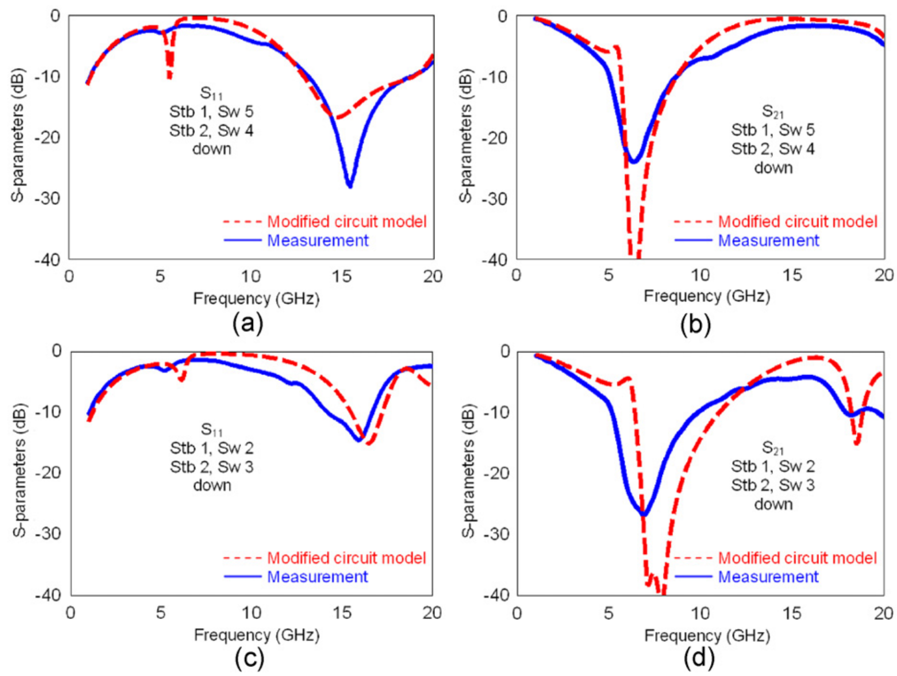

Fig. 8. The measured *S*-parameters of the fabricated modified MEMS impedance tuner for some sample states compared with the simulations.

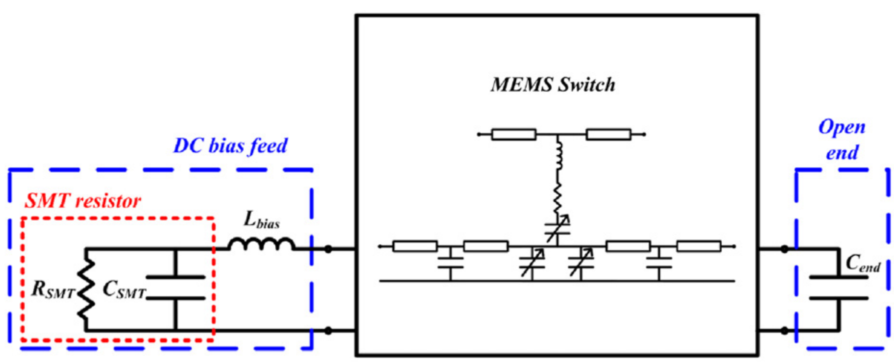

Fig. 9. The modified circuit model of the MEMS switch of the MEMS impedance tuner.

Table 3
The values of the parameters in the modified circuit model of the fabricated MEMS switch.

Bias parameters	Values
C_{end} (pF)	0.01
L_{bias} (pH)	830
C_{res} (fF)	60
R_{res} (Ω)	100 k

reasonable, and it should be mentioned here that the value of L_{bias} is an average value since the lines connecting the resistors to the MEMS switches are different in length for all switches. Remaining parameters are kept the same as given in Tables 1 and 2. All of these components as well as the components added to the conventional *CLR* circuit model are extremely important for estimating the performance of the hybrid impedance tuner.

During the impedance mapping on the Smith Chart, the input impedance of the hybrid tuner is extracted from *S*-parameter measurements. Fig. 10(a) compares the measured impedance distribution with the circuit model simulations for all 25 design points. There are discrepancies between some of the simulated and measured points; because the input impedance is affected from the variations in L_{bias} and C_{res}. It should be noted here that although the same L_{bias} value is used for all switches, it is an average best fit value. The exact values of L_{bias} might change since the length of the thin metal line between the switches and resistors are different for all switches (Fig. 7). The situation is almost the same for C_{res} because the conductive epoxy that is used to connect the resistors can easily affects the stray capacitance. C_{res} value for only 1 out of 10 switches is extracted as 20% more than what is given in Table 3. In any case, the impedance coverage obtained shows that the modeling is achieved for fixed values of L_{bias} and C_{res}, and the values of these components can be extracted successfully using this model.

Other than the above proposed operation of the hybrid tuner, it can be operated in a different way in which MEMS switches are used as tunable capacitors with two digital states. With this consideration, more than one switch on each stub can be actuated at a time, which results with 1024 (2^{10}) impedance states. Since this model almost fits the measurements in 25-state case, it is expected to work for all possible states. In this mode, the hybrid

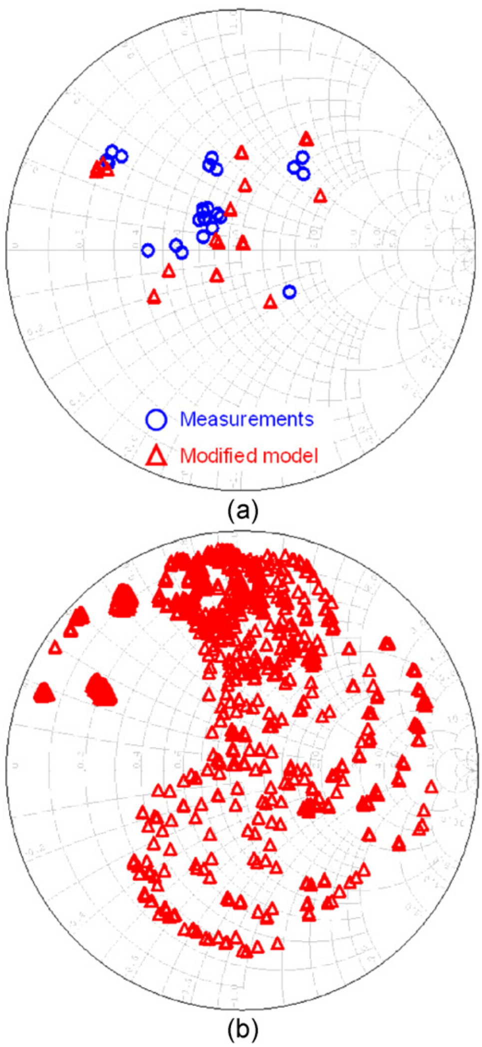

Fig. 10. (a) The comparison of measurements with the simulations of the MEMS impedance tuner at 18 GHz. (b) The simulated Smith Chart distribution all possible states of the designed MEMS impedance tuner at 18 GHz.

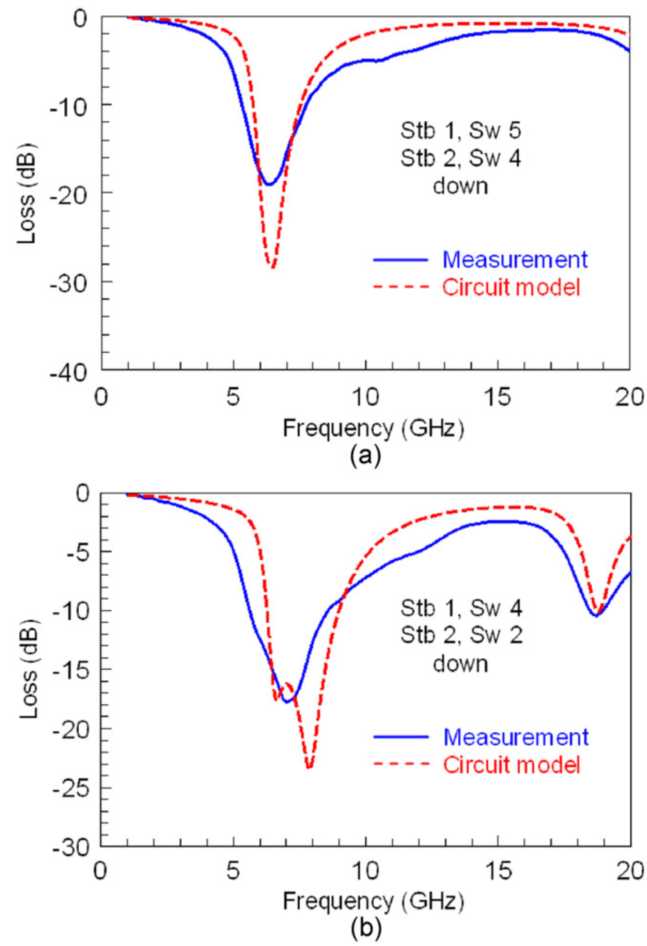

Fig. 11. The measured loss performance of the tuner compared with the simulations.

tuner has an impedance range of 1.4–393 Ω in the real and −210 to 220 Ω in the imaginary parts providing a maximum VSWR of 40 at 18 GHz. The simulated Smith Chart coverage of these states can be seen in Fig. 10(b). The simulated coverage also shows that the hybrid design, which includes the effects of the parasitics, is successful, and it is possible to obtain a wide impedance coverage impedance tuner with this hybrid topology.

5.3. *The loss of the SMT-RF MEMS hybrid MEMS impedance tuner*

The loss of the hybrid tuner is effective on its performance since the losses decrease the VSWR level that can be obtained from the circuit, especially when the VSWR level is high. Moreover, the hybrid tuner cannot make the expected impedance transformation properly if the losses increase significantly.

$$Loss = |S_{21}|^2/(1\text{-}|S_{11}|^2) \quad (1)$$

The loss of a two-port network can be calculated using Eq. (1), and the loss of the hybrid tuner can be easily extracted from the measurements using this equation. The loss performance of the hybrid tuner is given in Fig. 11 for some sample states. The peaks in the loss performance of the hybrid tuner are because of the natural resonances, which occur due to the multiple reflections within the circuit. The average measured loss of all states is around −4.5 dB at 18 GHz, which stems from the resonances that occur around 18 GHz in the loss performance of some states. It is observed that the loss is originating from the CPW line losses, and the bias resistors are almost ineffective on the loss performance.

The increase in the average measured loss is due to the changes in the material properties. The measured conductivity of the gold first metal layer is 1.5×10^7 S/m, where it was assumed to be 4.1×10^7 S/m in the simulations; and the measured loss tangent of the Pyrex wafers is 0.015, where it is reported as 0.005 in the literature. These unexpected changes cause the CPW line losses to increase drastically, which is the dominant reason of the losses of the hybrid tuner. Table 4 gives the measured losses of the CPW lines compared with the ones used in the hybrid tuner design.

It should be noted here that this design is a demonstrator for the modeling of hybrid usage of MEMS and SMT components; and hence, the loss was not taken as a major design concern. However, although the measured CPW losses are higher than the calculated values, it is also shown in this work that the losses can be reduced *below* the designed level. For this purpose, CPW lines that are used in the hybrid tuner design have been fabricated again on quartz substrate (tan $\delta = 0.001$) using an optimized first metal layer deposition process. The optimized first metal layer deposition results with a measured conductivity of 3×10^7 S/m. The measured losses of the CPW lines that are fabricated using this process on quartz substrate (Table 4) are much lower than that of the CPW lines used in the hybrid tuner design. If the optimized CPW lines area used in the hybrid tuner design, the average

Table 4
The parameters of the CPW lines used in the tuner design.

CPW line	Width (μm)	Gap (μm)	Calculated loss (dB/m) (Glass)	Measured loss (dB/m) (Glass)	Measured loss (dB/m) (Quartz)
Line used in the switches	160	22	86	141	70
Line used between the switches	138	35	70	120	55
Interconnection line	178	19	91	150	75
Bias line	18	35	137	214	118

measured loss of the hybrid tuner reduces to around -1.5 dB, which is much lower than the average measured loss of the hybrid tuner. The measurement results of the modified CPW line show the loss performance of the hybrid tuner can be improved easily to acceptable levels.

6. Conclusion

A reconfigurable double stub impedance tuner, which is composed of SMT and RF MEMS components, is presented as a demonstrator of the hybrid usage of MEMS and SMT technologies. The double stub hybrid impedance tuner structure was selected on purpose since it inherently includes a high number of MEMS switches, each of which requires a separate biasing resistor. In this way, the parasitics brought by all of these components as well as those brought by the connections are emphasized. The fabrication of the hybrid tuner is made in two stages, which combine an in-house five-mask surface micromachining process and a mounting process for SMT resistors. The measurements are then performed in 1–20 GHz band at 25 different switch combinations covering the 18 GHz center frequency of the design.

Based on the measurement results, a model is constructed considering each and every part of the complex hybrid structure including the individual MEMS switches, SMT resistors, and all the connections between these components. By this model, it is demonstrated that the response of a complex hybrid structure can be determined by use of individual models for the constituent components. This approach yields consistent results with full-wave electromagnetic simulations and measurements.

It can be concluded here that MEMS and SMT components can be used in a hybrid circuit and the performance of such a hybrid system with various causes of parasitics can be predetermined with the systematic modeling approach proposed in this paper. It is also shown that discrete resistors can be used in the absence of any in-process resistive layers that are crucial for the MEMS impedance tuners.

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