A Low-Cost 128 × 128 Uncooled Infrared Detector Array in CMOS Process

Selim Eminoglu, *Member, IEEE*, Mahmud Yusuf Tanrikulu, *Member, IEEE*, and Tayfun Akin, *Member, IEEE*

***Abstract*—This paper discusses the implementation of a low-cost 128 × 128 uncooled infrared microbolometer detector array together with its integrated readout circuit (ROC) using a standard 0.35 μm n-well CMOS and post-CMOS MEMS processes. The detector array can be created with simple bulk-micromachining processes after the CMOS fabrication, without the need for any complicated lithography or deposition steps. The array detectors are based on suspended p^+-active/n-well diode microbolometers with a pixel size of 40 μm × 40 μm and a fill factor of 44%. The p^+-active/n-well diode detector has a measured dc responsivity ($\Re$) of 4970 V/W and a thermal time constant of 36 ms at 50 mtorr vacuum level. The total measured rms noise of the diode type detector is 0.69 μV for an 8 kHz bandwidth, resulting in a detectivity (D^*) of 9.7×10^8 cm · $Hz^{1/2}$/W. The array is scanned by an integrated 32-channel parallel ROC including low-noise differential preamplifiers with an electrical bandwidth of 8 kHz. The 128 × 128 focal plane array (FPA) has one row of infrared-blind reference detectors that reduces the effect of FPA fixed pattern noise and variations in the operating temperature relaxing the requirements for the temperature stabilization. Including the noise of the reference and array detectors together with the ROC noise, the fabricated 128 × 128 FPA has an expected noise equivalent temperature difference (NETD) value of 1 K for $f/1$ optics at 30 frames/s (fps) scanning rate. This NETD value can be decreased to 350 mK by improving the post-CMOS fabrication steps and increasing the number of readout channels. [2007-0157]**

***Index Terms*—CMOS infrared detector, CMOS micromachined sensor, low-cost infrared detector, microbolometer, microbolometer readout circuit, uncooled infrared detector.**

I. Introduction

UNCOOLED infrared detectors have recently gained wide attention for infrared imaging applications, due to their advantages, such as low cost, low weight, low power, wide spectral response, and long-term operation compared to those of photon detectors. Uncooled technology has great potential for use in various civilian applications, like driver's night vision enhancement, fire detection, security systems, and automotive safety systems. A worldwide effort is still continuing to implement very large format arrays at low cost. For this, many researchers are trying to integrate uncooled infrared detectors with readout electronics monolithically with a CMOS process. The compatibility of the detectors with CMOS technology, and therefore, monolithic CMOS integration, is one of the main issues for achieving low-cost detectors.

One of the most famous approaches for uncooled infrared imaging is to implement microbolometers using surface micromachined bridges on CMOS processed wafers, where infrared radiation increases the temperature of a material on the thermally isolated and suspended bridge, causing a change in its resistance [1]–[17]. There are efforts to implement microbolometers using many different materials, such as vanadium oxide (VO_x) [1], [2], [9]–[15], amorphous silicon (a-Si) [3], [16], [17], polycrystalline silicon−germanium (poly SiGe) [4], yttrium barium copper oxide (YBaCuO) [5], [6], and metal films [7], [8]. Outstanding performance has been demonstrated with surface micromachined microbolometers having focal plane array (FPA) sizes as large as 640 × 480 and pixel sizes ranging from 50 μm down to 17 μm, especially using VO_x and a-Si, with performances close to those of cooled infrared detectors at much lower cost [9]–[17]. However, these detectors are mainly developed for military application, and their costs are not as low as the required level for many commercial applications, as all of the surface micromachined resistive bolometers require post-CMOS material deposition and etching steps, as well as a number of high-precision lithography steps, limiting their cost reduction. In addition, some of these approaches are not compatible with CMOS process lines and require dedicated fabrication facilities.

Another important microbolometer approach is to use silicon p-n diodes as the temperature sensitive element in microbolometer arrays [18]–[20]. Array pixels are based on suspended multiple series diodes fabricated on SOI CMOS wafers, and successful implementation of 320 × 240 FPAs with 40 μm pixel pitch and 640 × 480 FPAs with 25 μm pixel pitch have been reported [18]–[20]. Although this approach provides very uniform arrays with very good potential for low-cost high performance uncooled detectors, its fabrication is based on a dedicated in-house SOI CMOS process, where intra-CMOS MEMS process steps are included. Since these detectors cannot be implemented in a standard CMOS or SOI CMOS process, it would be difficult to reduce their costs down to limits that very low-cost applications require.

A different microbolometer approach is recently proposed for very low-cost applications, where the detector material is obtained with very thin Si/SiGe single crystal multilayers [21].

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As this material requires high temperature epitaxial growth, it cannot be grown on CMOS readout electronics. Instead, the material is grown on a separate substrate, and then, it is transferred on top of the CMOS readout electronics using a 3-D bolometer integration process [22]–[24]. Although this approach aims at low cost detector arrays, it requires a rather complicated process with unconventional production methods, where yield might be a problem.

One of CMOS based infrared imager approaches is to use thermopile arrays implemented with front or back-side bulk-micromachining of CMOS fabricated wafers [25], [26]. However, thermopile arrays have low responsivity values (2–15 V/W) and large pixel pitch (100–250 μm), limiting their use for large detector arrays. In addition, these detectors also require extra processing steps to form electroplated gold lines for thermal isolation between the pixels [25] or special processing steps that results in a custom-made CMOS process to achieve the required structure [26].

Another unconventional and potentially low-cost approach is to implement FPAs using thermally tunable thin film filter membrane pixels [27]–[29]. Each of these pixels acts as a wavelength translator, converting far infrared radiation signals into near infrared signals, which are optically detected by off-the-shelf charge coupled device (CCD) or CMOS cameras. This optical readout approach introduces some unique difficulties such as readout complexity, shot noise, and vibration and thermomechanical noise. In addition to these unique difficulties, this approach has other challenges such as nonuniformity, sensitivity to critical film properties, and sensitivity to ambient temperature, limiting its low-cost target. There are still efforts to overcome these difficulties and fabricate low-cost infrared imagers with high performance [29].

For ultra low-cost applications, the best approach would be to implement the detector arrays together with their readout circuitry fully on a standard CMOS or SOI-CMOS process, using some simple post-CMOS etching steps where neither any critical lithography nor any detector material deposition steps are needed. We have previously demonstrated the implementation of such low-cost uncooled microbolometer FPAs with 16 × 16 array format, where the n-well layer in a standard 0.8 μm CMOS process is used as the active detector material [30], [31]. The pixels in these prototype FPAs have a size of 80 μm × 80 μm with a fill factor of 13%, which is low due to the limitations of silicon bulk-micromachining used in detector fabrication. We have also reported fabrication of a new low-cost small pixel size detector structure, where the pixel is achieved with a new post-CMOS processing approach on dies fabricated using a standard 0.35 μm CMOS process [32], [33] along with its first array implementation [34]. This paper reports the implementation of a larger FPA with 128 × 128 pixels based on this detector structure along with improved readout circuitry [35]. The pixels used in the FPA have a size of 40 μm × 40 μm, while having an increased fill factor of 44%. Each detector in the FPA is implemented with a suspended p^+-active/n-well diode, which provides very low noise when biased at low current. This infrared FPA fabrication approach is very simple and suitable for ultra low-cost infrared imaging applications.

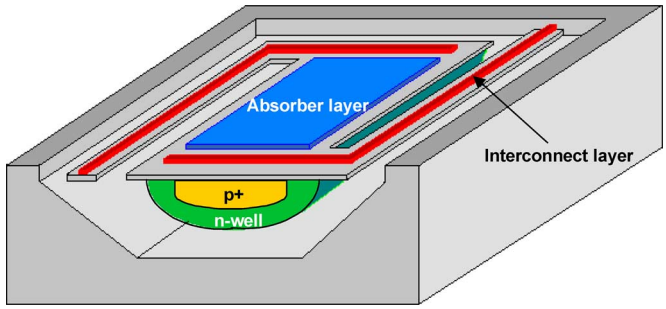


Fig. 1. Perspective view of the p^+/n-well active diode microbolometer that can be obtained in a standard n-well CMOS process.

II. Pixel Structure and Implementation

Fig. 1 shows a perspective view of the p^+-active/n-well diode microbolometer that can be obtained in a standard n-well CMOS process after post-CMOS MEMS processes [33]. Infrared radiation heats the absorbing layer on the thermally isolated n-well, increasing its temperature, which in turn results in a change in the diode voltage related to its temperature coefficient. Bulk silicon under the n-well is etched away to reduce thermal conductance and to increase responsivity of the detector. To obtain high thermal isolation, the interconnect material on support arms are implemented using polysilicon. This thermally isolated suspended structure is obtained by front-side bulk-etching of fabricated CMOS dies, where the electrochemical etch-stop technique is used to prevent the etching of the n-well [36], [37].

The pixel size and fill factor are determined by process limitations, such as the minimum interconnect width and openings between the arms that allow silicon to be exposed to the solution during etching. To improve the fill factor, etch openings are drawn at their minimum possible dimensions, and no initial oxide openings are created on the CMOS fabricated FPAs. The required etch openings are created in an optimized selective dry etch process using a mixture of CHF_3 and O_2 gases, where CMOS metal layers are used as protection masks [34], [38]. After the necessary openings are created on the surface to reach the silicon substrate, the silicon underneath the pixel is removed in an anisotropic silicon etchant, Tetra-Methyl Ammonium Hydroxide (TMAH), while the electrochemical etch-stop process is used to prevent etching of the n-well layer. Fig. 2 shows the post-CMOS fabrication steps and the cross-sections of the pixel structure after (a) CMOS fabrication, (b) dry-etch, and (c) anisotropic silicon etch process in TMAH. At the beginning, the surface of the pixel is covered with oxide. After dry-etching, all the oxide not protected by metal layers is etched down to the silicon substrate, and the protected regions are stopped at particular metallization levels. The silicon underneath the pixel is removed by using a front-side bulk silicon micromachining technique. Finally, the metal mask layers are removed by a simple metal etch process [33].

This approach has a number of advantages. First of all, it does not require any critical lithography step after the CMOS process, reducing the cost of the process. In addition, the gaps between the arms can be reduced as the CMOS technology allows, making it possible to reduce the pixel size while

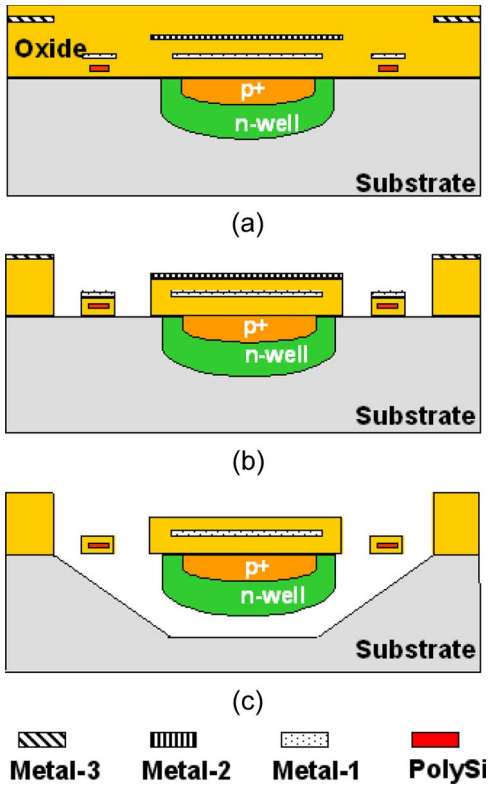


Fig. 2. Post-CMOS fabrication steps and the cross section of the diode pixel structure (a) after CMOS process, (b) after dry etch, and (c) anisotropic silicon etch [33].

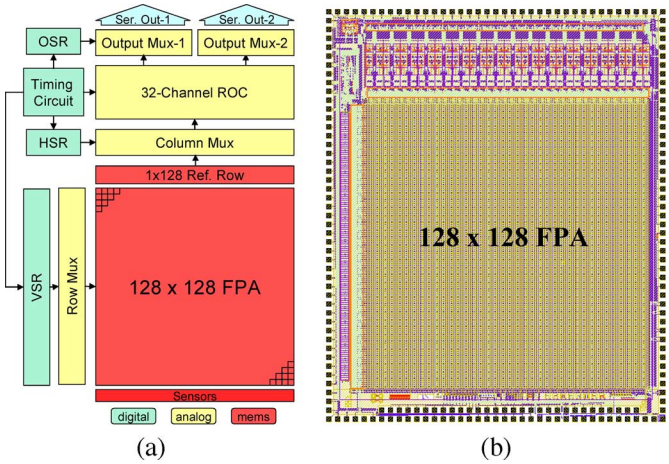


Fig. 3. (a) Block diagram and (b) layout of the 128 × 128 uncooled infrared imager chip. The chip measures 6.5 mm × 7.9 mm in a standard 0.35 μm CMOS process.

increasing the fill factor. Also, there is no need for any complicated post-CMOS deposition or surface micromachining process steps that increase the processing cost and that decreases the yield. Therefore, the detector cost is expected to be very close to the cost of the CMOS chip.

III. FPA Architecture

Fig. 3 shows the block diagram and the layout of the fabricated 128 × 128 uncooled infrared FPA. The array and reference row pixels are addressed by row and column multiplexers (Row and Column Mux) controlled by vertical and horizontal shift register (VSR and HSR) blocks. The array pixels are read out differentially with respect to reference pixels through a 32-channel low-noise readout circuit (ROC) composed of differential transconductance amplifiers, switched capacitor integrators, and sample-and-hold circuits at 30 frames/s (fps) with an electrical bandwidth of 8 kHz. Final analog output is multiplexed through two serial outputs (Ser Out-1, Ser Out-2) controlled by output shift register (OSR) at a rate of 250 K samples/s. All the blocks are controlled by an on-chip timing circuit. There are on-chip temperature sensors to monitor the die temperature, and on-chip etching circuitry to properly bias the pixels during the silicon etching process. The chip measures 6.5 mm × 7.9 mm in a standard 0.35 μm CMOS process.

Pixels in the array are read out with respect to on-chip infrared-blind reference detectors to minimize the effect of ambient temperature variations. Fig. 4 shows the simplified schematics of the 128 × 128 microbolometer array together with the reference detectors. Gray lines show the current flow through the array and reference pixels when the row switch $\langle 0 \rangle$ is closed. $V_{\mathrm{r\_pix}}$ and $V_{\mathrm{r\_ref}}$ are reference voltages for the array and reference pixels, R_x and R_y are horizontal and vertical routing resistance values per pixel, and R_z is the routing resistance per row below a selected row in the vertical routing structure on the left of the array for both array and reference pixels. Reference pixels have effectively N times wider vertical routing lines above the selected row in the routing structure to match the vertical voltage drops on the upper portion of the array. An improvement with respect to the previous array [35] is achieved by using an exact replica of the array row as a reference row of pixels just above the array pixels, and improving the vertical routing structure external to the detector area.

To compensate for the horizontal voltage variation, the reference pixels are placed in a single row above the array pixels. The electrical property of the reference pixels is identical to that of the array pixels, with the only difference being in their thermal conductance values. To reduce any possible self-heating due to excessively fast addressing of these pixels, they are connected with metal interconnects on wider oxide support arms. The corresponding electrical resistance of the reference pixels is matched by using the same interconnect structure outside the pixel area on the substrate. Because of the poor thermal isolation of the reference pixels, they can be considered to be infrared-blind due to their reduced responsivity by about three orders of magnitude. The high thermal-conductance associated with the reference pixels also reduces their thermal time constant to a very low level, and they can respond to the self-heating almost immediately. However, due to the increased thermal conductance value, the self-heating of these detectors is not as high as the actual detectors, even if they can reach the steady state very quickly. The disadvantage of having a short thermal time constant for the reference pixels is that they cannot be used to compensate for the self-heating occurring unavoidably for the array pixels. However, this can be solved by adjusting the current level just prior to the integration in the circuit level [39].

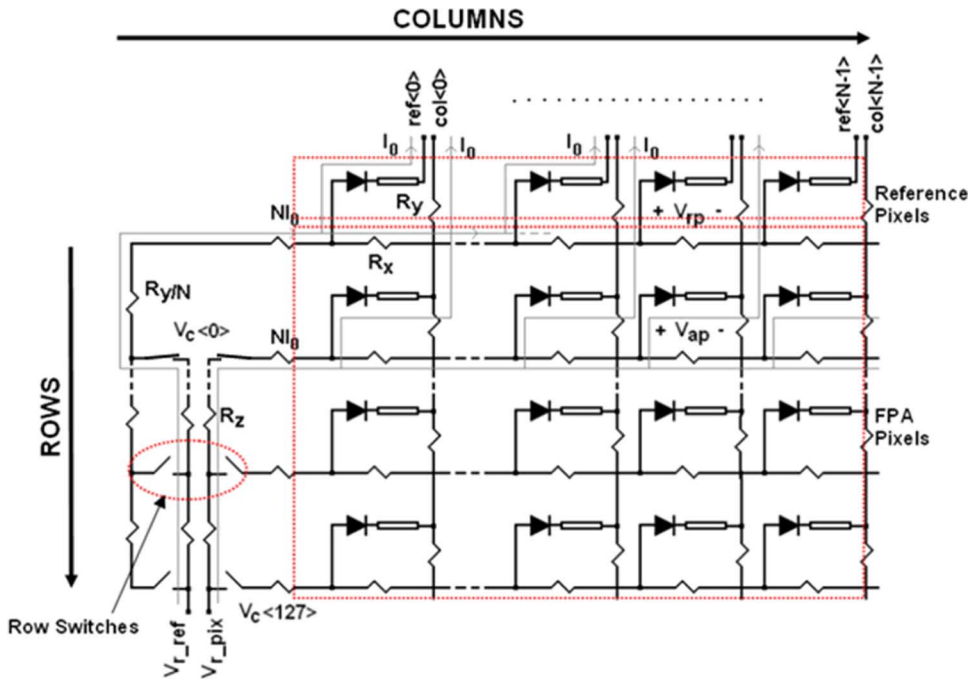


Fig. 4. Simplified schematics of the 128 × 128 array with the improved array structure. Gray lines show the current flow through the array and reference pixels when the row switch ⟨0⟩ is closed.

To compensate for the vertical voltage variations, the metal lines in the external vertical routing structure are implemented in such a way that the vertical voltage drop measured from a selected row bias voltage is the same both for the reference and array pixels, which is cancelled by a differential ROC. Although it is also possible to make the FPA insensitive to vertical pixel selection, the 128 × 128 FPA is designed so that the differential reading is compensated both for the horizontal and vertical voltage variations. The resulting array pixel voltage $(V_{\mathrm{FPA}}(m,n))$ and reference pixel voltage $(V_{\mathrm{REF}}(m,n))$ in the FPA are given as

$$V_{\mathrm{FPA}}(m,n) = V_{\mathrm{row}}(m) - V_{\mathrm{pix}}(m,n) - mI_0R_y - \frac{N}{K}(K-1-p)I_0R_x - KI_0R_x\sum_{k=0}^{c}\left(\frac{N}{K}-k\right) \tag{1}$$

$$V_{\mathrm{REF}}(m,n) = V_{\mathrm{row}}(m) - V_{\mathrm{REF}}(n) - mNI_0\frac{R_y}{N} - \frac{N}{K}(K-1-p)I_0R_x - KI_0R_x\sum_{k=0}^{c}\left(\frac{N}{K}-k\right) \tag{2}$$

where, m and n are the row and column of the pixel, respectively, V_{row} is the bias voltage for the selected row, V_{pix} and V_{REF} are the voltages of the selected array and reference pixels, respectively, I_0 is the pixel bias current, R_x and R_y are horizontal and vertical routing resistance values, respectively, for a single pixel, N is the number of columns and rows in the FPA $(N = 128)$, K is the number of the parallel readout channels $(K = 32)$, p is the position index of the pixel in a selected column group $(0 \le p \le 3)$, c is the position index of the corresponding readout channel $(0 \le c \le 31)$, and $V_{\mathrm{r\_pix}}$ and $V_{\mathrm{r\_ref}}$ are the reference bias voltages of the array rows and reference row, respectively. It should be noted that the total current carried by the external routing structure is the same on the left of the array, and the lower portion of the external routing structure is identical for both array and reference pixels; therefore, voltages after row select switches are identical for both array and reference pixels, denoted by $V_{\mathrm{row}}(m)$. However, the current distribution is different in the upper section above the select switch for a given row, since, the total current inside the array is divided into as many parallel paths as the number of parallel readout channels. Corresponding voltage drop in the upper vertical section is given by the third term in the above equations. To match the upper vertical voltage drop in the array and external vertical routing structure, as many multiple parallel paths as the number of routing channels are added to the vertical routing structure, so that the product of the total current and total resistance is kept the same both for the array and reference pixels. The fourth and fifth terms in the above equations give the horizontal voltage drop in the array and reference pixels, respectively, in the nth column, which corresponds to cth readout channel and pth pixel in the given channel. Since the pixel row structure for array and reference pixels are made identical in the design, corresponding terms are the same for array and reference pixels. Assuming that the line resistance values match well between the array routing lines and reference lines, the differential FPA output voltage $(\Delta V(m,n))$ is given as

$$\Delta V(m,n) = V_{\mathrm{REF}}(m,n) - V_{\mathrm{FPA}}(m,n) = V_{\mathrm{pix}}(m,n) - V_{\mathrm{REF}}(n). \tag{3}$$

As can be seen, the differential FPA output voltage does not include any voltage drop term related to the pixel position in the array. This result verifies that the differential FPA output voltage is fully compensated in terms of resistive voltage drops in the array. In addition to that, the differential voltage also helps compensate for the effect of operating temperature variations, relaxing the requirements for the temperature stabilization, and hence, making low-power operation possible. It should be noted that the 128×128 reference voltages are generated by a 1×128 reference row and a dummy routing structure outside the pixel area. The only disadvantage of the differential structure is that it introduces extra noise coming from the reference pixels and extra circuitry in the differential readout. However, considering its inherent nonuniformity (fixed-pattern noise) correction capability, it is still preferred to the single-ended structure. In the single-ended case, external compensation would be required, which would also increase the input noise level even at the expense of increased circuit complexity.

IV. Fabrication and Test Results

The FPA architecture is fabricated in a standard 0.35 μm CMOS process of AMS AG. The fabricated CMOS array is post-processed with the approach described in Section II. It should be noted here that the bonding pads in the chip are protected with photoresist by a noncritical photolithography before the dry-etching process. This photoresist is stripped away after the metal mask layer is etched with a simple metal etch process. During the post-processing of the array, the metal etching is done before the TMAH etching of the silicon underneath the pixels, as opposed to the metal etching of single pixels. Fig. 5 shows one of the $40\ \mu\text{m} \times 40\ \mu\text{m}$ p^+-active/n-well diode microbolometer pixels of the FPA chip during the fabrication process. Fig. 5(a) shows an SEM photograph of the pixel after CMOS fabrication and before post-CMOS etchings, where all of the CMOS layers exist. Fig. 5(b) shows an SEM photograph of the top view of the pixel after dry etching with reactive ion etching (RIE). It should be noted here that in the pixel area no additional protection layer is used other than the metal layers of the CMOS process. The only protection layer applied to the chip is in the bonding pad area as mentioned above. There is no need of an extra layer for the protection of the circuit area during the RIE process due to the metal mask. The TMAH etch process also does not affect the CMOS circuit since it is protected by one of the CMOS oxide layers. Fig. 5(c) shows an SEM photograph of the cross section of the pixel after dry etching with RIE, where openings less than 1 μm are visible, thanks to metal masking layers created during the standard CMOS process. This approach allows increasing the fill factor of the pixel.

Fig. 6(a) shows an SEM photograph of the pixel after anisotropic silicon etching, where one of the pixels is broken to show the unetched $\langle 111 \rangle$ planes of the silicon substrate. The unetched silicon areas serve as the thermal isolation regions between the pixels that are used to minimize thermal crosstalk, eliminating the need for silicon islands or gold stripes between the pixels which have been used in other approaches [25], [40]. The width of these unetched areas should be as small as possible

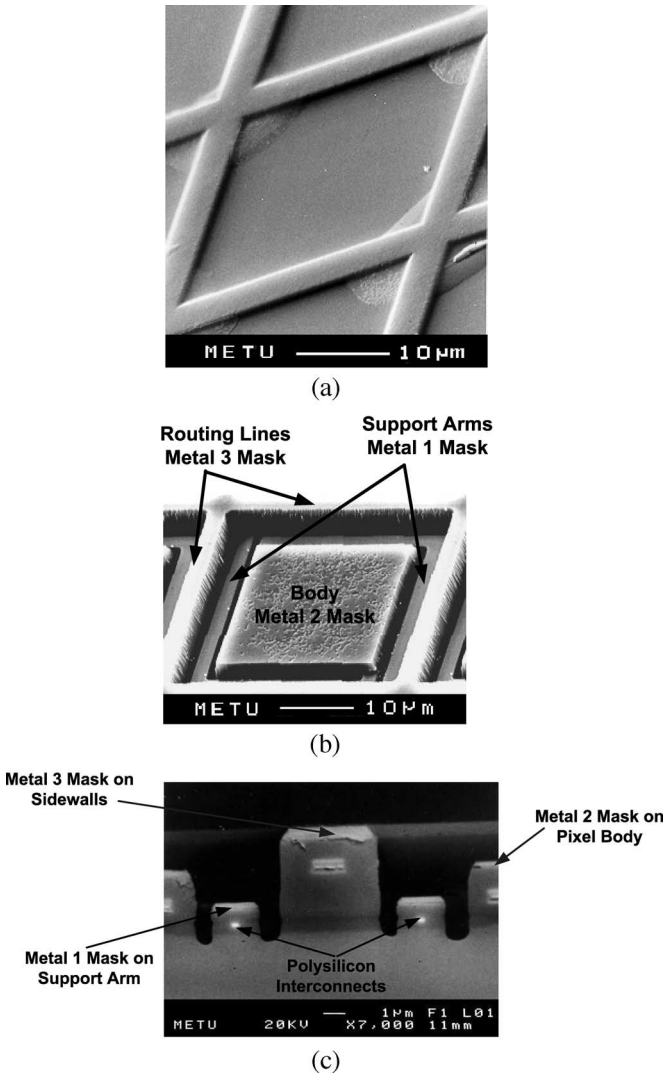
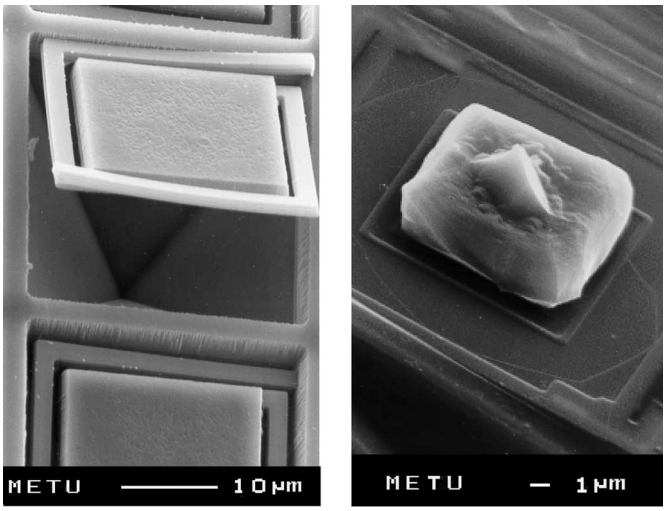


Fig. 5. SEM photographs of one of the $40\ \mu\text{m} \times 40\ \mu\text{m}$ p^+-active/n-well diode microbolometer pixels of the FPA chip during the fabrication process: (a) Pixel after CMOS fabrication and before post-CMOS etchings, where all of the CMOS layers exist, (b) top view of the pixel after dry etching with RIE, and (c) cross section of the pixel after dry etching with RIE, where openings less than 1 μm are visible, thanks to metal masking layers created during the standard CMOS process.

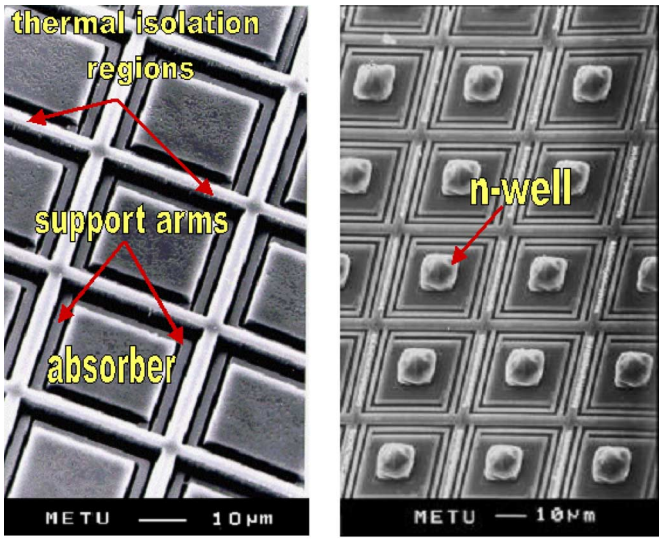
to increase the fill factor, but is limited by the postprocess parameters such as the undercut rate of the anisotropic etchant and the process time. Since the n-wells underneath the pixels cannot be seen from top view, the pixels are taken out by a sticky tape. Fig. 6(b) shows one of the pixels from the bottom view and the n-well underneath the pixel. Fig. 7 shows an SEM photograph of post-processed pixels in the array from (a) top view and (b) bottom view after removing pixels with a sticky tape. To show the pixels of the array intact in the bottom view, the walls of the pixels are etched away by overetching in the TMAH etching step.

A number of electrical and optical tests have been performed to determine the performance parameters of the array pixel and to verify the functionality of the on-chip ROC. Measured performance parameters include temperature coefficient of diode forward voltage, thermal conductance, thermal time constant,



(a) (b)

Fig. 6. SEM photographs of the pixel after anisotropic silicon etching: (a) where one of the pixels is broken to show the unetched ⟨111⟩ planes of the silicon substrate, (b) where one of the pixels is removed with a sticky tape to show its bottom view including the unetched n-well.

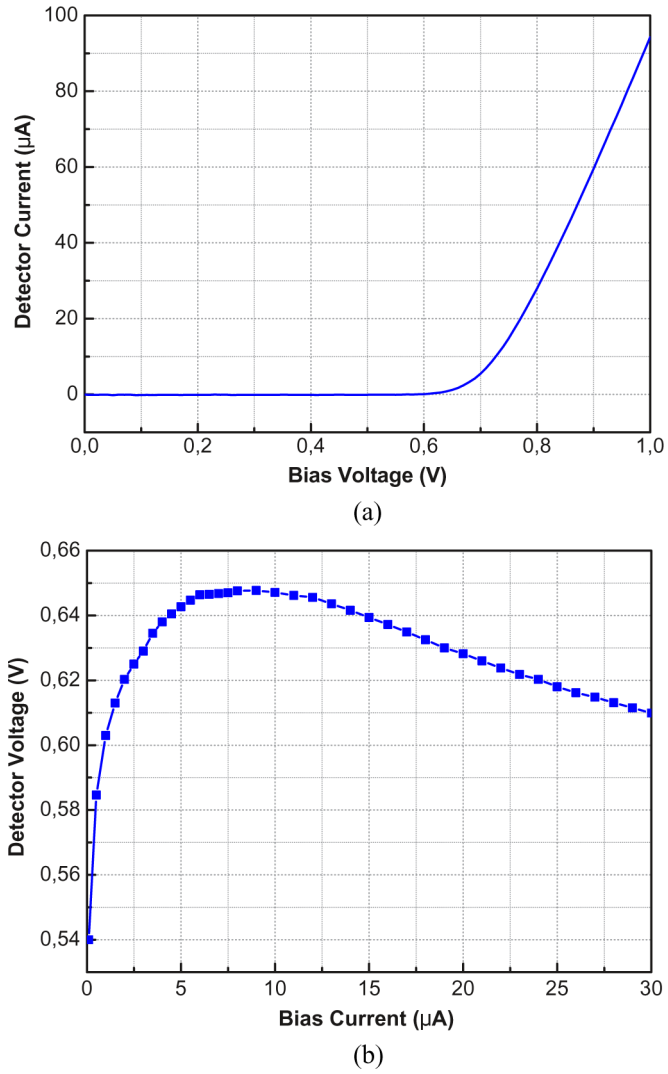


(a) (b)

Fig. 7. SEM photographs of the postprocessed pixels in the array from (a) top view and (b) bottom view after removing pixels with a sticky tape.

responsivity and detectivity of the pixel, as well as nonuniformity of the array pixels and their temperature sensitivities.

The temperature coefficient of the diode pixel is measured as -2 mV/K, and the thermal conductance $(G_{\rm th})$ of the pixel is measured based on the self-heating effect. Thermal conductance and other vacuum tests are performed using a simple in-house built dewar. Fig. 8(a) and (b) shows the measured I–V curves of the detector at room temperature and at pressure levels of 1 atm and 50 mtorr, respectively. When the detector is not in vacuum condition, the applied bias power does not cause any noticeable self-heating effect, and the detector current increases with the increasing detector bias voltage. In Fig. 8(a), the interconnect resistance is extracted as 3 kΩ using the slope of the I–V curve at high bias levels, and this result is very close to the designed value. The I–V measurement in vacuum is



(a)

(b)

Fig. 8. Measured $I-V$ curves of the suspended diode type microbolometer at room temperature and at pressure levels of (a) 1 atm and (b) 50 mtorr, respectively.

performed using a constant current source to avoid thermal runaway due to the negative temperature coefficient of the detector.

At low bias levels, the detector voltage increases with the increasing current level, and self-heating is negligible at these low levels. However, at increased current level, the slope of the V–I curve turns out to be negative, which is due to the fact that the applied bias causes a much larger increase in the detector temperature decreasing the detector voltage despite the expected increase related to the interconnect resistance and the dynamic resistance of the diode. Neglecting the power dissipation along the interconnects, the slope of the $V-I$ curve in Fig. 8(b) is given as

$$V = V_d + IR_{\rm connect} \tag{4}$$

$$\begin{aligned} dV &= \frac{\partial V_d}{\partial I}dI + \frac{\partial V_d}{\partial T}dT + R_{\rm connect}dI + I dR_{\rm connect} \\ &= r_d dI + \frac{\partial V_d}{\partial T}dT + R_{\rm connect}dI + IR_{\rm connect}\frac{\alpha_{\rm connect}}{2}dT \end{aligned} \tag{5}$$

$$dV = (R_{\text{connect}} + r_d)dI + \left(\frac{\partial V_d}{\partial T} + \frac{IR_{\text{connect}}\alpha_{\text{connect}}}{2}\right)dT$$

$$= (R_{\text{connect}} + r_d)dI + \text{TC}_{\text{eff}}dT \tag{6}$$

$$\frac{\partial V_d}{\partial T} = -n\frac{1.21V - V_d/n}{T} \tag{7}$$

$$dT = \frac{dP}{G_{\text{th}}} = \frac{IdV + VdI}{G_{\text{th}}} \tag{8}$$

$$\frac{dV}{dI} = \frac{R_{\text{connect}} + r_d + \text{TC}_{\text{eff}}V/G_{\text{th}}}{1 - \text{TC}_{\text{eff}}I/G_{\text{th}}} \tag{9}$$

where R_{connect} is interconnect resistance, r_d is the small-signal resistance of the diode, TC_{eff} is the effective temperature coefficient of the detector voltage, V is the detector voltage, n is the diode ideality factor extracted as 1.08 for the suspended n-well diodes, G_{th} is thermal conductance, I is detector bias current, α_{connect} is the temperature coefficient of resistance of the interconnect material (0.09%/K), V_d is the diode voltage, and T is detector temperature [18]. By calculating the slope of the measured V–I curve and TC_{eff} at each bias point, G_{th} of the detector is extracted as 1.55×10^{-7} W/K. This G_{th} value is larger than the expected value of 1.2×10^{-7} W/K according to simulations performed using the CoventorWare program. One possible reason for the increase in the G_{th} value is the fact that there remains a thin residual metal layer on the interconnection of the detector after postprocessing steps, and this problem can easily be solved by extending the etching periods during postprocessing steps. In fact, the simulated thermal time constant value is close to the measured value of 36 ms, which was expected to be smaller with increased thermal conductance value. This suggests that the pixel thermal mass is increased due to some extra material left on the pixel. With process optimization, it is possible to decrease the G_{th} down to its simulated value and to decrease the detector thermal mass without much increase in the thermal time constant value. The measured thermal time constant value suggests operating the FPA at around 9 fps for maximum responsivity performance; at 30 fps operation, the responsivity of the FPA decreases.

Fig. 9 shows the measured responsivity of the p^+/n-well active diode type microbolometer detector with respect to infrared modulation frequency from 8.5 to 85 Hz at 80 mtorr vacuum level. The measurement data fit into a single-pole frequency response, and the dc responsivity and the thermal time constant values of the detector are extracted as 4970 V/W and 36 ms, respectively. Measurement setup consists of a light source, a light chopper, a Germanium (Ge) bandpass infrared filter, a pyroelectric reference detector, a lock-in amplifier, and the microbolometer detector in a vacuum chamber. First, the incoming radiation is measured using the reference detector, and later measured using the microbolometer and a lock-in amplifier at different chopping frequencies.

Because of the negative temperature coefficient, self-heating has a negative effect on the dc responsivity of the detector, due to the so-called electrothermal effect observed especially for the continuously biased detectors [41]. When the infrared radiation heats up the detector, there is a decrease in the detector

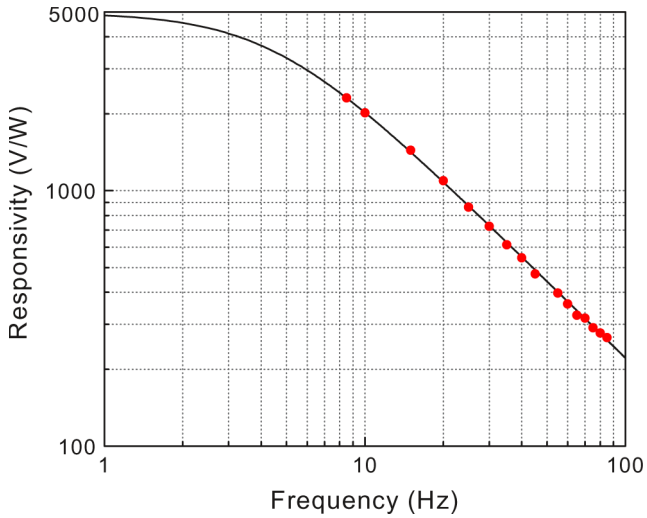


Fig. 9. Measured responsivity of the p^+/n-well active diode type microbolometer detector with respect to infrared modulation frequency from 8.5 to 85 Hz at 80 mtorr vacuum level. The measurement data fits into a single-pole frequency response, and the dc responsivity and the thermal time constant values of the detector are extracted as 4970 V/W and 36 ms, respectively.

voltage related with its negative TC value. Since it is biased by a constant current source, applied electrical power also decreases, which in turn decreases the expected change in the detector temperature due to the reduced self-heating. The dc responsivity of the continuously biased diode type microbolometers ($\Re_{\text{dc\_cont}}$) is given as

$$\Re_{\text{dc\_cont}} = \eta\text{TC}_{\text{eff}}/G_{\text{th\_eff}} \tag{10}$$

$$\Re_{\text{dc\_cont}} = \frac{\eta\text{TC}_{\text{eff}}}{G_{\text{th}}(1 - \text{TC}_{\text{eff}}I/G_{\text{th}})}$$

$$\cong \frac{\eta\text{TC}_{\text{eff}}}{G_{\text{th}}(1 - \text{TC}_{\text{eff}}\Delta T_{\text{self\_heating}}/V)} \tag{11}$$

where η is the absorption coefficient, TC_{eff} is the effective temperature coefficient of the detector, $G_{\text{th\_eff}}$ is the effective thermal conductance value that accounts for the electrothermal feedback effect, I is dc bias current, V is the detector voltage, and $\Delta T_{\text{self\_heating}}$ the temperature rise due to self-heating. For the continuous bias case, $G_{\text{th\_eff}}$ of the detector becomes as large as 1.8×10^{-7} W/K, and using this $G_{\text{th\_eff}}$ value and measured dc responsivity of the detector, absorption coefficient (η) is extracted as 0.45. It should be noted that in the pulsed bias case, $\Delta T_{\text{self\_heating}}$ is negligible; therefore, an improvement in thermal conductance value is expected for the array detectors operating in the pulsed bias mode. In the pulsed bias mode, self-heating will be negligible, and therefore, $G_{\text{th\_eff}}$ of the detector will decrease from 1.8×10^{-7} W/K to its measured physical value of 1.55×10^{-7} W/K, providing an improvement of about 16% in the overall dc responsivity.

Fig. 10 shows the measured noise spectral density of the diode type microbolometer detector. The measurement setup consists of a dynamic signal analyzer (Agilent 35670A), low-noise preamplifier with measured frequency response and noise

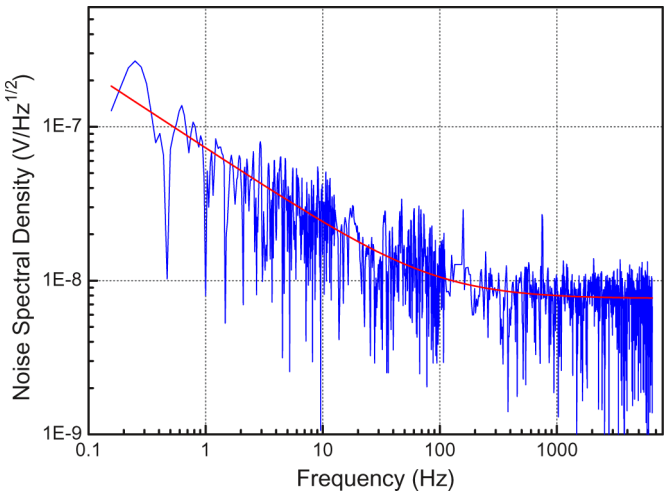


Fig. 10. Measured noise spectral density of the diode type microbolometers. Total rms noise voltage is found as 0.69 μV for 8 kHz bandwidth with a $1/f$ noise corner frequency of 90 Hz.

spectrum, diode type microbolometer detector, faraday cage, and battery-driven power and bias circuitry. The measurement noise spectrum is fitted into an expression with $1/f$ and thermal noise components, from which the corner frequency is determined as 90 Hz. The low corner frequency shows that the $1/f$ noise contribution of the n-well microbolometer is low, which is due to the single crystal nature of the n-well and low $1/f$ noise value at low biasing levels. The measured detector noise is 0.69 μV for the 128 × 128 FPA with an electrical bandwidth of 8 kHz, which is the case when the FPA is scanned at 30 fps resulting in a measured detectivity (D^*) of 9.7×10^8 cm $\cdot$ Hz$^{1/2}$/W. The input referred rms noise of the ROC is measured as 0.76 μV in the same electrical bandwidth.

Based on the measurement results, the fabricated 128 × 128 FPA has an expected noise equivalent temperature difference (NETD) value of 1 K for $f = 1$ optics when scanned at 30 fps. Considering the pulsed bias case and using optimized post-CMOS etching steps, the $G_{\rm th}$ of the pixel can be improved from 1.8×10^{-7} W/K to the simulated value of 1.2×10^{-7} W/K without much changing the thermal time constant, which will decrease the array NETD value below 700 mK. This NETD value can further be decreased by reducing the electrical bandwidth with the help of the increased number of parallel readout channels. In the limiting case, the bandwidth can be decreased down to 2 kHz by increasing the number of parallel readout channels to 128 at the expense of increased chip area, which will result in a NETD value below 350 mK.

Fig. 11(a) shows the measured voltages of the array pixels in the 128 × 128 FPA, and Fig. 11(b) shows the measured reference pixel voltages at each position of the row select switch. These measurements are done by setting the gain of the analog readout chain from the pixel to the output to unity, allowing direct measurement of array and reference pixel voltages. In these figures, voltage variation along the rows is much higher as compared to the voltage variation along the columns. This is due to the low resistance of the routing lines outside the

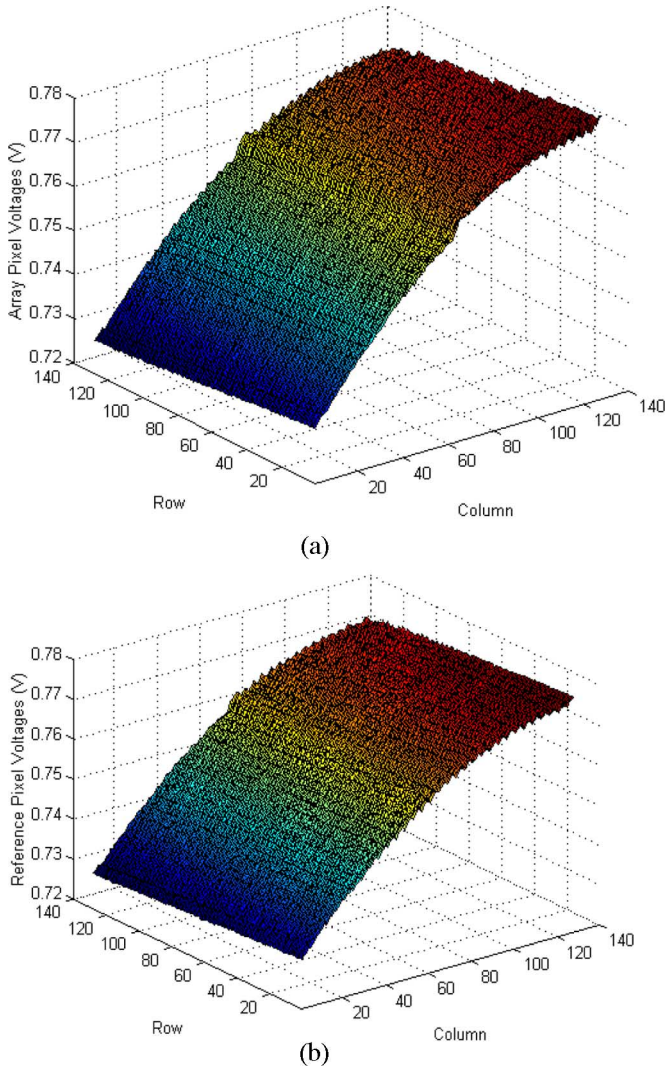


Fig. 11. Measured detector voltages in the 128 × 128 FPA (a) array pixels and (b) reference pixel voltages at each position of the row select switch. Standard deviation (σ) of the array and reference pixel voltages are measured as 14.9 and 13.6 mV, respectively.

pixel area. This result also shows that it is very important to compensate for the effect of voltage gradient along the rows. Standard deviation (σ) of the array and reference pixel voltages are measured as 14.9 and 13.6 mV, respectively. It should be noted that the reference pixel voltages change in the same way as the array pixel voltages, and they can be used for compensation purposes. Standard deviation of the differential pixel voltages is reduced down to 1.5 mV, which is equivalent to a nonuniformity value of 0.2% when calculated for the single-ended array pixel voltages. It should be noted that the proposed differential array structure with compensated routing provides about 10 times improvement in the nonuniformity compared to the uncompensated single-ended case.

Fig. 12 shows the measured histogram of the temperature sensitivity of the array pixels in the 128 × 128 FPA. The FPA is mounted on a thermoelectric cooler (TEC) and placed in a ceramic pin-grid-array package. The temperature of the chip is changed by varying the power applied to the TEC and monitored using on-chip temperature sensors. Pixel voltages

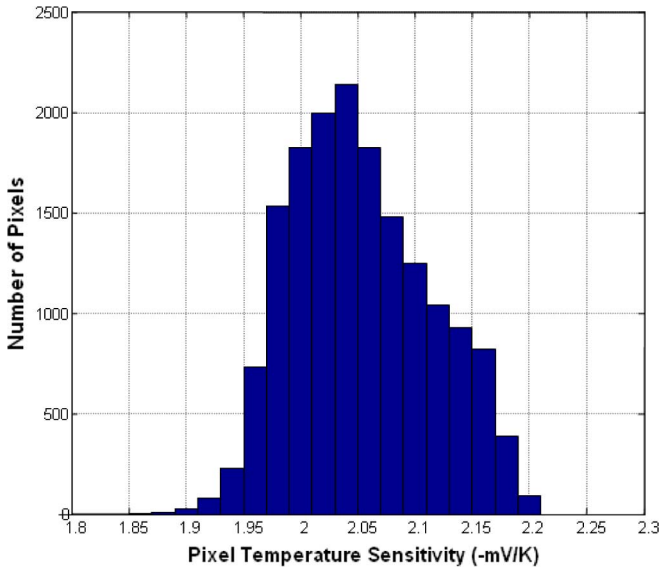


Fig. 12. Measured histogram of the temperature sensitivity of the array pixels in the 128 × 128 FPA. Mean value is −2.05 mV/K, and the standard deviation is 61 μV/K with a nonuniformity of 2.96%.

TABLE I
PERFORMANCE PARAMETERS FOR THE FABRICATED 128 × 128 DIODE TYPE MICROBOLOMETER FPA

Parameter	Value
Fabrication Technology	0.35μm 3-metal CMOS
Post Process Method	Dry Etch + Wet Etch in TMAH
Array Format	128 × 128
Pixel Size	40 μm × 40 μm
Pixel Type	Diode
Pixel Fill Factor	44 %
Absorption Coefficient	0.45
Temperature Sensitivity (dV_{pix}/dT)	-2 mV/K
Pixel Thermal Conductance (G_{th})	1.8×10^{-7} W/K
Pixel Thermal Time Constant (τ)	36 msec
Scanning Rate	30 fps
Pixel Responsivity (ℜ)	4970 V/W
Pixel Detectivity (D^*)	9.7×10^8 cmHz$^{1/2}$/W
Chip Size	6.5 mm × 7.9 mm
Number of Readout Channels	32
Electrical Bandwidth @ 30 fps	8 kHz
Detector Noise (V_n)	0.69 μV rms
Readout Noise (V_n)	0.76 μV rms
NETD† (f=1)	1 K

†Expected

are then recorded at different die temperatures. The mean value of temperature sensitivity is measured as −2.05 mV/K for both array and reference pixels. The standard deviation is calculated as 61 μV/K with a nonuniformity value of 2.96%. The mean value of the temperature sensitivity of the differential voltage between the array and reference pixels is measured as 2.3 μV/K, which shows that a differential readout structure can compensate for the variations in the ambient temperature, eliminating the need for high-precision temperature stabilization. Table I summarizes the performance parameters for the diode type microbolometer detector and the fabricated 128 × 128 FPA.

V. CONCLUSION

A low-cost 128 × 128 uncooled microbolometer FPA with its on-chip multichannel parallel readout circuitry has been implemented in a standard 0.35 μm n-well CMOS process. The fabricated FPA is based on suspended and thermally isolated p^+-active/n-well diodes, which have a pixel size of 40 μm × 40 μm with a fill factor of 44%. The detector has a measured dc responsivity of 4970 V/W when it is biased continuously by a constant current source. The detector has a measured electrical noise of 0.69 μV in 8 kHz bandwidth, which corresponds to a detectivity (D^*) value of 9.7×10^8 cm · Hz$^{1/2}$/W. The 128 × 128 FPA is scanned at 30 fps by on-chip 32-channel readout circuitry, with a measured input referred noise of 0.76 μV. Based on the measurement results, the fabricated FPA has an expected NETD value of 1 K for $f = 1$ optics when scanned at 30 fps. Considering the pulsed bias case and using optimized post-CMOS etching steps, $G_{\rm th}$ of the pixel can be improved from 1.8×10^{-7} W/K to the simulated value of 1.2×10^{-7} W/K without much changing the thermal time constant value, which will decrease the array NETD value below 700 mK. This NETD value can further be decreased by reducing the electrical bandwidth with the help of the increased number of parallel readout channels. In the limiting case, the bandwidth can be decreased down to 2 kHz, which will result in an NETD value below 350 mK. The measured uncorrected differential voltage nonuniformity for the 128 × 128 array pixels after the CMOS fabrication is 0.2% with a standard deviation of only 1.5 mV, which is low due to the improved array structure that can compensate for the voltage drops along the routing resistances in the array. Nonuniformity of temperature sensitivity of the array pixels is measured to be less than 3% with a mean and standard deviation of −2.05 mV/K and 61 μV/K, respectively. The temperature sensitivity of the differential pixel voltages has a measured mean value of 2.3 μV/K, relaxing the requirements on the temperature stabilization. Considering its performance and its simple fabrication steps, the proposed method is very cost-effective for fabricating large format FPAs for low-cost commercial infrared imaging applications.

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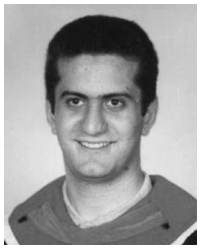

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