A LOW-POWER SWITCHED-CURRENT ALGORITHMIC A/D CONVERTER

A. Tezel[*] *and T. Akin*[*,**]

[*]Middle East Technical University, Dept. of Electrical and Electronics Engineering, Ankara, Turkey
[**]TUBITAK-BILTEN, Middle East Technical University, Ankara, Turkey
c073505@orca.cc.metu.edu.tr, tayfun-akin@metu.edu.tr

ABSTRACT

This paper reports the development of a low-power switched-current algorithmic A/D converter based on a new algorithm, providing the bit conversion in three-cycles. The converter uses modified S^2I type current copiers to reduce the overall area and power consumption. The analog portion of the converter occupies only $0.35mm^2$ area in 3μm CMOS technology. The simulation results show that the converter provides 10 bits resolution with a conversion rate of 61kHz, while dissipating only 1mW power from a single 5V supply.

1. INTRODUCTION

Algorithmic current-mode A/D converters have found a high interest due to their low power consumption and small area [1-4]. These converters have low-power consumption and small area, since the converters use a simple circuit to perform the conversion in a serial manner. The conversion algorithm is achieved using current copiers; therefore, the conversion algorithm and the quality of the current copiers directly effect the accuracy, speed, and power consumption of the converter.

There are a number of algorithms developed for algorithmic current mode A/D converters. One of the widely used algorithms is the reference restoring (RR) algorithm [1]. Although this is the simplest algorithm, the accuracy of the A/D converter in this algorithm is directly limited with the accuracy of the current copiers and comparators. Effect of comparator errors can be reduced with better algorithms. Two different algorithms are developed to reduce the nonlinearity errors caused by the comparator inaccuracy and the offset error [2, 3]. These are called redundant−signed-digit (RSD) [2] and modified reference-nonrestoring (MRN) [3] algorithms. Although these algorithms reduce the nonlinearity errors, the accuracy of the A/D converters in these algorithms is limited by the accuracy of the current copier. In addition, their power dissipation is relatively high. A novel technique was developed to increase the accuracy of A/D converters by using the more accurate regions of the current copiers [4], i.e., every memorized current is kept between $I_{ref}/2$ and I_{ref}. Although, this algorithm provides higher accuracy, the conversion speed is very low, partially due to the conversion algorithm and partially due to the current copier used in the A/D. Therefore, there is a need for a better conversion algorithm and current copiers to implement a high-speed, low power, and small area A/D converter while providing high accuracy.

This paper reports the development of such an A/D converter. The converter uses a new algorithm, providing the bit conversion in three cycles. In addition, the converter uses a new current copier cell based on S^2I current copier [6] for higher accuracy and low power consumption. The accuracy of the converter is also increased with the use of current copiers in their more accurate regions. Section II explains the new conversion algorithm and its advantages. Section III gives an overview of the current copiers that can be used in algorithmic A/D converters and explains the new copier cell developed for this converter. Finally, Section IV summarizes the circuit performance and gives conclusions of this work.

2. EFFICIENT CONVERSION ALGORITHM

In the previous ADC algorithms, the current is copied three times before it is compared with the reference current. However, in the proposed algorithm, the current is copied two times before it is compared with the reference current so the proposed algorithm gains one copying time per bit. Moreover, it also reduces the overall error, as shown in Figure 1 and Figure 2. If we assume that an error, ε, occurs per copying current, for two current copiers we get an error equal to 2ε. If we copy the currents on two current copiers to one current copier, we get a total error of 3ε, so this algorithm decreases the error by one third.

Figure 3 shows the simplified block diagram of the analog part of the converter, and Figure 4 shows the flowchart of the conversion algorithm. The conversion algorithm begins with comparing the input current with $I_{ref}/2$. If it is greater than $I_{ref}/2$, the first bit is logic 1, and the input current is copied to the dynamic current copiers N1 and N2. If it is not, the first bit is logic 0, and $I_{ref}/2$ is added to the input current to shift the current to more accurate regions of the current copiers i.e., between $I_{ref}/2$ and I_{ref}. The resulting current is copied to N1 and N2. Then, $I_{N1}+I_{N2}$ is compared with $3I_{ref}/2$. If $I_{N1}+I_{N2}$ is larger than $3I_{ref}/2$ then, the second bit is logic 1, and $I_{N1}+I_{N2}-I_{ref}$ is copied to the copiers P1 and P2. However, if $I_{N1}+I_{N2}$ is smaller than $3I_{ref}/2$ then, the second bit is set to logic 0 and $I_{N1}+I_{N2}-(I_{ref}/2)$ is copied to P1 and P2. To obtain the third bit, $I_{P1}+I_{P2}$ is compared with $3I_{ref}/2$. If $I_{P1}+I_{P2}$ is larger than $3I_{ref}/2$, then the output of the converter is logic 1 and $I_{P1}+I_{P2}-I_{ref}$ is copied to N1 and N2. If $I_{P1}+I_{P2}$ is smaller than $3I_{ref}/2$, then the output of the converter is logic 0, and the current $I_{P1}+I_{P2}-(I_{ref}/2)$ is copied to N1 and N2. This loop continues until the least significant bit is obtained.

0-7803-5474-5/99/$10.00(C)1999 IEEE

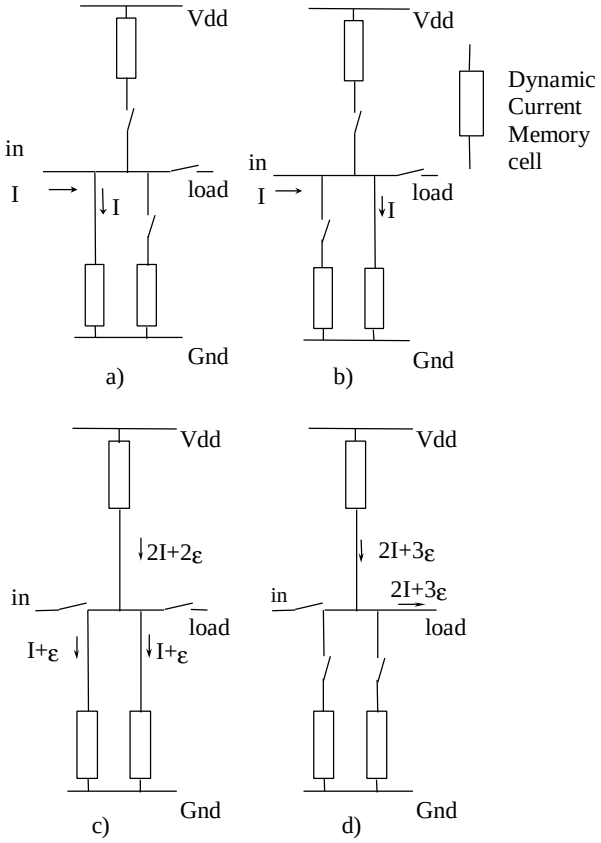

Figure 1: Errors caused by current copiers in conventional algorithm ADCs; a) current I is copied to first current copier, b) current I is copied to second current copier, c) the two copied currents, each causing error of ε, are copied to the third current copier, d) with the error caused by the third current copier total error becomes 3ε.

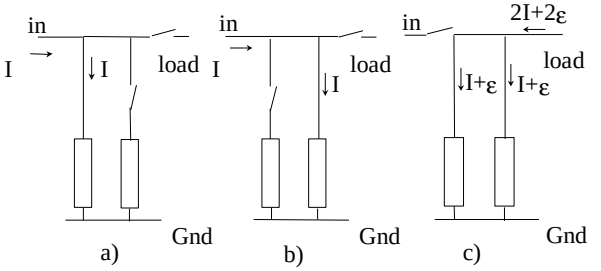

Figure 2: Errors caused by current copiers in the proposed ADC, a) the current I is copied to first current copier, b) the current I is copied to the second current copier, c) the input current is multiplied by two with an error of 2ε.

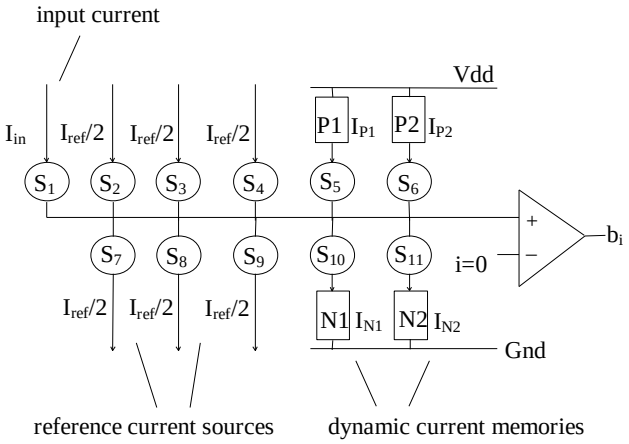

Figure 3: Simplified block diagram of the analog part of the A/D converter. This circuit requires the copying of the input current only twice, reducing the overall error and conversion cycle.

The advantage of this algorithm compared with previous algorithms is that the input current is compared with reference current before it is doubled. That means, for an n-bit converter, the input current has to be doubled n-1 times. Therefore, it gains one doubling time for each conversion. Moreover, it increases the resolution one bit more, because mainly copying the currents causes the errors, and the current will be doubled n-1 times, instead of n times.

3. NEW CURRENT COPIER

The current copier is the most important part of switched-current algorithmic A/D converters. The sampling time, power consumption, and accuracy of an ADC depend on current copiers. There are three outstanding current copiers that can be used for algorithmic A/D converters: the zero-voltage switching type current copier [5], the current copier that is used in [4], and the S^2I type current copier [6]. The zero-voltage switching current copier avoids signal-dependent charge injection, increasing the sampler's linearity significantly. It achieves 13-bit accuracy and 50Msample/s sampling rate [5], which is extremely good. However, its drawbacks are the high power consumption and large occupied area, making it unsuitable for low power applications. The current copier used in [4] is based on controlling gate voltages of several transistors in the current copier circuit. It achieves a 14-bit resolution; but, the conversion time is 175μs, which is very long [4]. The S^2I type current copier seems to be the most suitable one for low power algorithmic A/D converters. The S^2I type current copier achieves high accuracy by sampling the input signal in two steps: a coarse step and a fine step. It achieves more than 10-bit resolution with a 20MHz sampling rate [6]. This resolution can be increased further with the new modified S^2I copier cell, as explained below.

0-7803-5474-5/99/$10.00(C)1999 IEEE

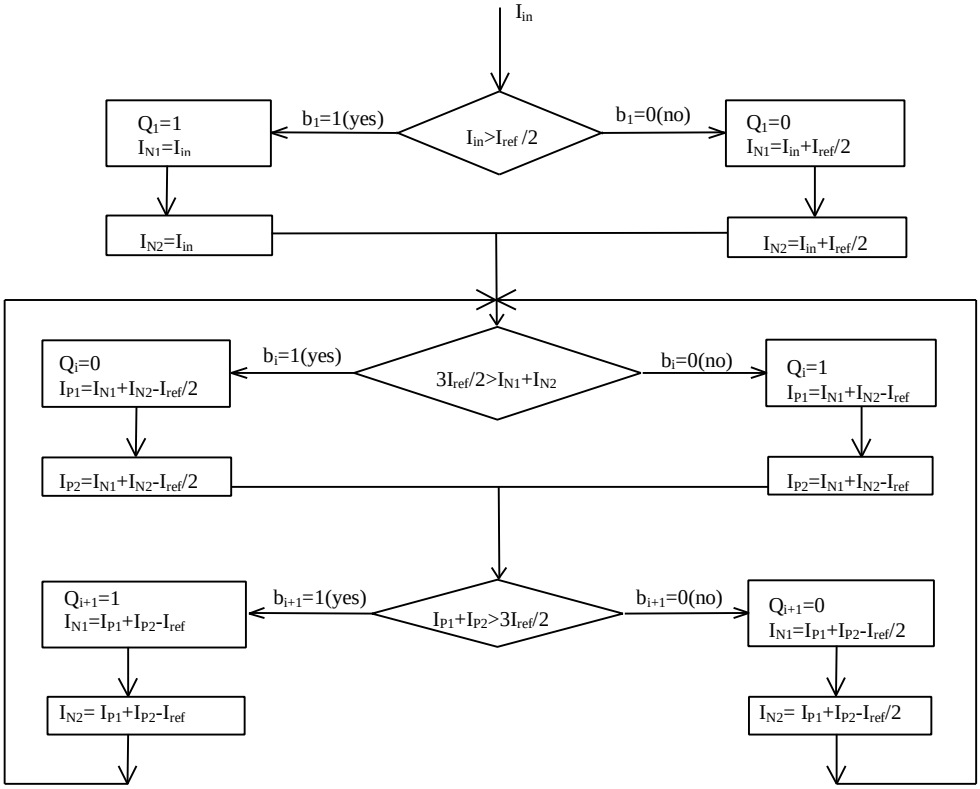

Figure 4: Flowchart of the algorithm of the A/D converter, where b_i is output of the comparator and Q_i is the output of the converter.

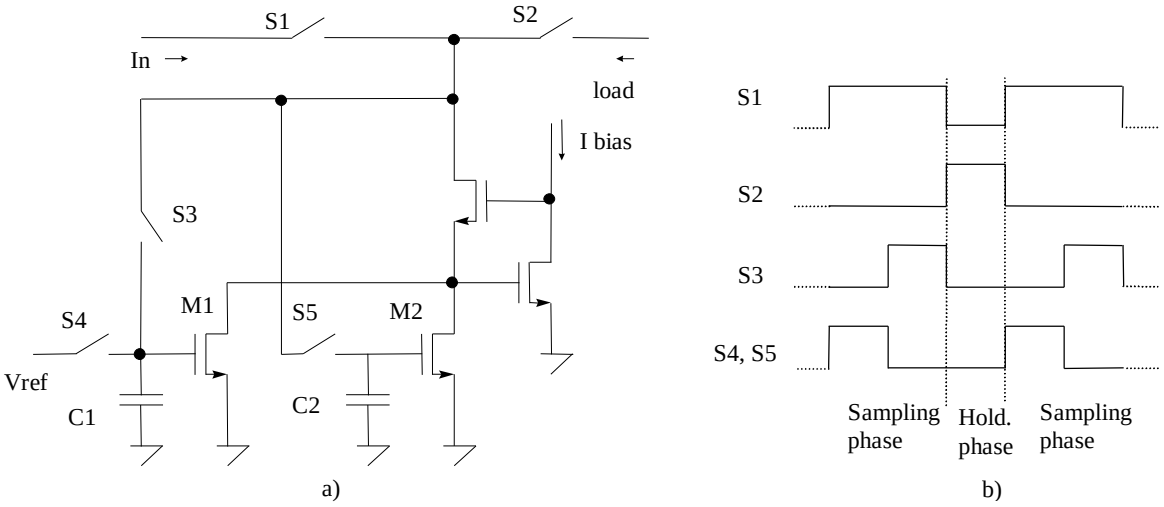

Figure 5: The new current copier cell: a) schematic view, b) states of the switches.

Figure 5 shows the schematic view of the modified current copier. This current copier is based on the regulated cascode memory cell instead of the basic dynamic current memory cell to overcome the error caused by channel length modulation.

Moreover, it uses only one cell for both coarse and fine sampling, instead of two cells that were used in [6], reducing the occupied area.

0-7803-5474-5/99/$10.00(C)1999 IEEE

The proposed current copier copies current as follows: first, S1, S4, and S5 are closed to make the coarse sampling. Then, S4 and S5 are opened and S3 is closed to make the fine sampling. Finally, S3 and S1 are opened, and S2 is closed to transfer the copied current to the load. This operation allows achieving improved current copying accuracy.

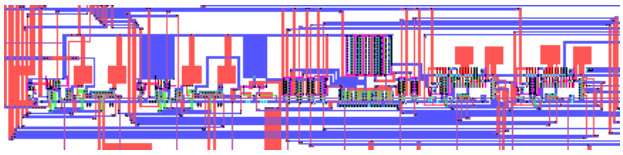

Figure 6: Layout of the analog part of the A/D converter, which occupies 0.35mm^2 area in a single metal double poly 3µm CMOS process.

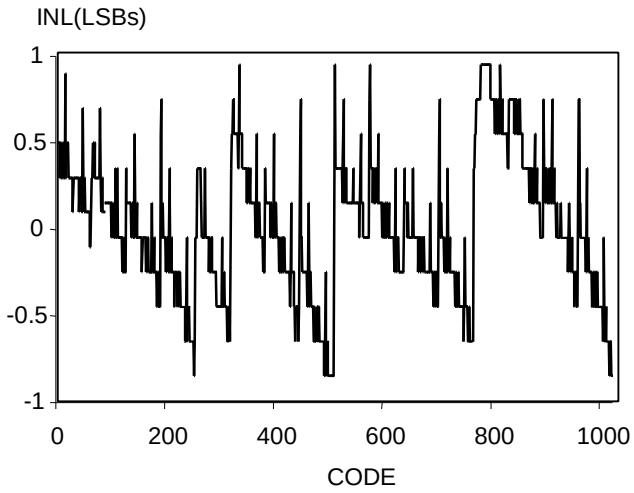

Figure 7: INL results showing 10-bit resolution at the 61ksamples/s conversion rate.

One drawback of this current copier is that it can only copy currents above a certain value given by

$$\frac{K}{2}\times\frac{W_1}{L_1}\times\left(v_{ref}-v_t\right)^2 \qquad (1)$$

where, K is the KP of transistor; W and L are width and length of the transistor, respectively; v_{ref} is the reference voltage for the gate to source voltage, and v_t is the threshold voltage of the transistor.

However, this does not make any problem in our case, because the copied current will be above $I_{ref}/2$ in this converter, as explained in Section II.

4. RESULTS AND CONCLUSION

A test circuit has been designed and send to fabrication. Figure 6 shows the layout of the analog portion of the A/D converter, which occupy 0.35mm^2 area in 3µm CMOS technology. The overall area of the converter is 4mm^2, including both analog and the digital part. The converter is simulated extensively using T-SPICE, which is an enhanced simulator for switching MOS circuits. Figure 7 shows the INL plot for 10-bit resolution when the converter is operated at the 61ksamples/s conversion rate. The maximum INL is $\pm$0.9 LSB while dissipating only 1mW from a single 5V supply. The speed of the converter can be increased further by parallel-processing, at the expense of area and power dissipation. The new algorithm, which decreases the conversion time by 1/4 and increases the accuracy by 1/3. In addition, the new current copier cell based on the S^{2}I current copier provides higher accuracy and low power consumption, and therefore, the new converter can be used in various other switched current applications.

Acknowledgments: The authors thank Mr. Selim Sermet Akbay for his help during simulations and Mr. Selim Eminoglu for his CAD support. This work is supported by NSF-International Grant No: 9602182, which is provided to Prof. Khalil Najafi of The University of Michigan and Prof. Tayfun Akin of Middle East Technical University for US-Turkey Cooperative Research on Solid-State Sensors and Interface Circuits.

5. REFERENCES

[1] D. Nairn and T. Salama, "Ratio-Independent Current Mode Algorithmic Analog-to-Digital Converters", *Proceedings of. IEEE International Symposium on Circuits and Systems*, May 1989.

[2] D. Macq and P. G. A. Jespers, "A 10-Bit Pipelined Switched-Current A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 967-971, Aug. 1994.

[3] C. Chen and C. Wu, "Design Techniques for 1.5-V Low-Power CMOS Current-Mode Cyclic Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Progressing*, vol. 45, pp. 28-40, Jan. 1998.

[4] P. Deval, J. Robert and M. J. Declercq, "A 14 bit CMOS A/D Converter based on Dynamic Current Memories," *IEEE Custom Integrated Circuits Conference*, pp. 24.2.1-4, 1991.

[5] D. Nairn, "A High-Linearity Sampling Technique for Switched-Current Circuits," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Progressing*, vol. 43, pp. 49-52, Jan. 1996.

[6] J. B. Hughes and K. W. Moulding, "S^{2}I: A Switched-Current Technique for High Performance," *Electronics Letters*, vol. 29, pp. 1400-1401, Aug. 1993.

0-7803-5474-5/99/$10.00(C)1999 IEEE