5.7 Experimental Results

In this section the dynamic overmodulation behavior of an IFOC algorithm based induction motor drive is experimentally investigated. The drive employs digital SFCR to achieve high bandwidth current regulation. Due to the laboratory limitations only an induction motor without load and without additional inertia could be tested.

A prototype digital control board (developed at Rockwell Automation-Allen Bradley, Inc. for PWM-VSC applications) and a commercial PWM-VSI (20 kW, 620 VDC, 460 V, 21 A, PWM-VSI by Rockwell Automation-Allen Bradley, Inc.) were interfaced to form the laboratory PWM inverter drive. The inverter was diode rectifier front end type. All the control tasks were performed by a digital signal processor (MOTOROLA 56005 DSP [80]) with a 40 MHz clock frequency (25 ns instruction cycle). Originally designed for computer disk drive applications, this DSP chip has six PWM counter comparators (analog/digital hardware triangular wave carrier signal and comparator circuits eliminated). Once loaded with the duty cycle count, each PWM counter increments the count, compares to the reference, and outputs a gate drive logic signal. Also, with the built in inverter blanking time generation circuit (digital), this PWM generator eliminates the need for hardware blanking time generation circuits. Since the digital control board was designed for PWM-VSC applications, it had no digital motor shaft encoder interface capability and therefore the incremental position information was absent in the controller. This hardware constraint

limited the drive bandwidth and the experimental investigation of drive dynamic performance.

The controller board employed the synchronous sampling technique to measure the motor feedback currents. An A/D converter with 2 μs conversion time and an eight-channel-multiplexer were utilized to sample the three phase motor currents, the DC link voltage, and several other analog input signals (analog speed feedback, speed reference and controller gains). The A/D sampling process was triggered every carrier cycle at the instant the PWM counters were loaded with the new duty cycle value (equivalent to triggering at the peak of the triangle). The multiplexer sequentially selected the analog signals to be sampled until all the analog inputs were sampled, held, put in a register, and finally stored in a memory location for access by the DSP.

With the motor currents being sampled first, the values of the first two currents could be utilized to calculate the third current. With this approach, the first feedback current was precisely measured (synchronous sampling), the second feedback current was measured with 2 μs delay. The current transducer (closed loop hall effect current transducers by LEM Inc.) offset errors were subtracted from these signals by the DSP (offsets were read and stored in the DSP memory with the inverter disabled during initialization). The third current was calculated from the first two and has an equivalent delay of 1 μs (average delay of the other two signals). Therefore, the feedback current values represented the per carrier cycle average currents with reasonable accuracy. This single A/D

solution resulted in a low cost controller and is suitable in many applications (Worthwhile to mention is some recent motion control DSPs utilize two parallel A/D channels and can sample two feedback currents simultaneously such that true synchronous sampling is possible [155]). The DC link voltage and other analog input signals were also sampled at the carrier frequency rate. However, due to the slow variation of these signals, they could be updated at the speed loop sampling rate (five times smaller than the carrier frequency).

Synchronous frame current controller with antiwindup structure (the algorithm described in the simulations section of this chapter) was implemented in the DSP and the controller calculations were updated once every carrier cycle. The carrier frequency was selected as 5 kHz (200 μ s carrier cycle). The speed loop and DC buc voltage disturbance rejection controller were also programmed in the DSP and the update rate was selected as 1 kHz (once every five carrier cycles). The speed loop antiwindup structure was similar to the current loop antiwindup structure and it had a constant maximum output signal limit (the maximum I_{qe} limit of the inverter drive).

Due to the lack of the digital encoder feedback signal interface capability, the experimental system had limited motion control performance. However, an analog speed feedback was utilized in order to achieve sufficient bandwidth to illustrate the dynamic overmodulation performance characteristics of various PWM methods. For this purpose, a digital incremental encoder was mounted on the shaft of the induction motor and an Allen Bradley encoder interface and

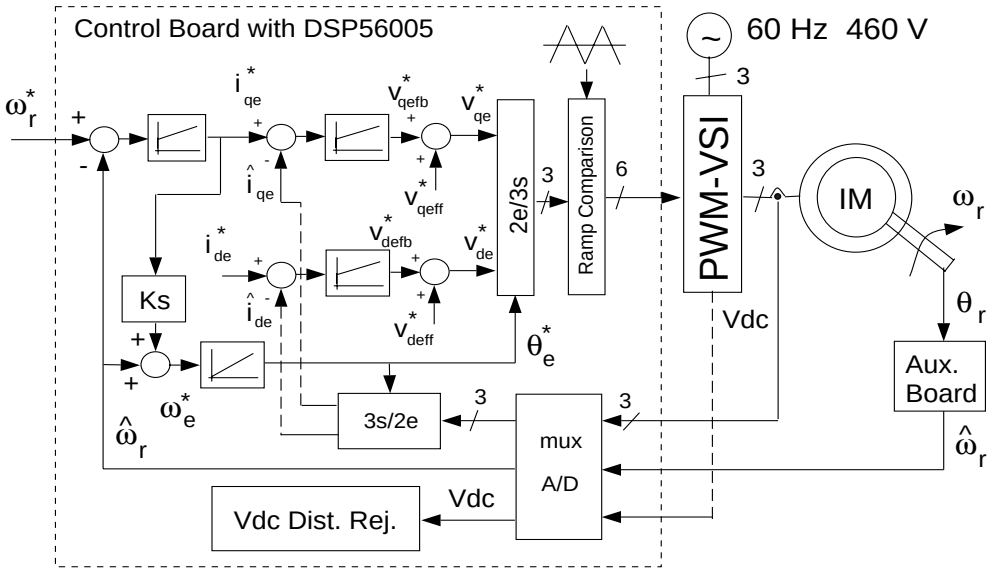

Figure 5.26: The experimental RFO-IFOC drive control diagram.

motion control circuit board (will be termed as the auxiliary board) which could provide analog speed signal output was interfaced with the encoder. The auxiliary board calculated the shaft speed and generated an analog output signal at a 1 kHz rate. This analog speed signal was input to the DSP through the analog input channels. It was processed through the A/D converter and updated once every five carrier cycles (at 1 kHz rate). Therefore, the total speed measurement delay was at least 2 ms (1 ms delay in each unit). The small delays of the several hardware and digital signal conditioning filters slightly contributed to the measurement delay. The experimental drive control diagram is illustrated in Fig. 5.26 in detail.

As illustrated in Fig. 5.26, the speed feedback signal, and the slip frequency (computed by multiplying the slip gain with I_{qe}^{*}) are added to generate the

electrical frequency reference. This signal is integrated to generate the electrical angle reference for the controller. Unlike the conventional industrial drives, which measure the shaft position and estimate the speed by computational procedures, the laboratory drive employed the reverse procedure. Therefore, the precision of the speed measurement could lead to a significant error between the shaft position and its estimate. Since the IFOC system dynamic performance is strongly affected by the position error, the bandwidth of such a system is expected to be significantly smaller than a system with an accurate position estimate. Therefore, the drive controller gains were tuned for a relatively low bandwidth. The speed loop proportional and integral gains of the laboratory drive were experimentally optimized and a 5 Hz bandwidth with unity damping could be obtained. This bandwidth value is significantly below the bandwidth of the industry standard IFOC controlled industrial drives with encoder feedback (typically 30 Hz and above is achievable) and comparable to the bandwidth of observer based drives. However, this bandwidth was sufficient to generate a notable dynamic overmodulation condition and illustrate the performance of the laboratory drive with various modulators.

The experimental motor is a four pole squirrel cage induction motor (US Motors Inc.) with the following nameplate: 5 HP, 60 Hz, 460 V, 6.9 A, 1745 RPM. The motor lumped equivalent circuit parameters were obtained by measurement and estimation (from Auto-tuning test with a commercial drive). The stator phase resistance was measured as 1.969 ohm per phase. The stator transient inductance estimated as 22.39 mH, the stator magnetizing inductance as 0.276 H,

the rotor inertia as $0.07kgm^2$, the rated magnetizing current as $I_{deR} = 3.4734A$, the slip gain as $K_s = 1.263$, the rated slip as $s\omega_{eR} = 11.52rad/s$ (55 RPM mechanical radial speed), and the rotor resistance as 1.73 ohm. The rated torque current was calculated as $I_{qeR} = 9.119A$. And the maximum torque current limit of the current controller was set to 150 % of the rated torque current, i.e. $I^*_{qemax} = 14.22A$.

In order to illustrate the dynamic overmodulation performance of the SFCR based drive with different modulators, a dynamic overmodulation condition was forced by rapidly varying the speed reference signal. While the drive was operating at 1350 RPM (45 Hz electrical frequency) at steady state and no load conditions, the speed reference was increased to 1650 RPM (55 Hz electrical frequency) in 50 ms with a ramp function. The speed ramp signal was programmed with the DSP by incrementing the signal at 1 ms rate and it was externally triggered. Since the analytical investigation clearly illustrated the inferior performance characteristics of SPWM and the THIPWM methods, experimental investigation of these methods was omitted. Therefore, the dynamic overmodulation test was conducted with SVPWM, DPWM0, DPWM1, and DPWM2. In each case the motor phase currents and speed, the modulation waves, and the controller signals (obtained through the D/A channels of the DSP board) were recorded. Since the laboratory oscilloscope channel capacity was limited to four, for each modulator the experiments had to be repeated several times to observe and record all the important the waveforms.

The dynamic overmodulation behavior of DPWM0 is illustrated in Figures 5.27,5.28,5.29,5.30, 5.31,5.32, and 5.33 with both zoomed and long time behavior waveforms. As Fig. 5.28 clearly illustrates, the saturated modulation wave indicates the drive exhibits dynamic overmodulation. Due to the saturation, the motor d and q axis current regulation becomes poor and the current and speed errors become large and oscillatory. As the speed reference is rapidly increased, first the speed regulator delay and following the current controller saturation limit the drive torque and the actual speed lags the reference significantly. With the overmodulation condition enduring, the speed loop exhibits oscillation. Note as illustrated in Fig. 5.28, the motor currents within the first few overmodulation cycles are similar to the six step mode waveforms. However, as the speed error gradually decreases to zero (in about six fundamental cycles) the linear modulation region is approached, the next steady state operating point is reached and the current waveforms become more sinusoidal. Note the new steady state operating point is slightly outside the linearity limit of this modulator. Although the final speed is smaller than the rated speed, and the drive is expected to operate in the linear modulation region, this does not occur. As Fig. 5.31 and Fig. 5.32 illustrate, in the new steady state, the d axis current is larger than its reference value. This condition implies that correct field orientation is not achieved due to the difference between the actual rotor flux angle and the flux angle the position estimator computes. Also, as a result of the incorrect field orientation the drive requires higher terminal voltage than the voltage required for the intended steady state operating speed. Therefore,

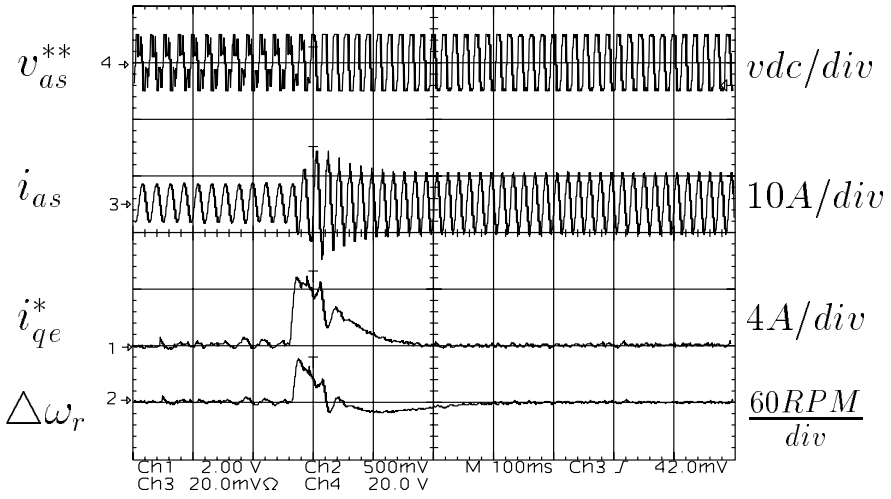

Figure 5.27: DPWM0 modulation signal, phase current, q axis current reference, and speed error oscillograms.

following the dynamic overmodulation transient, the new steady state operating point is slightly outside the linear operating region, i.e. in the overmodulation region. However, the experimental waveforms clearly illustrate the dynamic overmodulation condition and provides a base for comparing the performance of all the discussed modulators.

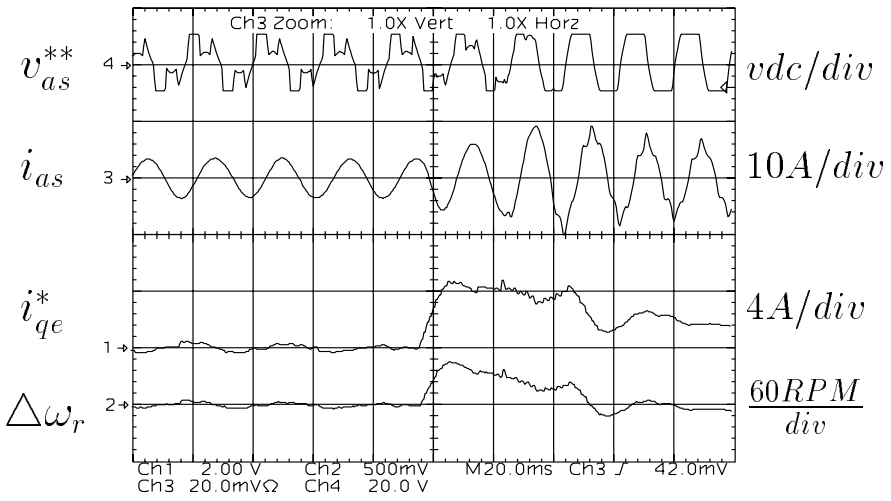

Figure 5.28: DPWM0 modulation signal, phase current, q axis current reference, and speed error oscillograms: zoomed view of the first few cycles.

Shown in Figures Fig. 5.34, Fig. 5.35, Fig. 5.36,the DPWM1 dynamic overmodulation waveforms exhibit similar characteristics to DPWM0. With the DPWM1 method having higher fundamental component voltage gain and the transients enduring several fundamental cycles, the DPWM1 method output voltage has stronger dynamics. It responds faster. However, it is more oscillatory. The speed error peak value of DPWM1 is larger than the DPWM0 case. Also the phase currents of DPWM1 have larger peak value. The large phase error and high fundamental component voltage gain characteristics of this method result in poorer dynamic overmodulation performance of this method compared to DPWM0. As the waveform of Fig. 5.36 illustrates, with this method also correct field orientation is not achieved due to the incorrect rotor flux angle estimation and at the final operating point the d axis current is larger than

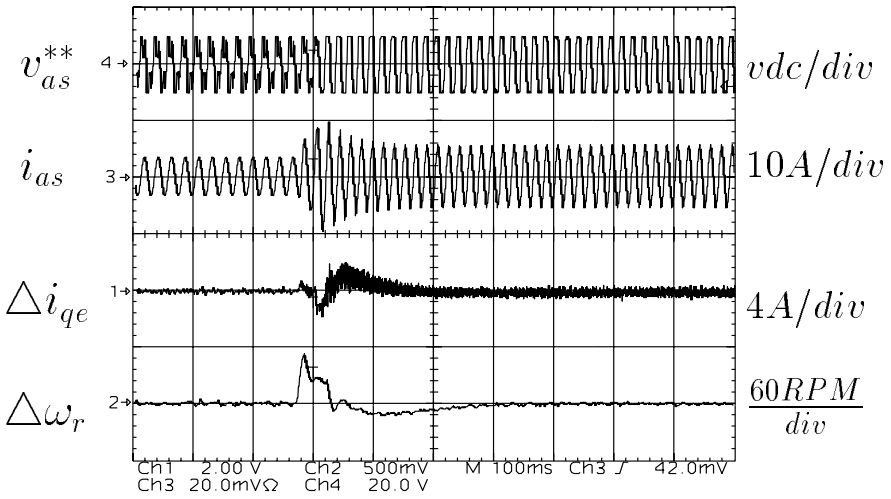

Figure 5.29: DPWM0 modulation signal, phase current, q axis current error, and speed error oscillograms.

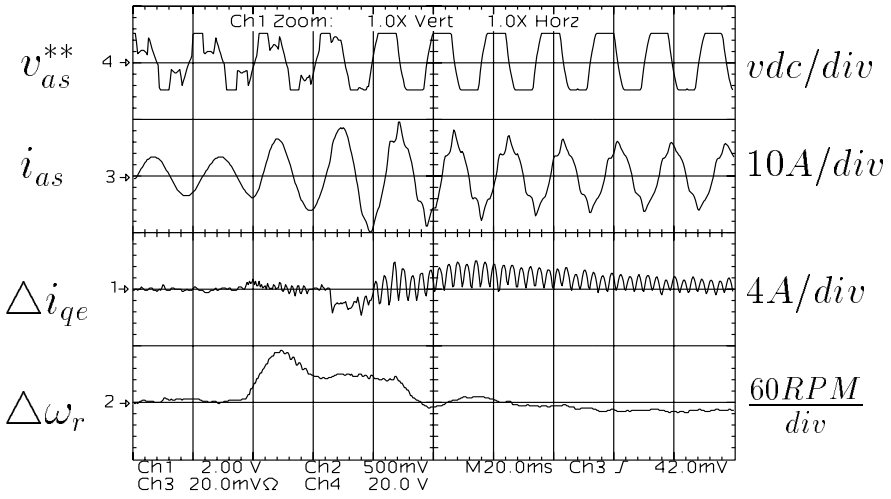

Figure 5.30: DPWM0 modulation signal, phase current, q axis current error, and speed error oscillograms: zoomed view of the first few cycles.

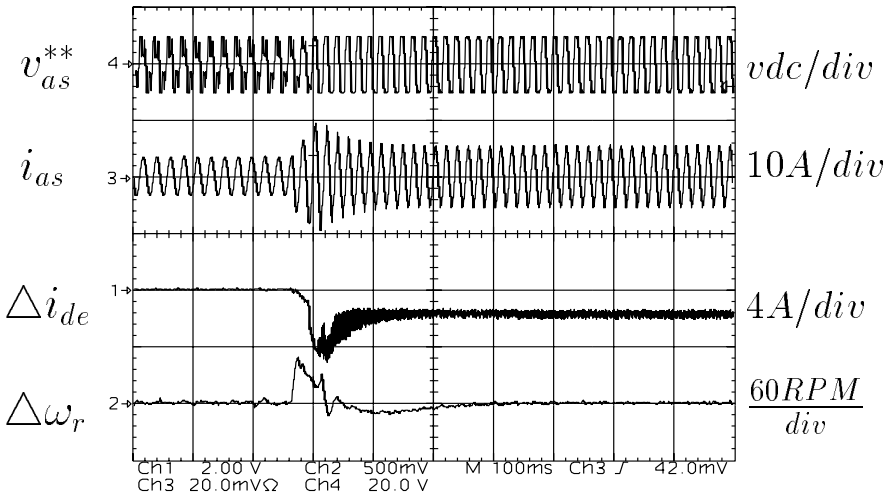

Figure 5.31: DPWM0 modulation signal, phase current, d axis current error, and speed error oscillograms.

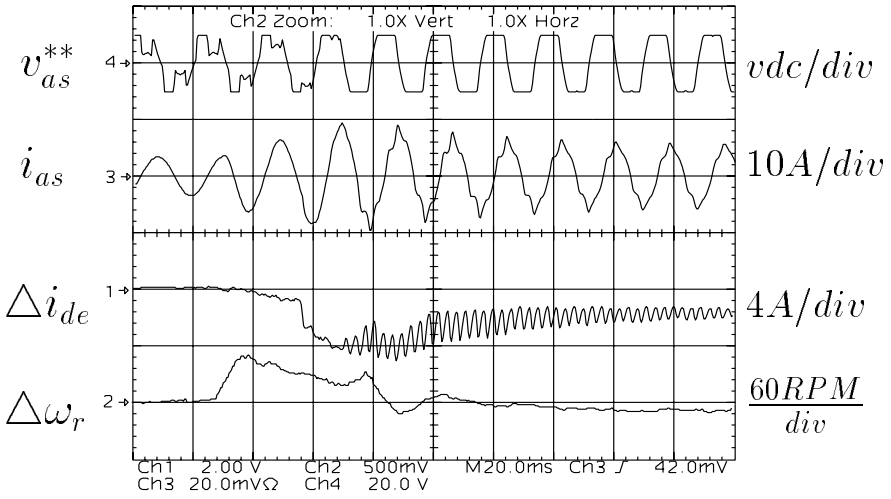

Figure 5.32: DPWM0 modulation signal, phase current, d axis current error, and speed error oscillograms: zoomed view of the first few cycles.

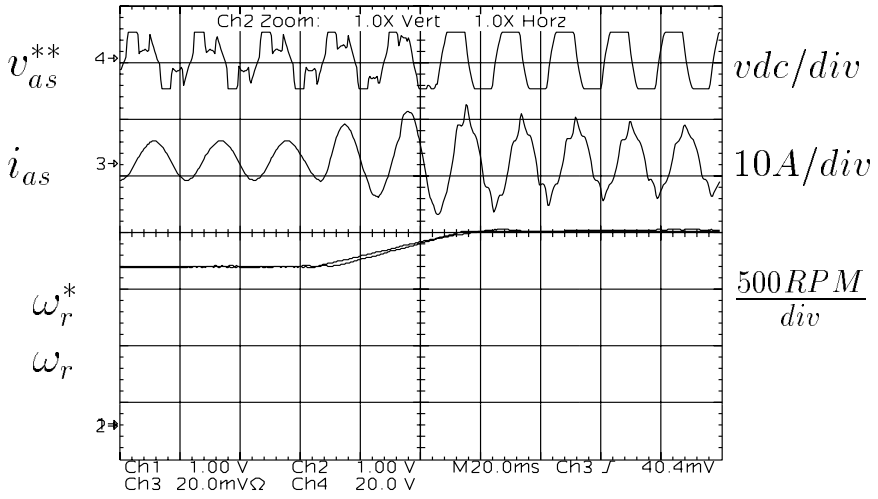

Figure 5.33: DPWM0 modulation signal, phase current, speed and speed reference oscillograms.

the reference value. Therefore, at the final operating point this modulator also operates outside its voltage linearity region. The long term waveforms of this case will be omitted and they are similar to the DPWM0 waveforms.

Figures Fig. 5.37, Fig. 5.38, Fig. 5.39, and Fig. 5.40 illustrate the DPWM2 dynamic overmodulation characteristics. It is apparent from the waveforms that the poor phase error characteristics of this modulator result in poorer response compared to DPWM0 and DPWM1. As the all the three figures illustrate, the speed error is more oscillatory and the maximum error is significantly larger than the DPWM0 and DPWM1 case. Under a dynamic overmodulation condition, DPWM2 results in poor d and q axis voltage partitioning and results in significantly larger flux current and significantly smaller torque current. As a result, the dynamic performance significantly degrades. Although the zoomed

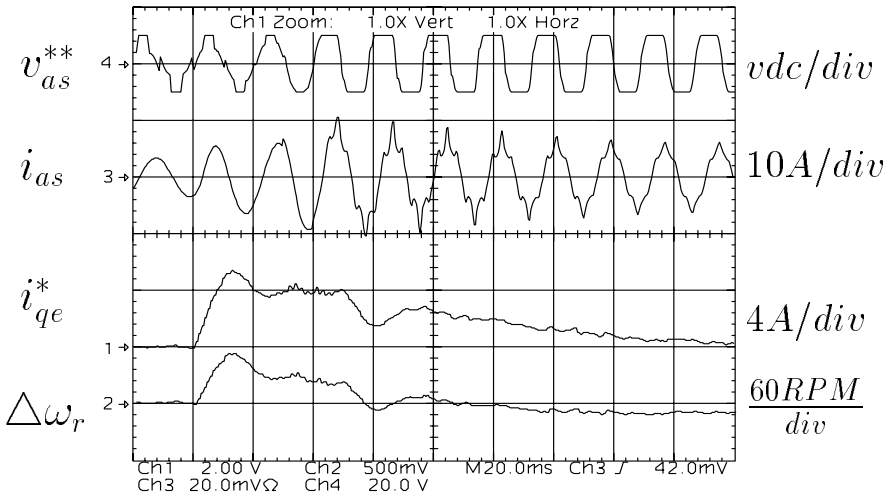

Figure 5.34: DPWM1 modulation signal, phase current, q axis current reference, and speed error oscillograms.

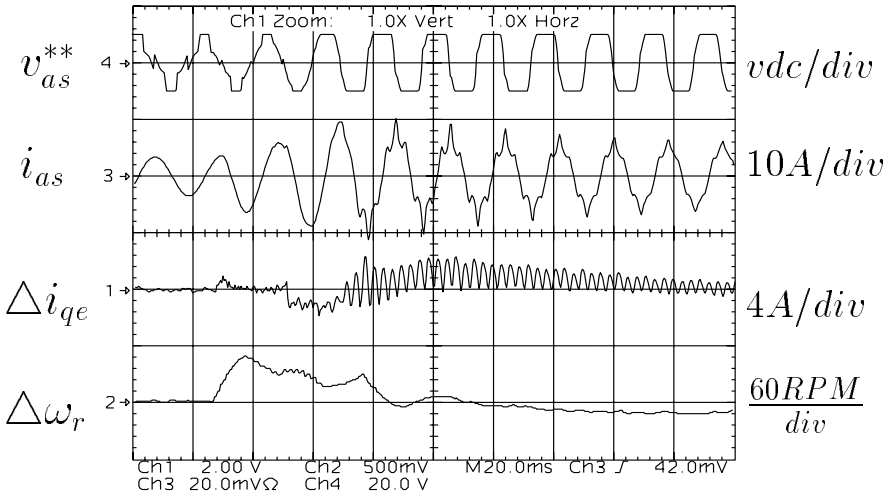

Figure 5.35: DPWM1 modulation signal, phase current, q axis current error, and speed error oscillograms.

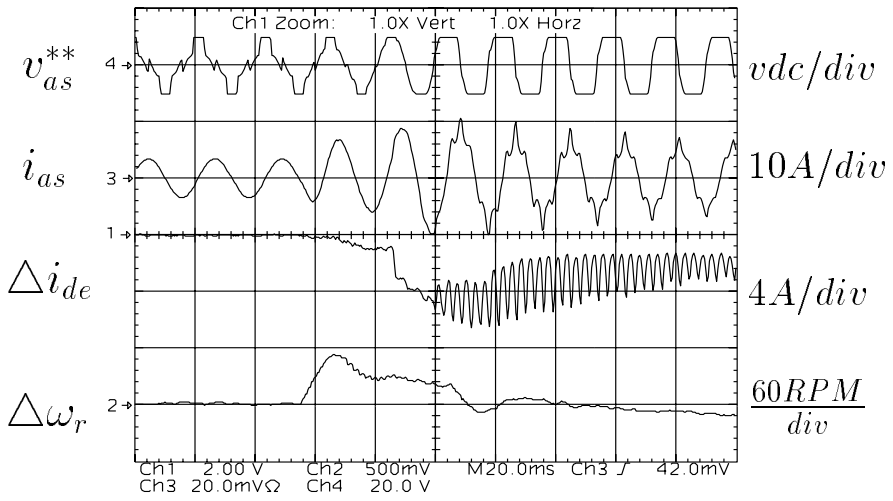

Figure 5.36: DPWM1 modulation signal, phase current, d axis current error, and speed error oscillograms.

view of Fig. 5.39 illustrates the d axis current error is more successfully manipulated than the other cases (at least for the first few cycles), as the speed error is not rapidly manipulated, the d axis current error increases again and the incorrect flux orientation (due to incorrect flux angle estimation) yields a final operating point in the overmodulation region.

Figures Fig. 5.41, Fig. 5.42, and Fig. 5.43 illustrate the SVPWM dynamic overmodulation performance. As the figure indicates, the SVPWM performance is less oscillatory than DPWM1. However, a comparison between SVPWM and the DPWM1 and DPWM0 indicates these modulators perform quite similarly. This is due to the fact these methods exhibit similar phase characteristics. DPWM0 phase error is positive, however small. DPWM1 phase error is larger, however its polarity alternates and for dynamics enduring a period of one-sixth

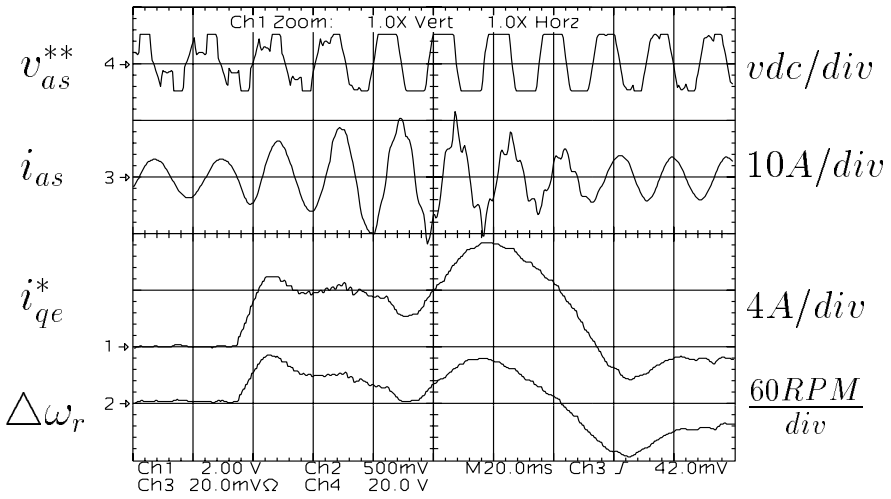

Figure 5.37: DPWM2 modulation signal, phase current, q axis current reference, and speed error oscillograms.

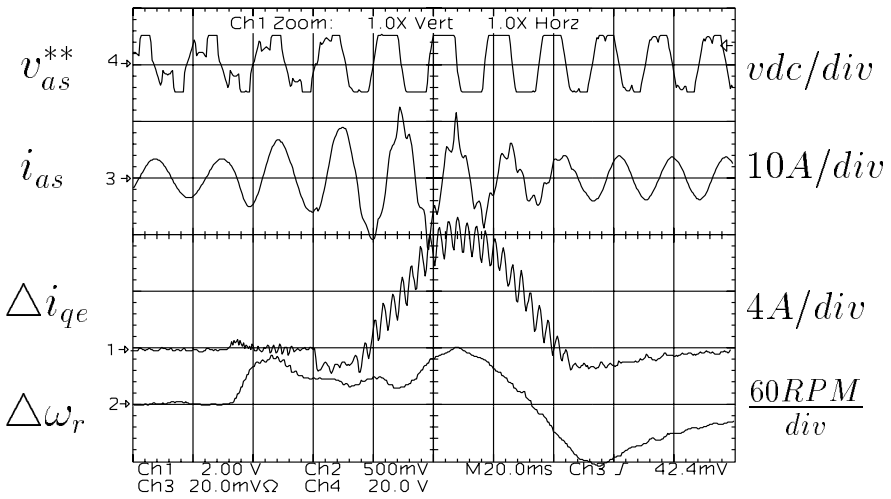

Figure 5.38: DPWM2 modulation signal, phase current, q axis current error, and speed error oscillograms.

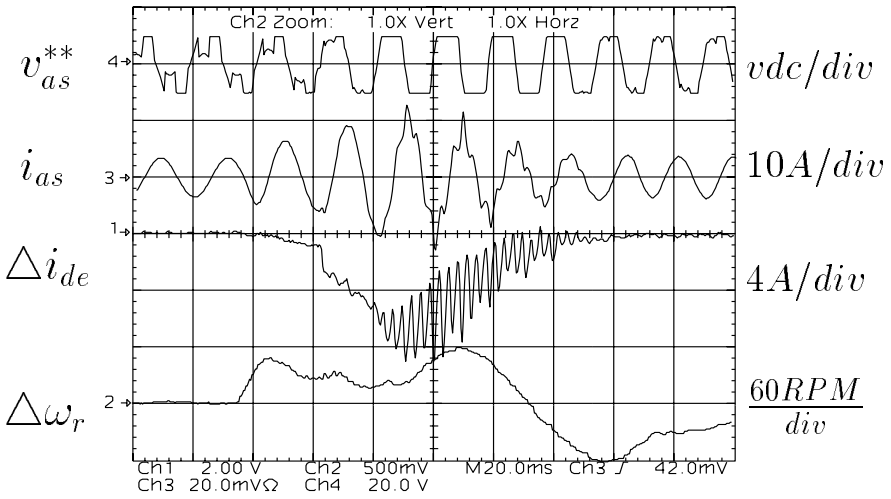

Figure 5.39: DPWM2 modulation signal, phase current, d axis current error, and speed error oscillograms.

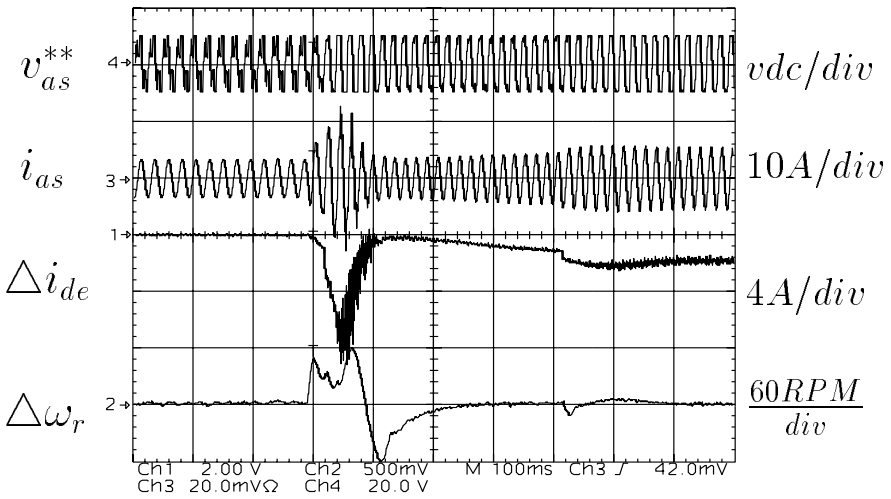

Figure 5.40: DPWM2 modulation signal, phase current, d axis current error, and speed error oscillograms.

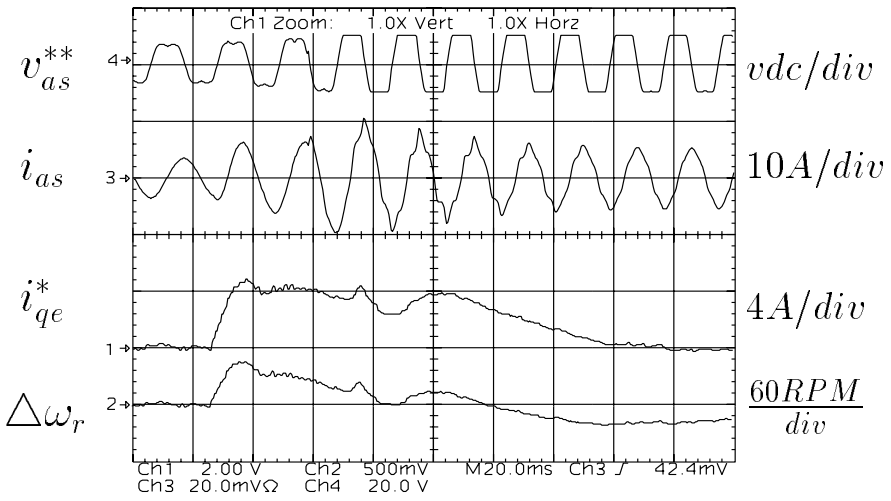

Figure 5.41: SVPWM modulation signal, phase current, current reference, and speed error oscillograms.

of a fundamental cycle or longer, it yields practically a small average value. Although for different reasons, both DPWM methods exhibit a performance similar to SVPWM. However in a higher bandwidth drive, dynamics enduring shorter time intervals are expected to yield distinguishable differences between all the methods (as predicted by analytical models). Due to its one-step-optimal performance, the SVPWM method manipulates the flux oscillation more rapidly and in the final operating point the motor phase current is more sinusoidal indicating an operating point closer to the maximum linear modulation boundary. Partially, the current waveform is more sinusoidal due to the fact the effective PWM frequency of DPWM methods is 66 % of the SVPWM method.

Although the overshoot and the initial response characteristics vary, the settling time is practically the same in all the modulator cases. This is due to the

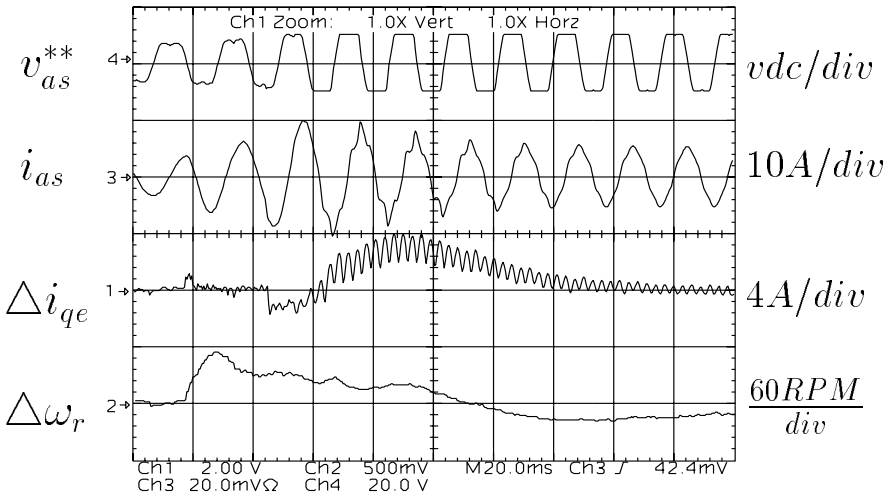

Figure 5.42: SVPWM modulation signal, phase current, q axis current error, and speed error oscillograms.

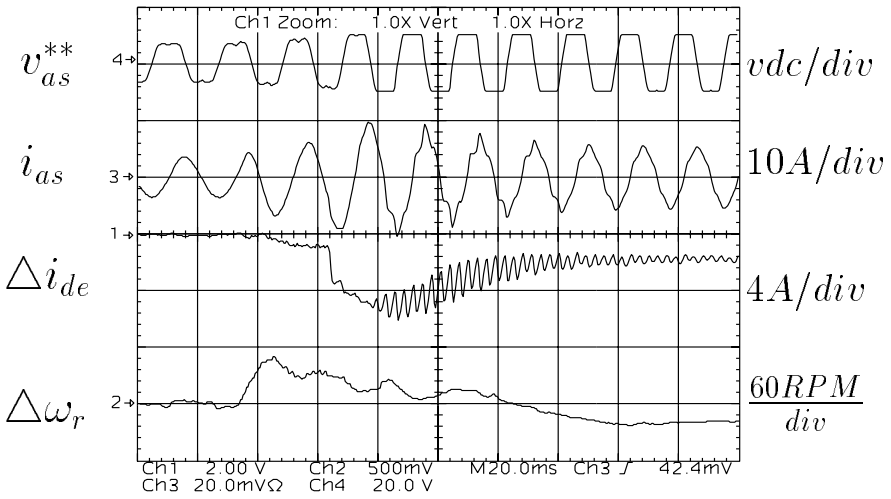

Figure 5.43: SVPWM modulation signal, phase current, d axis current error, and speed error oscillograms.

fact that the drive bandwidth is small (the proportional and integral gains are small) and the antiwindup controllers limit the reference voltage vector magnitude to be only slightly larger than the hexagon boundary (relatively small modulation index values). As all modulators have small phase and magnitude error for small modulation index values, the response is slow and takes several fundamental cycles. Over such a long period the fundamental component gain concept is valid in predicting the performance. With the modulation signals limited to the neighborhood of the hexagon, the voltage gain values of the discussed modulators are comparable, therefore the settling time of the speed controller (or the average response time) is practically the same in all the modulators tested in the laboratory. However, as illustrated, the maximum error and oscillations are different, and determined by the modulator characteristics.

Since the dynamic overmodulation behavior is dependent on the position of the voltage vector immediately before the transient (i.e. the rotor position at the triggering instant), randomly triggering the dynamic overmodulation mode results in slight differences in the dynamic performance. If the reference vector is closer to the hexagon sides than the middle, initially there exists more voltage to manipulate the dynamics (same in any segment). Therefore, the dynamic behavior is dependent on the initial (previous to dynamic overmodulation) position of the reference vector phase angle. However, with the experimental system having a relatively low bandwidth, and the dynamics lasting significantly longer than a time period corresponding to a hexagon segment, the triggering instant

of the dynamic overmodulation condition had little effect on the transient period and the peak speed ripple. Therefore, the initial conditions deserve less attention than the overall dynamic behavior. A large number of dynamic overmodulation tests triggered at different voltage vector spatial positions indicated the triggering point sensitivity of the dynamics was negligible. Therefore, the remaining experiments were conducted with no significant attempt to repeat the same exact initial conditions in each case.

Although the experimental system could not exhibit a true IFOC performance due to the inaccuracy involved in measuring the rotor angle, the experiments were sufficient to illustrate the modulator dependent dynamic overmodulation behavior of the drive. With a high bandwidth controller and accurate rotor angle measurement, the modulator characteristics could be illustrated into more detail, as the simulation results indicated.

The experimental results of this section clearly illustrated the influence of the modulator phase and magnitude characteristics on the drive dynamic performance in the overmodulation region. The experiments suggest the SVPWM has better performance than DPWM methods, and DPWM2 in particular performs poorly and may render the drive unstable. It is apparent that combining several modulators and in the overmodulation region selecting a higher performance modulator will yield a high dynamic performance. While in the linear modulation region, GDPWM or a DPWM method of choice can be selected for low switching losses. During dynamic overmodulation, SVPWM or other

methods discussed in the simulation section could be selected. Such a hybrid algorithm could be successfully implemented in modern digital platforms and result in an overall high performance drive.

5.8 Steady State Overmodulation In Current Controlled Drives

As the previous chapter illustrated, voltage feedforward drives could be successfully operated in the overmodulation region. However, the dynamic performance and steady state output voltage/current waveform quality of the drive would degrade in the overmodulation region. As the overmodulation region is entered, the PWM output voltage begins to contain a considerable amount of subcarrier frequency harmonic content. The waveform distortion rapidly increases with the modulation index, and becomes maximum at the six-step operating point. The degree of performance loss is secondarily dependent on the modulator type and as clearly illustrated, DPWM methods are superior to all other modulators. With the overmodulation performance of voltage feedforward drives being limited, certain applications involving such drives may limit the drive maximum output voltage to a value smaller than the six-step voltage value (a modulation index smaller than unity). As the theoretical and experimental investigations indicated, all high performance modulators (including DPWM methods) exhibit rapid performance deterioration after approximately 0.95 modulation index. In

waveform distortion sensitive applications this approximate value may be utilized as the maximum modulation index limit. As a result, voltage feedforward controlled drives can be operated in the overmodulation region and power electronics devices of the inverter can be utilized at high capacity and the drive can perform in a wider operating range with improved DC bus voltage disturbance rejection. In high performance current regulated drives, however, the overmodulation region is less efficiently utilized than in voltage feedforward drives.

As the dynamic overmodulation studies of this chapter indicated, in the overmodulation region, current controlled drives exhibit strong interaction between the modulator and the current controller (and possibly outer control loops also). This interaction results in significant current, torque, and speed oscillations and degrades the performance. As the simulations and experimental investigations illustrated, dynamic overmodulation performance of current controlled drives could be enhanced by employing antiwindup controllers, careful current controller design, and proper modulation algorithm choice. Regardless of the controller type and performance, however, the overmodulation performance remains inferior to the linear modulation region performance.

Due to the high performance motion quality requirements, in most current controlled drives the intended steady state operating region is the linear modulation region and the overmodulation region may only be entered during transients. However, in certain applications steady state operation in the overmodulation may be allowed. For most electric motor drives steady state

overmodulation occurs at high shaft speed, and the torque ripple generated due to overmodulation harmonics could be sufficiently suppressed by the shaft inertia and speed regulation can be satisfactory. In particular, this is true for induction motors with relatively large leakage inductance. Since the leakage inductance suppresses the overmodulation harmonic currents, with higher leakage inductances the associated torque ripple is relatively small. Perhaps, PM motors with small leakage inductance values would have significant harmonic current and the associated torque ripple would be prohibitive in certain applications. Therefore, current controlled AC motor drives with moderate high speed regulation requirements and suitable motor characteristics could be operated in the overmodulation region not only during transients, but also at steady state (at least in the lower overmodulation region). In this section the performance issues of current controlled drives when operating in the overmodulation region at steady state will be investigated.

While within the linear modulation range, the steady state voltage and current waveform characteristics of an SFCR controlled drive are the same as the voltage feedforward drive for the same modulator and operating conditions. However, in the overmodulation region the SFCR controlled drive (with or without current controller antiwindups) exhibits poorer steady state performance than the voltage feedforward type. This performance degradation is due to the fact that the feedback currents affect the current controller performance.

In voltage feedforward drives when operating in the overmodulation region,

the overmodulation harmonics result in current harmonics at their associated frequencies. In particular, the first few harmonics, the 5th, 7th, 11th, and 13th are large in magnitude. They induce torque ripple that results in speed oscillations and performance degradation. Since the $\frac{V}{f}$ controller and the modulator are feedforward no additional dynamics are generated. In current controlled drives, however, the feedback current overmodulation harmonics affect the drive performance significantly. As they are fed to the proportional and integral blocks of the controller, the controller generates modulation signals with overmodulation harmonic components and oscillatory behavior results. Intelligently designed antiwindup controllers partially limit these voltages and the associated oscillations. However, they introduce additional voltage nonlinearity to the drive and limit the voltage range of the drive. It is apparent that for superior steady state overmodulation performance of current controlled drives, the overmodulation harmonic currents should be removed from the measured feedback current. In addition the modulator fundamental component voltage gain loss in the overmodulation region could be compensated by employing the inverse gain compensation technique. However, both modifications degrade the drive dynamic overmodulation performance. Inverse gain compensation increases the current controller overshoot and eliminating the overmodulation harmonics from the feedback currents by filtering techniques increases the controller delay. Also, with the overmodulation harmonics absent from the feedback path, the current controller can no more provide inherent overcurrent protection. The above discussions clearly illustrate the trade-off between the steady

state and dynamic overmodulation performance of the current controlled drives. Therefore, steady state overmodulation of most current controlled drives in the overmodulation is limited to less than 0.95 modulation index (in particular, for drives employing motors with relatively small leakage inductances) and the effect of the overmodulation harmonics is only suppressed by the antiwindup controllers. This performance limitation is valid for all the carrier based and on-off current controllers. Therefore, the discussion involving the high performance SFCR is sufficient. However, it should be noted, on-off current controllers such as the hysteresis current controller have inferior steady state overmodulation and superior dynamic overmodulation performance to SFCR. In the following, a simulation study will attempt to illustrate the steady state overmodulation performance issues of current controlled drives and describe a method to provide enhanced steady state current controlled drive performance. Perhaps, such studies are necessary to initiate thoughts for developing current controllers with better overall characteristics than the conventional current controllers.

5.8.1 A Simulation Study of Steady State Overmodulation

In this section, the current controlled drive steady state performance will be investigated by a computer simulation. For the sake of simplicity, a simple three phase load consisting of resistance, inductance, and sinusoidal voltage connected in series (per phase) will be simulated. The load parameters are

$L_\sigma = 12.79mH$, $R_\sigma = 0.4425ohm$, $f_e = 60Hz$, and $E_{max} = 310.0V$. A digital SFCR with once per carrier cycle synchronous sampling and PWM write-out rates will be employed. The carrier frequency is 5 kHz. Except for the antiwindup controllers, the current controller is designed in the same manner as for the simulations in the dynamic overmodulation study. In the simulation, the current controller does not employ any antiwindup on the PI controller such that the influence of overmodulation harmonics on the drive performance could be clearly observed. The DC bus voltage of the inverter is fixed at 620 V. Only the DPWM1 method is simulated.

The system is first operated at 0.933 modulation index until $t = 0.1s$ (with $E_{max} = 365V$ an overmodulation condition is created), then the d axis current command is stepped up to a value to yield approximately a modulation index of 0.975. Figure 5.44 shows the corresponding current, modulation, and controller signal waveforms during overmodulation. As the figure indicates, in particular in the higher overmodulation region, the currents contain large amount of overmodulation harmonics. The PI controller signals are oscillatory and they generate modulation waves with no quarter-wave symmetry. Hence, increased current harmonic content and oscillatory behavior compared to an open loop overmodulation operating condition.

In Figure 5.45, a small portion of the previous figure is shown. Generated from the synchronously sampled phase currents, the d and q axis currents, labeled in the figure as IQSE, and IDSE, have significant ripple, mainly at $6f_e$

frequency. Since the 5th and 7th overmodulation harmonics form a 6th harmonic in the synchronous frame, this result is to be expected. The PI controllers respond to these harmonics and generate modulation signals with such harmonic components and the modulator quarter-wave symmetry is lost. Figure 5.46 provides a more detailed view of the modulation and phase current waveforms at $M_i = 0.933$. It is clear from the figure that the modulation wave is not quarter-wave symmetric. Operating at higher modulation indices (as the 0.975 modulation index case illustrated) increases the asymmetry and the distortion, such that the performance is unacceptable. Therefore, without proper structural modifications, the SFCR controlled drive can not successfully operate in the higher overmodulation region at steady state.

5.8.2 Steady State Overmodulation Performance With Feedback Current Harmonic Reduction

Having demonstrated the steady state overmodulation performance deficiency of the SFCR controlled drive in the previous section, we next investigate the performance of such a drive when the overmodulation harmonics are eliminated from the feedback path of the controller. An overmodulation harmonic current estimation method will be developed and the estimation method will be employed in eliminating the harmonic currents from the controller feedback simulated in the previous section. The simulation results will be evaluated and compared to the previous case.

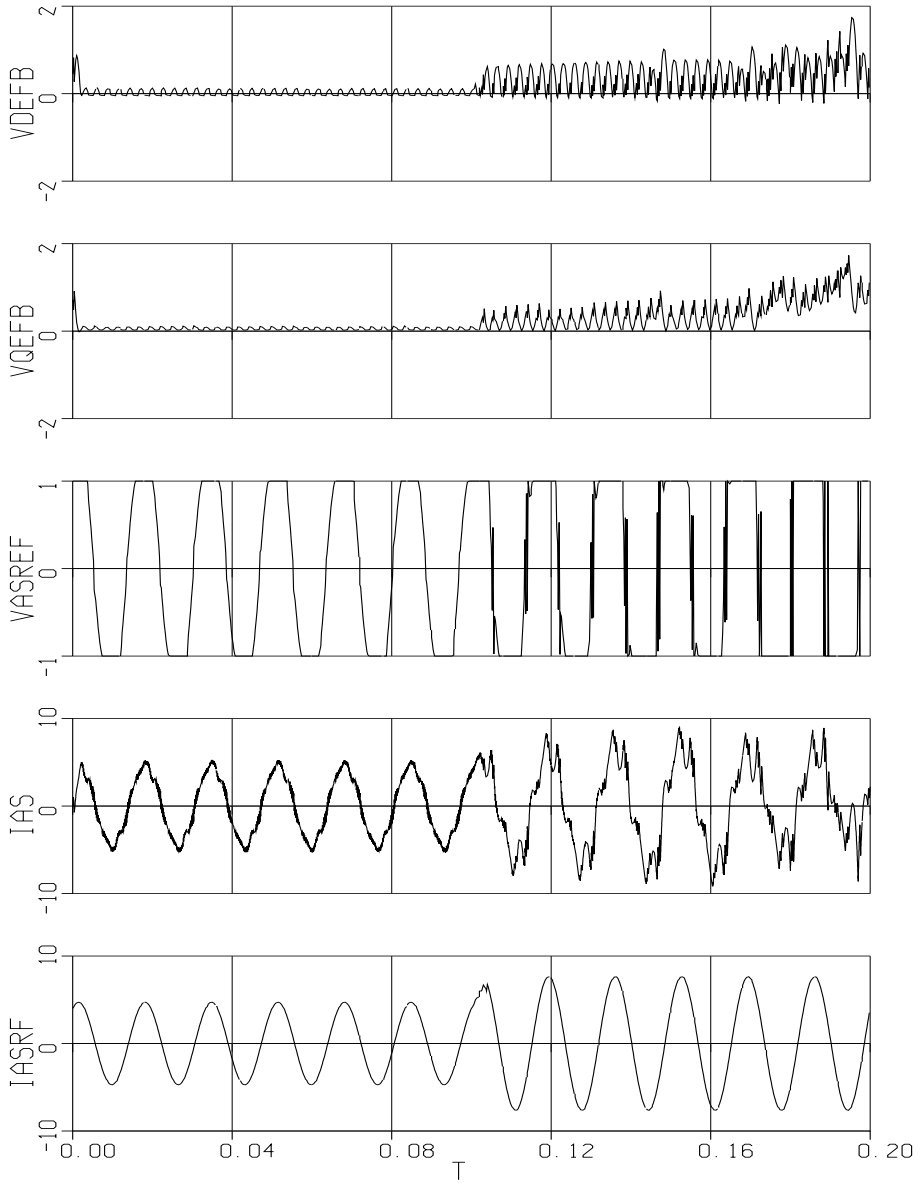

Figure 5.44: SFCR based system simulation waveforms in the overmodulation range. Traces (bottom to top): reference and actual phase currents, DPWM1 modulation wave, q and d axis PI controller outputs. At $t = 0.1s$, M_i is increased from 0.933 to 0.975.

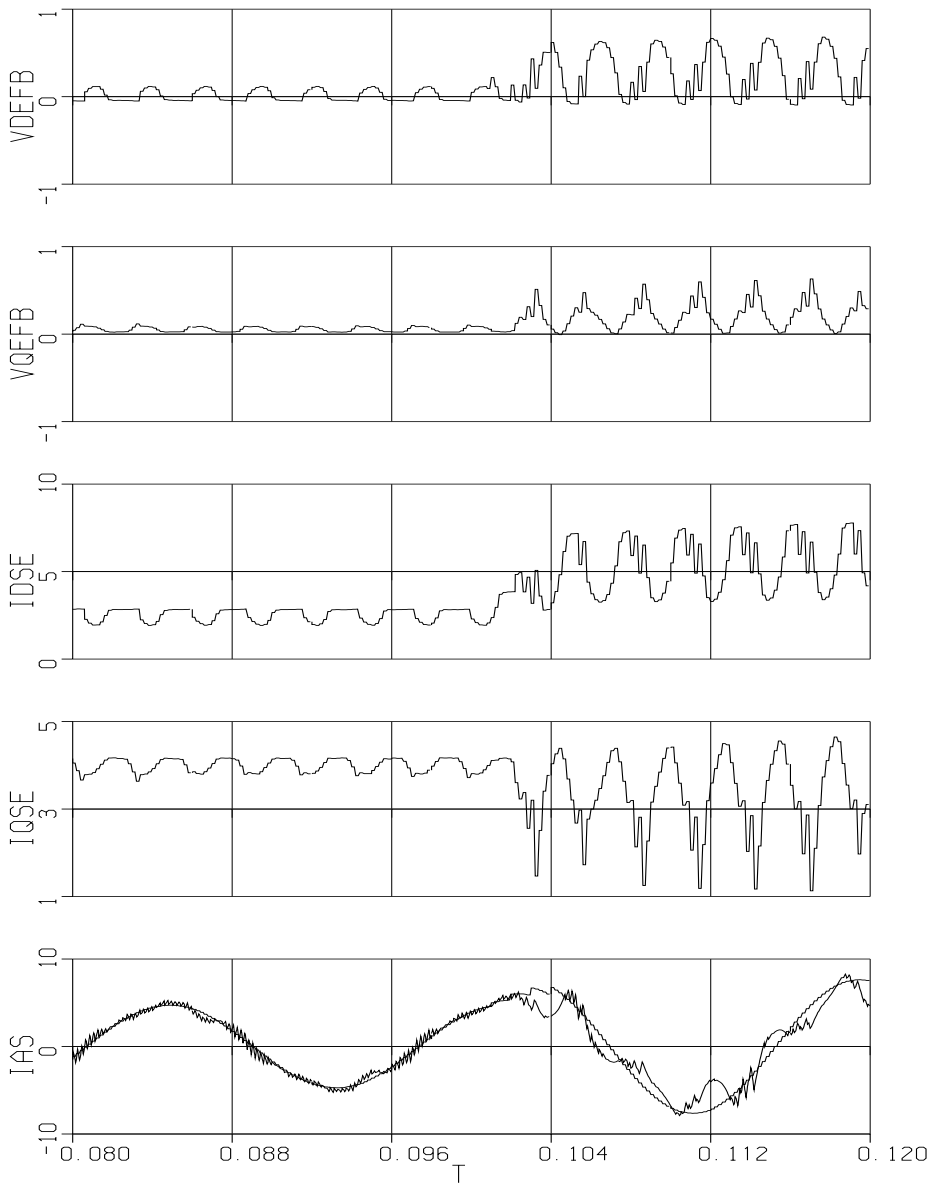

Figure 5.45: Detailed view of the system characteristic waveforms in the overmodulation range. Traces (bottom to top): reference and actual phase currents, discretized q and d axis currents, q and d axis PI controller outputs.

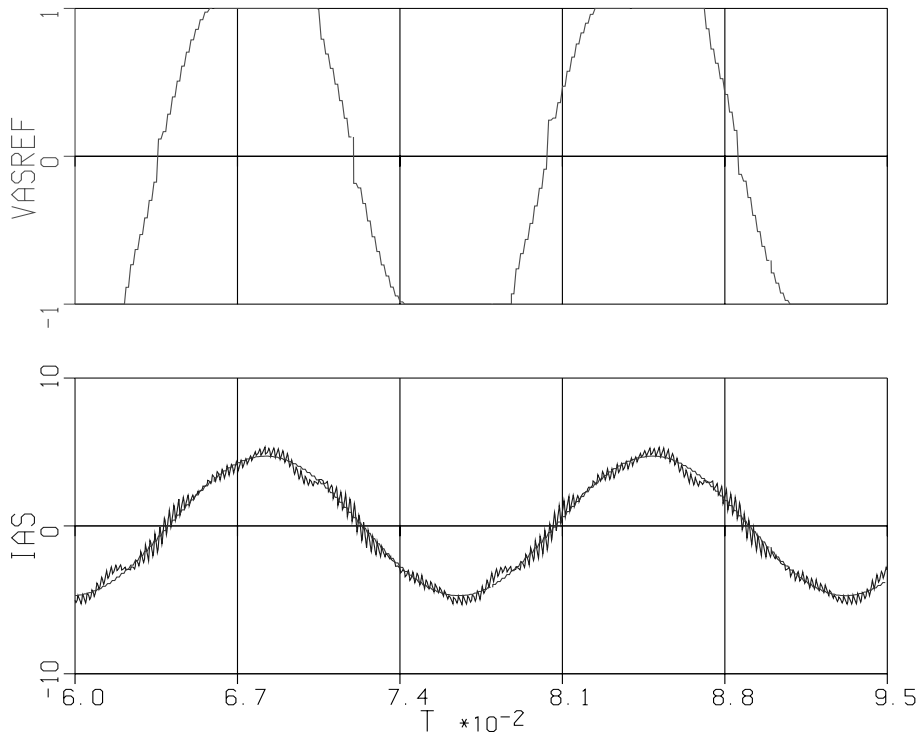

Figure 5.46: Zooming into the phase current and modulation wave at $M_i = 0.933$. Traces (bottom to top): reference and actual phase currents, and DPWM1 modulation wave.

In this work, a reference model based harmonic estimation method is developed. The induction machine harmonic behavior can be modeled by its transient impedance circuit [108, 145]. Figure 5.47 shows the induction machine constant flux model, and harmonic equivalent circuit. The motor harmonic equivalent circuit model can be represented in any reference frame. For this application, the synchronous frame equivalent circuit is suitable. If the AC motor harmonic voltages are known, then the corresponding d and q axis harmonic currents can be estimated from the harmonic equivalent circuit as follows.

$$i_{qeh}(t) = \int_0^t \frac{v_{qeh}(t) - r_\sigma i_{qeh}(t) - w_e L_\sigma i_{deh}(t)}{L_\sigma} dt + i_{qeh}(0) \qquad (5.18)$$

$$i_{deh}(t) = \int_0^t \frac{v_{deh}(t) - r_\sigma i_{deh}(t) + w_e L_\sigma i_{qeh}(t)}{L_\sigma} dt + i_{deh}(0) \qquad (5.19)$$

Figure 5.48 shows the harmonic estimation based system controller block diagram. Figure 5.48(a) shows the current regulator structure, including the fundamental component gain compensation scheme. The low pass filter (LPF), provides a smooth gain compensation signal and helps estimate the overmodulation harmonic voltage signal. As shown in Figure 5.48(b), the overmodulation harmonic voltages are estimated from the modulator input and output waveforms. In the overmodulation region, the modulator output signal is saturated and has a lower fundamental component magnitude than the reference. When the inverse gain compensation technique is involved, the original modulation signal and the modulator output signal have the same fundamental component.

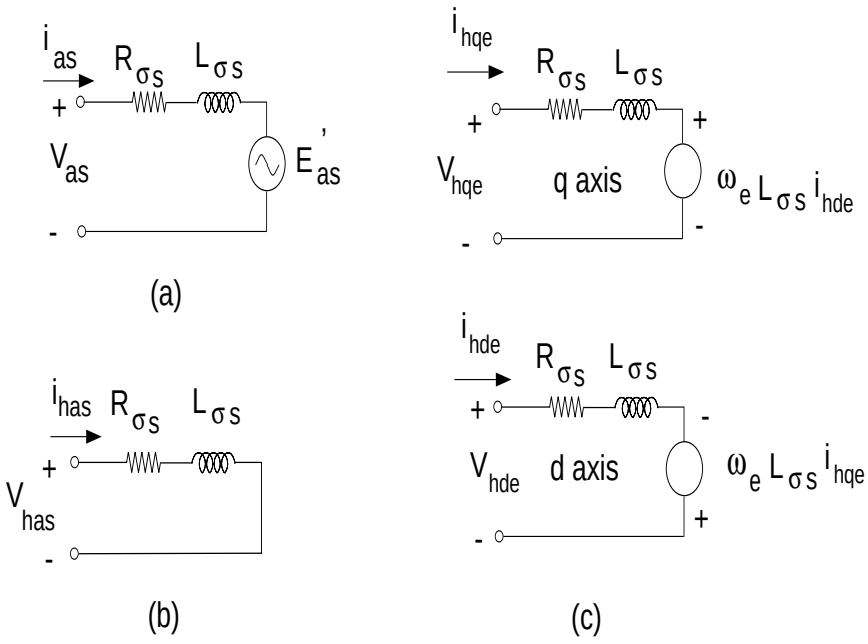

Figure 5.47: Three phase AC induction motor transient and harmonic equivalent circuits; (a): Per phase fundamental component transient model, (b): Per phase harmonic model, (c): Harmonic model in the synchronous frame.

Therefore, the difference between the original modulation signal and the output modulation signal equals the overmodulation harmonic voltage. In case of inaccurate inverse gain compensation, the estimation will include a fundamental component also. Therefore, additional filtering to block the fundamental component voltage is required for accurate harmonic voltage estimation. As will be shown in the simulations, a single frequency band pass filter (BPF) tuned to the dominant $6f_e$ component and implemented in the $6f_e$ frame provides satisfactory results. In Fig. 5.48 (c), the overmodulation harmonic current, and fundamental component current estimation block diagrams are illustrated. Employing the synchronous frame harmonic equivalent circuit and the estimated synchronous frame harmonic voltages, the overmodulation harmonic currents can be easily computed. Subtracting the estimated harmonic currents from the synchronously sampled and d-q transformed currents, the synchronous frame fundamental component currents can be found. The accuracy of the discussed harmonic current estimation scheme depends on the knowledge of machine parameters. Parameter inaccuracy, computational accuracy, etc. factors can strongly affect the overmodulation harmonic current prediction accuracy. However, at this stage the accuracy and implementation issues of the overmodulation harmonic current prediction algorithm will be omitted.

The overmodulation harmonic feedback current reduced current controller scheme has been simulated to illustrate its superior steady state overmodulation performance. The same load, inverter, and controller parameters as the previous case are assumed. The overmodulation harmonic estimator computes

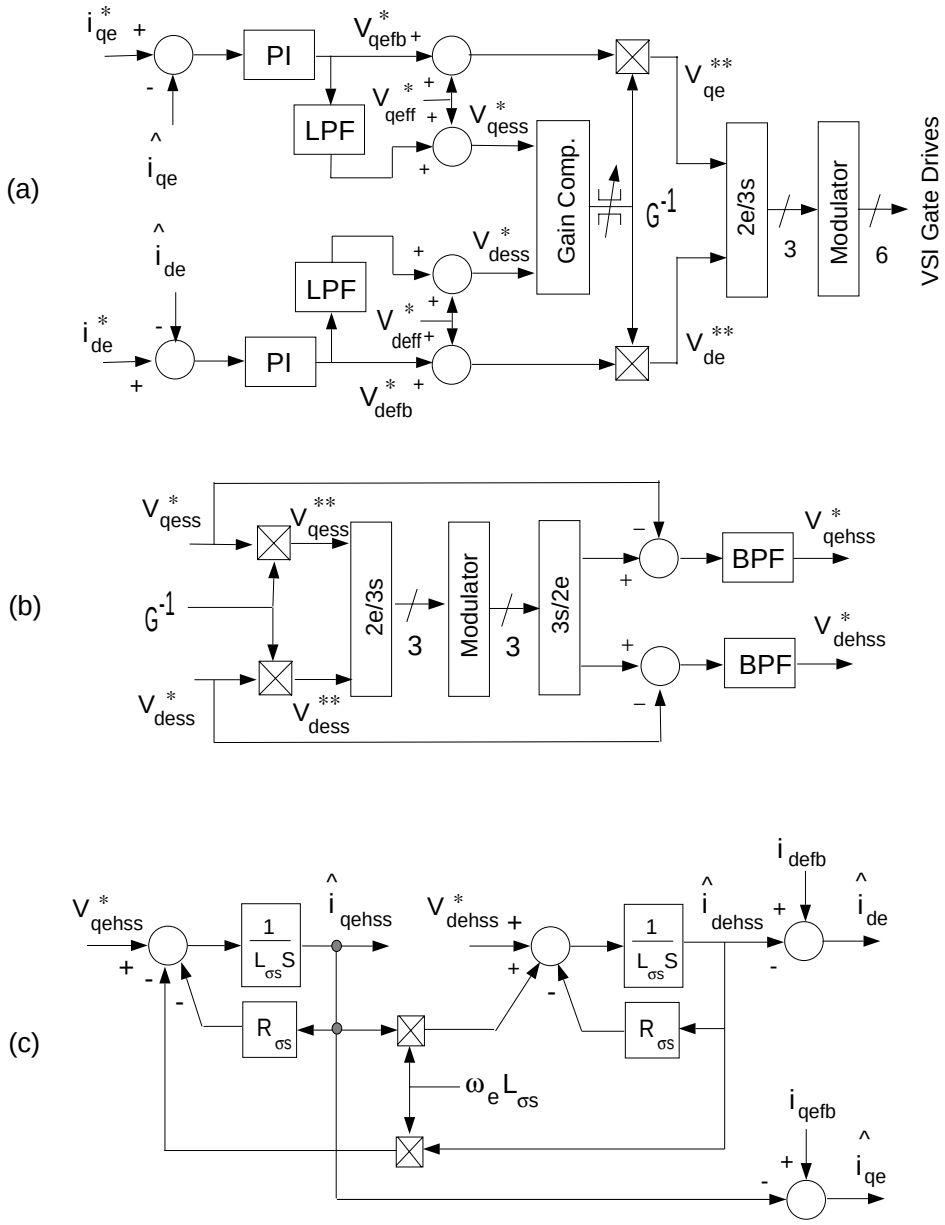

Figure 5.48: The SFCR drive with overmodulation harmonic estimation algorithm. (a): Current regulation algorithm including the gain compensation block, (b): Overmodulation harmonic voltage estimation block diagram, and (c): Overmodulation harmonic current estimation block diagram.

the signals once per carrier cycle. Once the reference voltage signal is computed (at the beginning of the cycle), the estimator predicts the harmonic current value at the end of the associated carrier cycle. Figure 5.49 shows the simulation waveforms of the harmonic reduced system. The system is operated at 0.933 modulation index(at $t = 0$ all the currents are zero) for 0.1 s. Then the d axis current reference is stepped to a value corresponding to 0.965 modulation index. As the figure indicates the current regulator provides improved steady state current waveform. With the absence of the dominant overmodulation harmonics from the feedback, the PI controller output signals are less oscillatory and the operation is less oscillatory. Zooming into the figure, it can be seen in Figure 5.50, the synchronous frame d-q axis discretized currents are not as oscillatory as the previous case (Fig. 5.45). Including more detail, the waveforms in Fig. 5.51 indicate the steady state performance superiority of this controller. The modulation waveform has quarter-wave symmetry and the phase currents are more sinusoidal than the previous case.

This section illustrated high performance SFCR based drives have significant performance issues in the overmodulation region. Without PI controller antiwindups, current controllers exhibit poor steady state and dynamic performance in the overmodulation region. Employing antiwindups on the PI current controllers aids manipulating dynamic overmodulation conditions without significant current oscillations. Steady state operation of an SFCR based drive with or without antiwindups in the overmodulation region results in higher

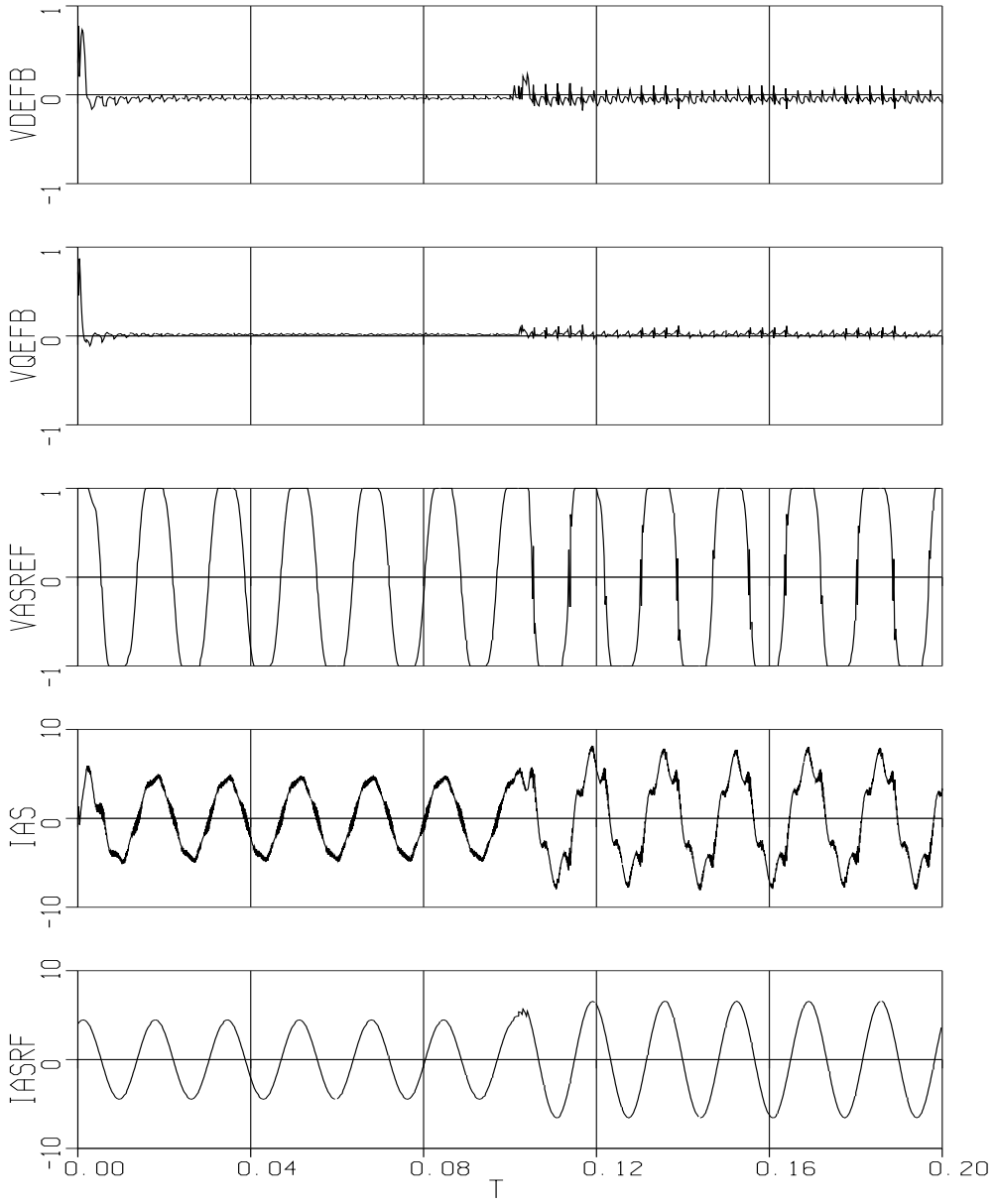

Figure 5.49: Harmonic feedback reduced, SFCR based drive simulation waveforms in the overmodulation range. Traces (bottom to top): reference phase current, actual phase current, modulation wave, q and d axis PI controller outputs. At $t = 0.1s$, the modulation index is increased from $M_i = 0.933$ to $M_i = 0.965$.

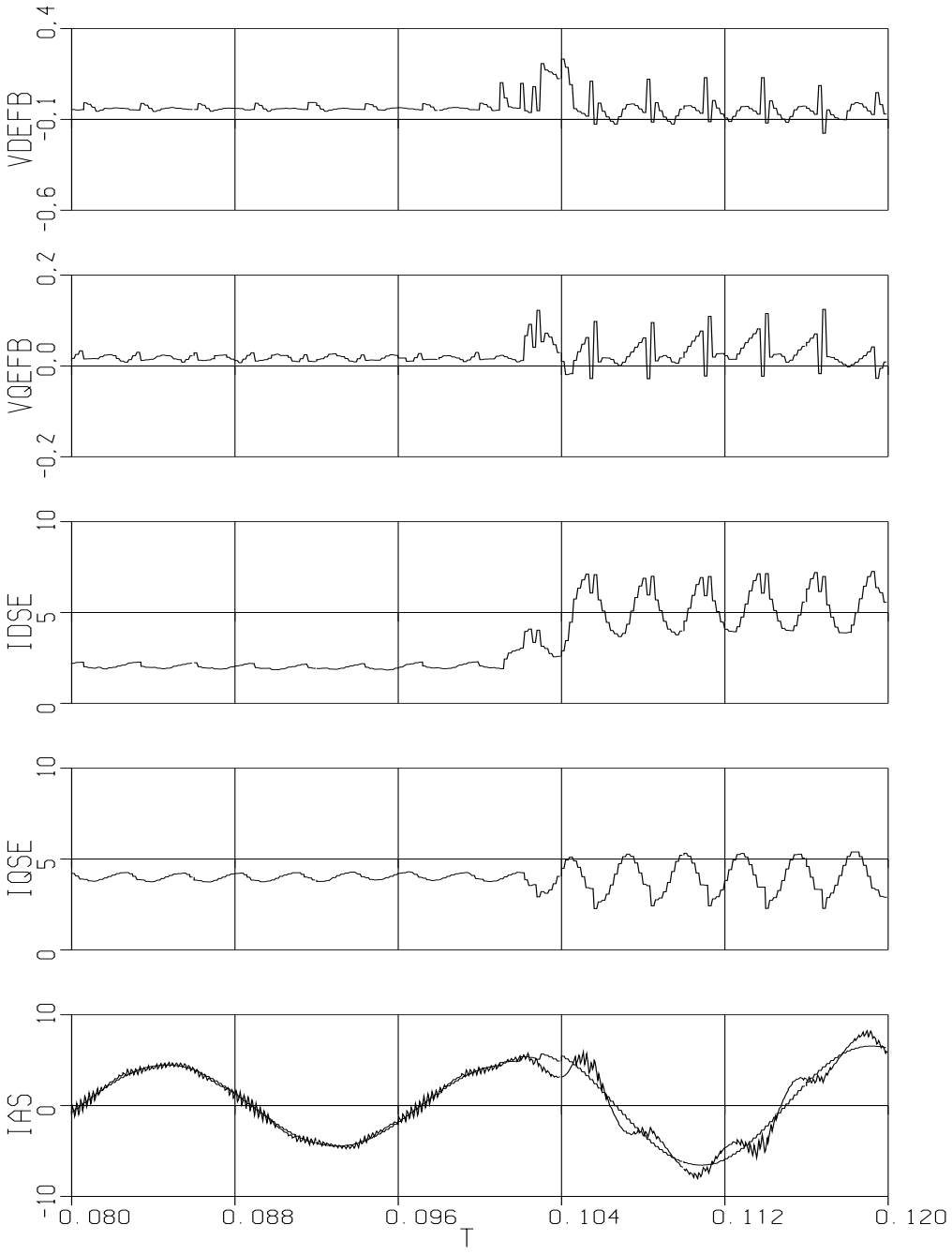

Figure 5.50: Detailed view of the system characteristic waveforms in the overmodulation range. Traces (bottom to top): reference and actual phase currents, discretized q and d axis currents, q and d axis PI controller outputs.

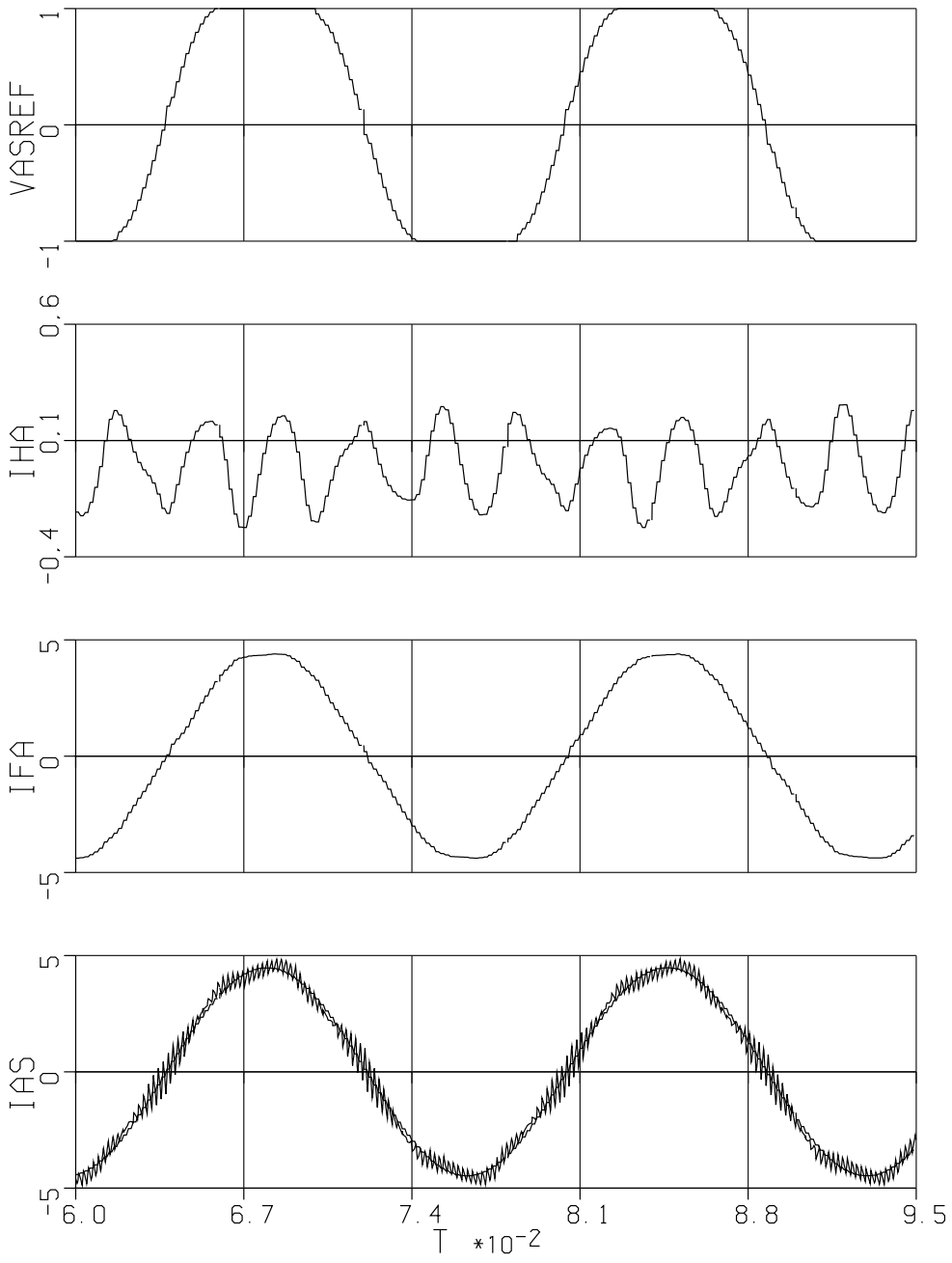

Figure 5.51: Zoomed view of the phase current and modulation wave at $M_i = 0.933$. Traces (bottom to top): reference and actual phase currents, estimated fundamental component and harmonic currents, and DPWM1 modulation wave.

overmodulation harmonics than voltage feedforward drives for the same operating point. The steady state performance of an SFCR based drive can be enhanced by removing the overmodulation harmonic feedbacks from the controller. However, this approach requires filtering and the dynamic performance reduction due to the introduction of such filters is generally prohibitive. Although the implementation difficulties can be overcome with high performance digital signal processors, the inherent delay of the filters is prohibitive from the performance perspective. As a result, most drives only employ antiwindup controllers and the dynamic performance is retained. Although their presence limits the voltage utilization and steady state operating range of a drive, antiwindups are invaluable for they manipulate the dynamics safely. The simulation study of this section illustrated the poor steady state overmodulation performance characteristics of current controllers and aided in understanding the problem. Therefore, it becomes clear, the overall overmodulation region performance of current controlled drives is limited.

Perhaps, the steady state modulation limit of an SFCR based drive with antiwindup and with a high performance modulator could be estimated by calculating the modulation index corresponding to an operating condition which forces the inverter output vector follow the hexagon sides. This condition corresponds to the minimum (zero) phase error method developed for direct digital PWM overmodulation [58] and illustrated in Fig. 5.6 with the tip point "a" in detail. Projecting the reference voltage vector on the "q" axis of the complex

plane, the q axis AC voltage signal can be found and the fundamental component voltage magnitude can be closed form calculated. Expressed in terms of modulation index, the resulting maximum steady state voltage utilization is as follows.

$$M_{imaxa} = (\frac{\sqrt{3}}{2})ln(3) \approx 0.9514 \tag{5.20}$$

This operating point also corresponds to the practical breakthrough point for the rapid increase of the overmodulation harmonics. Although some applications may require smaller or wider operating range, the authors experience indicates the 0.95 modulation index limit generally represents the rapid performance degradation point and it is the typical performance boundary for many industrial current controlled drives with moderate performance requirements.

5.9 Summary

Dynamic overmodulation and steady state overmodulation issues are different and the modulator fundamental gain characteristics are not a sufficient performance measure to evaluate the dynamic overmodulation performance. An elegant approach is the characterization of the reference and modulator output voltage vector angle and magnitude relations. A simple technique provides analytical tools to obtain these characteristics. Each triangle intersection PWM method is shown to have a unique dynamic overmodulation characteristic. The

investigation reveals the minimum voltage magnitude error dynamic overmodulation attribute (one-step-optimal) of SVPWM method, indicating a significant implementation advantage compared to the two methods reported to achieve such performance. In a motor drive, motion quality is more important than rapid current control and the high performance phase error regulation approach is superior to the inherent overmodulation characteristics of the modern PWM methods. For intermediate dynamic overmodulation performance SVPWM provides satisfactory performance and for high dynamic overmodulation performance a phase error regulation method is adapted from the direct digital PWM technique to enhance the dynamic overmodulation characteristics of the triangle intersection PWM methods. In both methods the antiwindup limiters play an important role in keeping the phase error small and maintaining high dynamic performance. The theoretical modulator dynamic overmodulation characteristics were verified by detailed computer simulations and laboratory experiments.

This chapter also illustrated the steady state overmodulation performance deficiency of current controlled drives. Detailed computer simulation studies illustrated the overmodulation harmonic currents affect the current controller through the feedback channels and the performance degrades. As a result the steady state overmodulation performance of current controlled drives is inferior to voltage feedforward drives. Current controlled drives with antiwindups provide approximately a maximum steady state operating point of 0.95. Although their operating range is narrower than the voltage feedforward drives, current controlled drives manipulate dynamic conditions more rapidly and safer.