Chapter 5

Overmodulation in Current Controlled Drives

5.1 Introduction

The performance of voltage feedforward controlled constant $\frac{V}{f}$ PWM-VSI drives is insufficient for most industrial processes with stringent position, speed, and torque regulation and high dynamic response requirements. Its AC power line and motor load disturbance rejection capability is also poor. Therefore, many applications require higher performance control methods. Electric traction, elevators, textile machines, paper and plastic machines, steel mills, conveyors, cranes, machine tools, etc. belong to the industrial drives category with stringent speed/torque regulation and disturbance rejection requirements. Assembly robots, semiconductor manufacturing, disk drives, cutting machines, etc. belong to the servo drives category and these drives additionally require precise position control, and more stringent regulation. When operated as a regenerative converter, the PWM-VSC interfaces a three phase AC voltage source with a

DC link voltage source. In such applications power flow must be tightly regulated for high performance and safe operation. Therefore, high bandwidth and good disturbance rejection characteristics are required. Three phase UPS applications have similar requirements. In all these applications, PWM-VSI drives employ inner current or flux loops to improve the regulation, dynamic response, and disturbance rejection. With the exception of the DTC methods which employ flux and torque regulators, modern high performance PWM-VSI drives generally utilize current controllers.

In current controlled drives, the current references are generated by the outer control loops (the speed loop of an AC machine or the DC link voltage loop of a PWM-VSC etc.). In tension control applications, the torque producing current reference may be directly obtained by scaling the torque reference (in case of nonlinear torque-current relations, by reading the current reference value from a table etc.) and the flux producing current reference is directly commanded (constant or a function of the motor speed/voltage). Depending on the controller structure involved, the reference currents may be three phase (abc) variables or two phase (d-q) variables. In the latter case, they may be defined in the stationary frame or a rotating frame (typically synchronous frame). Once the reference currents are generated the task of a current controller is to generate a switching pattern for the inverter that will force the load currents follow the reference currents as accurately as possible. However, with the DC link voltage being lmited and variable (due to the finite DC bus capacitor size of most drives) and the switching frequency being finite, the current controller

performance is constrained.

In the carrier based PWM methods, the modulator voltage linearity boundaries may significantly constrain the performance of a current controller. Due to the interaction between the outer loops (speed/position/DC voltage regulation loop etc.), current loop and the modulator, in the overmodulation region the drive performance may degrade significantly. Therefore, the steady state operation of most high performance current regulated PWM-VSI drives is confined to the linear modulation range. However, operation in the overmodulation region may be allowed during transients and in the so called "dynamic overmodulation" region the full voltage capability of the modulator may be utilized to improve the dynamic response. For example, in an induction motor drive, the speed response and robustness to load torque variations and disturbances can be greatly improved. Therefore, the overmodulation region performance issues of current controlled drives deserve a detailed study and thorough understanding.

Since the duration of the dynamic overmodulation transients can be smaller than the minimum fundamental cycle (at the maximum fundamental frequency), the per fundamental cycle modulator characteristics are not appropriate for the investigation of the dynamic overmodulation behavior of a modulator, and the per carrier cycle voltage linearity is important. The dynamic overmodulation characteristics of various direct digital PWM methods were investigated in [88, 131, 58] and various solutions with performance and implementation

complexity trade-offs have been developed. The dynamic overmodulation characteristics of the triangle intersection PWM methods of Fig. 3.7, however, have not been reported and their behavior is not well understood. In this chapter, the influence of the triangle intersection PWM method voltage linearity on the current controller and drive performance will be thoroughly investigated.

Although the focus of this chapter mainly involves the overmodulation region behavior of current loops, a clear understanding of the linear modulation region behavior is necessary for a thorough understanding of the issues. Therefore, the chapter will start with a review of the current regulator operating principles, design, and implementation methods. In particular the fully digital Synchronous Frame Current Regulator (SFCR), which is the wide most recognized current regulation technique (it has zero steady state error and superior dynamic performance) will be reviewed in detail. Following, the current regulator behavior in the overmodulation region will be thoroughly investigated. The direct digital PWM dynamic overmodulation methods will be reviewed. The dynamic overmodulation characteristics of the popular triangle intersection PWM methods will be analyzed in detail. Following the discussion on the influence of these characteristics on the drive performance in various applications, the induction motor drive dynamic overmodulation behavior will be investigated in detail and the correlation between theory, simulations, and laboratory experiments will be illustrated. Finally, the steady state operating performance and voltage limit will be discussed.

5.2 The Synchronous Frame Current Regulator

Shown in Fig. 5.1 in detail, SFCR is the industry standard high performance current control method. In this method, the reference and measured three phase currents are transformed to the d-q coordinates which rotate synchronously with the electrical frequency of the system (the angular speed of the stator flux of a motor, the AC line frequency of a VSC etc.). The transformed currents are compared with their reference values, and the errors are input to PI controllers to generate the synchronous frame feedback voltage references. Voltage feedforward signals and inductive cross-coupling decoupling voltage references are added to the feedback references to form the total d and q axis voltage references. These synchronous frame reference voltages are transformed to the stationary d-q frame and at this stage a modulator is involved in generating the switching device gate signals. In the direct digital modulation technique, the stationary frame d-q voltage references are directly utilized to calculate the switch duty cycles. In the triangle intersection technique, transformation from d-q frame variables to abc variables is required, and then generation of the modulation signals follows. The modulation techniques described in the previous chapters are utilized to generate the switching signals.

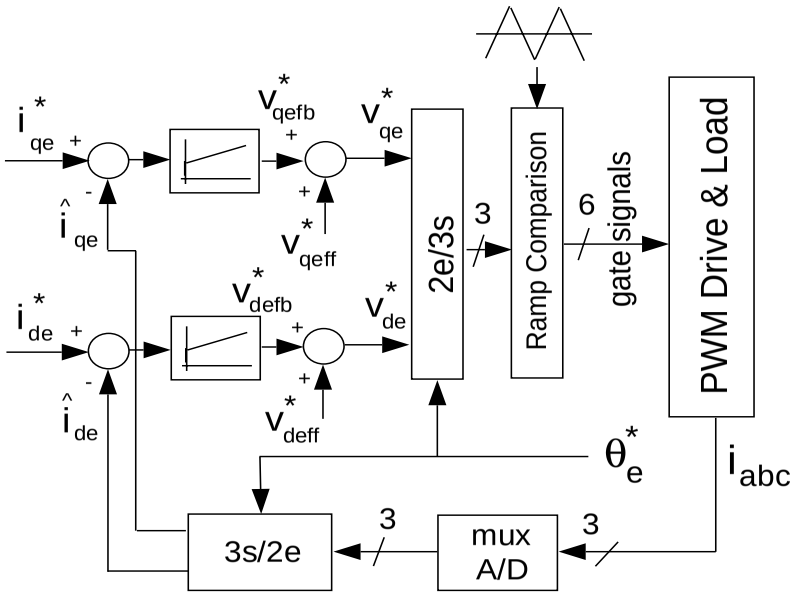

Figure 5.1: High performance drive employing the SFCR algorithm.

At sinusoidal steady state the synchronous frame d and q axis currents become DC variables. Therefore, SFCR yields zero steady state error. The cross-coupling decoupling terms eliminate the coupling between the d and q axis controllers and yield two independent current controllers. The voltage feedforward terms form a direct signal path for the EMF decoupling purpose and therefore enhance the drive dynamic performance. Algorithms and calculations involving the voltage feedforward terms have been discussed in detail in [50]. With the voltage feedforward terms forming the most significant portion of the reference voltage magnitudes, the PI controller output signal range can be retained wide. With a wider PI controller gain choice and wider number range for the integrators, a higher performance drive can be realized.

The SFCR performance is strongly dependent on the implementation method involved. The regulator can be implemented with analog hardware or digital hardware/software. Mostly suitable for analog implementation, its stationary frame equivalent implementation (illustrated in Figure 2.2.b) eliminates the stationary to synchronous frame and backwards coordinate transformations [167]. In the conventional SFCR digital software implementation, however, the coordinate transformations are easily computed. In all the implementations, one important detail is the feedback current measurement technique involved. The feedback current measurement, conditioning and processing methods strongly influence the current regulator steady state and dynamic performance.

In the analog current regulator implementation, the feedback current signals are continuously monitored by the controller. Therefore, the output signals of the PI controllers and the modulation signals continuously vary. However, in order to avoid multiple switchings (more than one switching per device over a half carrier cycle may occur due to noise or system dynamics), a lockout circuit is involved. Following a switching action, the gate signal of each switch retains its position for at least the remaining time interval of the corresponding half carrier cycle. Required for safe thermal and electrical performance, this constraint limits the current controller dynamic response. This limitation on the dynamic performance of the drive can be modeled as a modulator delay and is termed as "PWM delay." As shown in Fig. 5.2(a), in this case the PWM delay is $\frac{T_s}{4}$ (T_s is the carrier wave cycle), the weight center of the half carrier wave. Since the modulation wave is allowed to change once within every

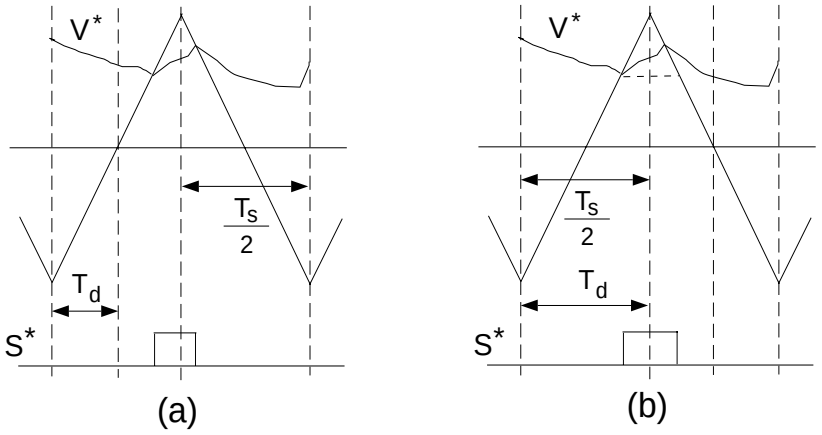

Figure 5.2: Analog current regulator reference, carrier, and gate signal waveforms, and the PWM delay: (a): Asymmetric PWM, (b): Symmetric PWM.

half carrier cycle, typically asymmetric pulse pattern occurs, and this leads to increased steady state voltage and current harmonic content. As shown in Fig. 5.2(b), in order to reduce the harmonic content, symmetric switching can be employed (the first time a switching occurs in a carrier cycle the modulation wave is sampled and held constant until the end of the cycle) at the expense of increasing the PWM delay to $\frac{T_s}{2}$. Although the modulator signal is sampled and held constant, the current regulator proportional and integral components continuously operate on the current errors such that the current controller prime characteristics are not strongly affected. In either case, while in the modulator linearity range, the feedback PWM harmonic currents only slightly influence the drive performance, and the switching frequency harmonic content may slightly increase. Therefore, the analog implementation of SFCR has high steady state and dynamic performance.

In the digital software implementation, the feedback currents can not be continuously monitored. Instead, the feedback currents or their integral value (charge) over a specific time interval is sampled with an analog to digital (A/D) converter. With the integral value of the switching frequency components (harmonics) of the feedback currents over a carrier cycle (or half carrier cycle) being equal to zero, following a scaling operation on the sampled value (dividing the integral value by the time interval) the computed value corresponds to low frequency components (lower than the carrier frequency). During steady state it equals the fundamental component value. This technique is also called the average sampling technique. The method yields high signal to noise ratio. However, in addition to an A/D converter, the integral value sampling technique requires a high accuracy analog integrator and a reset circuit. Therefore, the integral value sampling technique is expensive and most applications employ the simpler and more economical synchronous sampling technique.

In the synchronous sampling technique, the feedback currents are sampled at the positive and/or negative peaks of the triangular carrier signals. With the switching frequency harmonic currents at these instants being negligible, the measurement values correspond to the feedback current low frequency components (at sinusoidal steady state they correspond to the fundamental component). The microscopic harmonic voltage and current waveform sketches of Figure 5.3 aid illustrating this characteristic of inductive loads. How accurately the synchronous sampling method represents the low frequency component depends on the load transient impedance time constant to carrier cycle ratio; the

larger the ratio, the better the approximation. A ratio of 10 or higher (typical) yields satisfactory results. For systems with very small time constant, the synchronous sampling method may not provide sufficiently accurate fundamental component estimation. In such cases, as shown in Figure 5.3 by dashed curves, the harmonic currents are significantly phase advanced with respect to the triangle peak points due to the exponential decay the resistive component of the transient impedance provides. In such applications, the per half carrier or per carrier cycle average value obtained by the integral sampling technique can give a better fundamental component estimate [12, 126]. As previously described, such integral value methods are involved and require dedicated hardware.

Since in the synchronous sampling technique, the feedback current signal is sampled only at specific instants, noise in the system can affect the measurement accuracy to a greater extent than the integral measurement. A/D sampling delays and bit resolution issues can also be other significant limiting factors. However, in most drives the measurement accuracy of the synchronous sampling technique is satisfactory. Therefore this method is widely employed [206]. With proper signal conditioning and low cost and high accuracy A/D converters (10-12 bit) the measurement accuracy meets the demand for most applications.

As shown in Fig. 5.4, when utilizing the synchronous sampling method, the signal is available at the following rates: $\frac{T_s}{2}$, T_s, $2T_s$, ..., NT_s. The figure also illustrates the PWM signal of a phase for the maximum PWM update rate condition. Depending on the controller response requirement, sampling rate

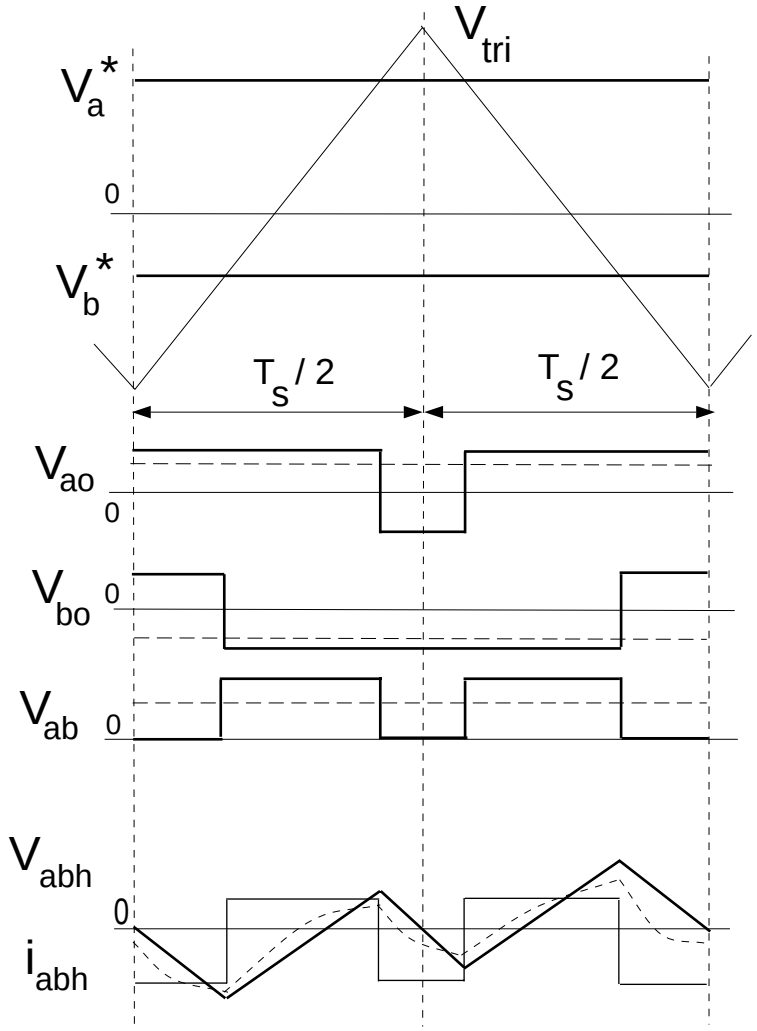

Figure 5.3: Microscopic view of PWM harmonic voltage and current waveforms. In the bottom two plots, the solid lines represent the line to line harmonic currents for purely inductive harmonic model, and the dashed curves illustrate the case with R-L model.

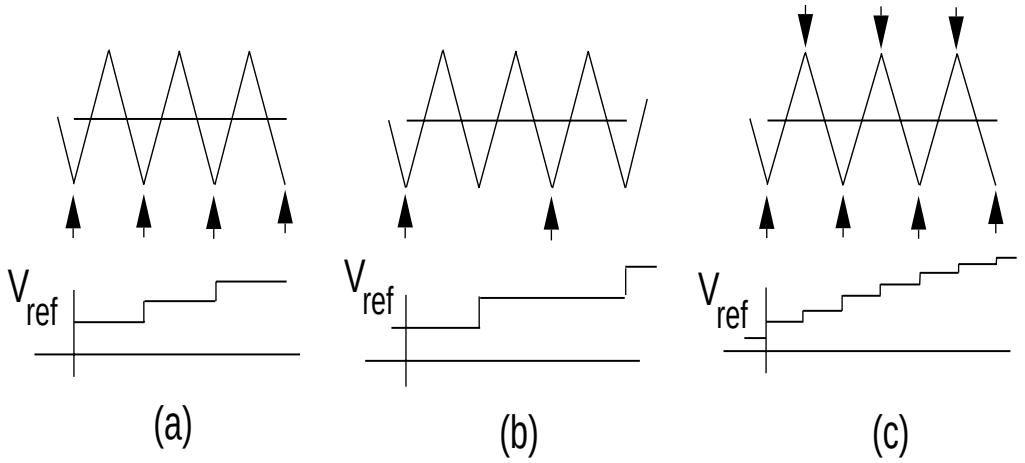

Figure 5.4: Synchronous Sampling Method. (a) : Once per carrier sampling, (b): Half carrier rate sampling, (c): Twice per carrier sampling. Arrows indicate the sampling instants. Bottom traces illustrate the modulation signals with maximum PWM update rate for each sampling case.

available, and processor structure, the most suitable of all the possible sampling rates is chosen. The synchronous sampling technique brings an additional limitation to the digital SFCR dynamic performance. The feedback current sampling rate influences the controller performance as a delay element. Therefore, slower sampling rates imply reduced dynamic performance.

Since in the digital SFCR the feedback current signal is read by the signal processor at most twice per carrier, the controller can at most update the modulation reference waveforms at this rate. As illustrated in Fig. 5.5, the regulator dynamic response is poorer than the analog current regulator case, and its actual value depends on the feedback current sampling rate and measurement method, and PWM write-out rate. As Fig. 5.5(a) indicates, twice per carrier cycle synchronous sampling with twice per carrier PWM signal update rate (the

phase currents are sampled and the PWM signals are output simultaneously at the positive and negative peaks of the triangular carrier wave) result in three-fourth carrier cycle delay (smallest possible). Shown in Fig. 5.5(b), in the more conventional case, once per carrier sampling and update rate (synchronized), the total delay is $1.5T_s$ (from the time the signal is measured, to the first PWM write-out time a T_s time length, and from the PWM write-out time to the weight center of the carrier cycle $\frac{T_s}{2}$). Lower sampling rates and PWM signal output rates imply increased delay and reduced bandwidth. The integral sampling method has an additional latency which equals half the integration time interval. Several feedback current sampling delay compensation methods have been proposed and utilized in applications that the delay degrades the performance significantly [126]. Further improvements on feedback current sampling, signal conditioning, and accurate fundamental component detection have been reported in [12, 39, 73, 184].

As the above discussions indicate, in analog SFCR implementations the PWM delay is small, while in the digital implementation in addition to the PWM delay a feedback signal delay exists. Therefore, with the same controller gains, an analog implementation has superior dynamic performance compared to digital implementation. However, the PWM and feedback current sampling delays are considered second order effects in determining the drive dynamic response and the dynamic performance is mainly determined by the controller proportional and integral gains, integrator limiters and voltage feedforward signals. As all these variables/parameters are practically bounded, both analog

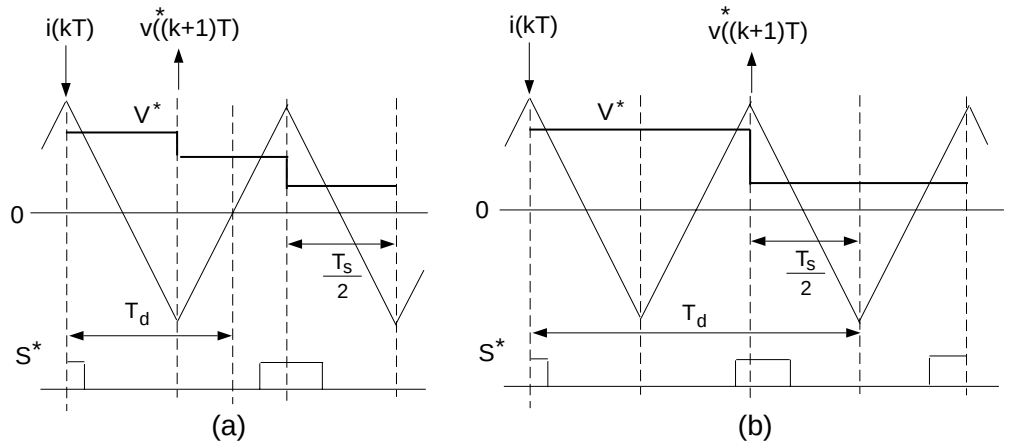

Figure 5.5: Synchronously sampled digital current regulator reference, carrier, and gate signal waveforms, and the delay times: (a): Asymmetric PWM with twice per carrier sampling and PWM write-out rate, (b): Symmetric PWM with once per carrier sampling and PWM write-out rate.

and digital current regulators have finite bandwidth.

The current controller proportional and integral gains are determined by the regulator bandwidth and overshoot requirements. With these performance criteria defined, the controller gains can be easily established analytically or experimentally. Since most PWM-VSI drive applications are electric motors or AC voltage sources (both with R-L-E circuit characteristics), the pole zero cancellation method (also termed as the technical optimum method) provides the best controller performance. The cross-coupling decoupling signals (W*L*I terms) are calculated from the estimated motor parameters, and reference/measured currents. The voltage feedforward terms also require the measured/estimated load parameters/variables. The controller integrator limits are selected as high

as possible so that during a significant transient the controller linearity is retained. With all the components designed carefully, the SFCR performance meets the bandwidth and overshoot requirements of most industrial and motion control applications. With zero steady state error and rapid dynamic performance from zero frequency to the maximum operating frequency, SFCR provides high performance three phase current regulation. Further advanced techniques to obtain high performance from the SFCR (in particular in the high frequency operating region) are discussed in detail in [50]. The performance, however, is only valid in the linear modulation region. Once outside the modulator voltage linearity limit, the current regulator performance experiences significant performance degradation.

The overmodulation region behavior of current controlled drives is complex. In this region the interaction between the control loops (current/speed etc.) and the modulator may result in additional dynamics when compared to the open loop $\frac{V}{f}$ controlled drives. With the modulator being the final element in the cascaded control system, its phase and magnitude error characteristics strongly influence the drive performance. Since the duration of the transients can be smaller than the minimum fundamental cycle (the maximum operating frequency), the per fundamental cycle modulator characteristics (voltage gain) are insufficient and may not be appropriate for the investigation of the dynamic overmodulation behavior of a modulator. The per carrier cycle voltage linearity characteristics are appropriate. Therefore characterization of the modulator reference voltage-output voltage phase and magnitude relations is vital for the

current regulator overmodulation region performance study. The next section reviews the direct digital technique overmodulation magnitude phase relations and then establishes the overmodulation characteristics for the modern triangle intersection PWM methods. Following, the dynamic overmodulation behavior of an AC motor drive is investigated in detail. Finally, the theory is supported with detailed computer simulations and laboratory results.

5.3 Direct Digital PWM Dynamic Overmodulation

Figure 3.4 of Chapter 3 indicates the fundamental component voltage linearity of all the direct digital PWM methods is bounded by the circle which touches the inverter voltage hexagon. The per carrier cycle voltage linearity boundary is the hexagon. However, once the reference voltage vector tip point lies outside the hexagon, (3.13) yields a negative time length, hence an inevitable per carrier cycle volt-seconds error. A voltage vector on the hexagon boundary (the modified reference voltage vector) must be selected and at least one back step has to be taken to re-calculate the vector time lengths that generate the modified reference voltage vector. Shown in Fig. 5.6, the three popular modified reference vector choices are the Minimum Magnitude Error PWM (MMEPWM) method (also called one-step-optimal method) [131, 181], the Minimum Phase Error PWM (MPEPWM) method [58], and the Dynamic Field Weakening PWM

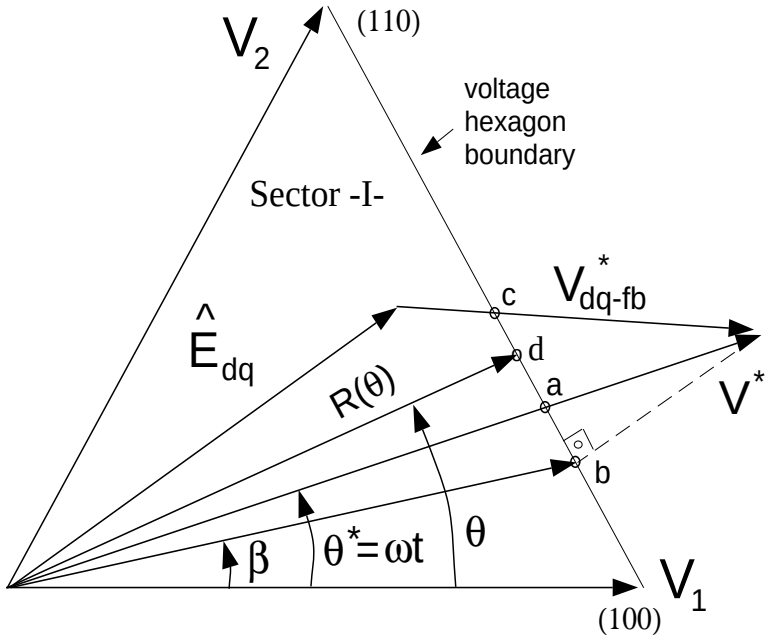

Figure 5.6: Vector space illustration of the popular direct digital PWM technique dynamic overmodulation methods. a: minimum phase error method, b: minimum magnitude error method, c: dynamic field weakening method.

(DFWPWM) method [88, 182]. These methods were evaluated in [88, 182] for induction motor and AC Permanent Magnet (PM) motor drives. The superiority of the last method and the implementation simplicity of the second were shown. The implementation of the first and the third methods is involved (significant computational burden) and the performance of the first is moderate.

In the triangle intersection PWM technique, unlike the direct digital PWM technique, the time lengths of the inverter states are not explicitly calculated: they are an end result of the comparison between the triangular carrier wave

and the modulation waves. Therefore, an overmodulation condition can be detected when the modulation wave signal magnitude exceeds the triangle wave magnitude and switching ceases. The overmodulation intervals, i.e. the time intervals where the reference voltage vectors belong outside the modulator voltage linearity boundaries, exhibit unique voltage error characteristics in each triangle intersection PWM method. These characteristics will be analyzed in detail in the following section.

5.4 Triangle Intersection PWM Dynamic Overmodulation Characteristics

When illustrated in the space vector diagram, the fundamental component voltage linearity boundaries of the triangle intersection PWM methods form circles. As Fig. 5.7 illustrates, the circle radius is smallest in SPWM. SVPWM and all the discussed DPWM methods are linear within the largest circle that fits inside the inverter hexagon. Not shown in the figure, the THIPWM1/6 and THIPWM1/4 methods have linearity circles smaller than the SVPWM circle and larger than the SPWM circle. The THIPWM1/4 circle is smaller than the THIPWM1/6 circle (the diameters can be calculated from the fundamental component linearity modulation indices calculated in the previous chapter). Outside the fundamental component voltage linearity boundaries (circles) the per carrier cycle modulator phase and magnitude characteristics are not well

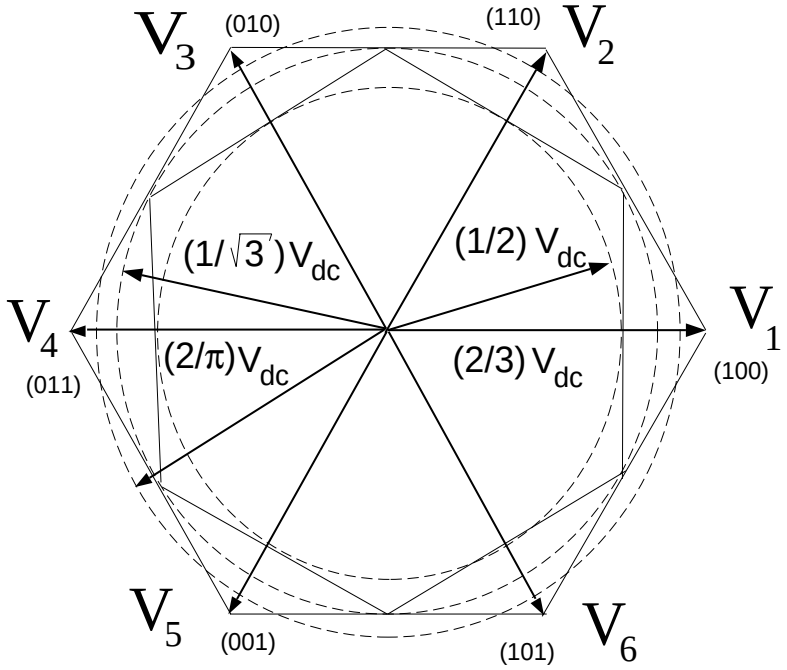

Figure 5.7: Vector space illustration of the PWM inverter voltage linearity limits. The circles illustrate the fundamental component voltage linearity limits.

understood and not reported in the literature.

In the triangle intersection PWM technique, a reference voltage outside the triangle wave boundaries $\pm\frac{V_{dc}}{2}$ can not be generated. Modeling this saturation, dynamic overmodulation characteristics (per carrier cycle phase and magnitude characteristics) of any triangle intersection PWM method can be obtained [65]. With this approach, by passing the reference modulation waves through the limiters shown in Figure 5.8 and employing transformation (3.1), as indicated in Fig. 5.6, for any reference voltage vector $V_{dq}^{*} = \mid V_{dq}^{*} \mid e^{j\theta^{*}}$, an output voltage vector $V_{dq} = \mid R(\theta) \mid e^{j\theta}$ is produced. Since the zero sequence signals of all the popular modulation methods are symmetric and periodic, characterizing the

first sector of the hexagon is sufficient. Note the output voltage vector is the time average value of a sequence of the inverter output voltage vectors applied over a carrier cycle. Time domain waveforms of the d and q axis output voltages can be utilized in calculating the average value of the output voltage vector and its phase relations.

In the SVPWM method and all the discussed DPWM methods, the zero state partitioning may take a zero value, a half, or a unity value. With such zero state partitioning values, the per carrier cycle linearity boundaries of these methods are equal to the linearity boundary of direct digital PWM methods. Therefore, in SVPWM, DPWM0, DPWM1, DPWM2, DPWM3, DPWMMAX, DPWMMIN, and GDPWM the voltage linearity boundary is the inverter voltage hexagon. Since in these methods the hexagon boundaries are known, characterizing the angular relations, $\theta = f(\theta^*, M_i^*)$ is sufficient. For example, in the first sector $R(\theta)$ can be calculated by the following.

$$\mid v_{dq} \mid = R(\theta) = \frac{V_{dc}}{\sqrt{3}\sin\left(\theta + \frac{\pi}{3}\right)} \tag{5.1}$$

The dynamic overmodulation characteristics of the triangle intersection PWM methods shown in Fig. 3.7 have been analyzed with the above approach. The characteristics of SVPWM and all the discussed DPWM methods are summarized in the following, while the SPWM, THIPWM1/4 and THIPWM1/6 characteristics are more involved and will be discussed at a later stage.

In SVPWM, when the modulation signal becomes larger than the saturation

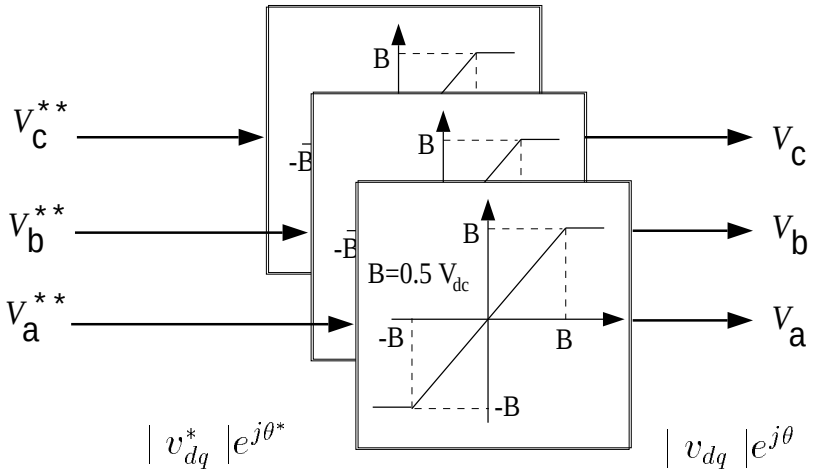

Figure 5.8: The saturation block diagram of the triangle intersection PWM methods.

boundaries $\pm\frac{V_{dc}}{2}$, the saturated modulation signals can be transformed by (3.1) and in the first segment ($0 \leq \theta^* \leq \frac{\pi}{3}$), the output voltage vector angle can be calculated in the following.

$$\theta_{SVPWM} = \arctan\left(\sqrt{3}\frac{1+\frac{6}{\pi}M_i^* cos(\theta^* - \frac{2\pi}{3})}{3-\frac{6}{\pi}M_i^* cos(\theta^* - \frac{2\pi}{3})}\right) \tag{5.2}$$

A software which graphically overlays the MMEPWM, and MPEPWM, and triangle intersection SVPWM dynamic overmodulation reference-output voltage vector trajectories indicated a surprising result: The MMEPWM and SVPWM vectors are exactly the same. Calculated by projecting the tip point of the reference voltage vector on the hexagon side (point b in Fig. 5.6), the analytical angle relation of MMEPWM yields the following formula.

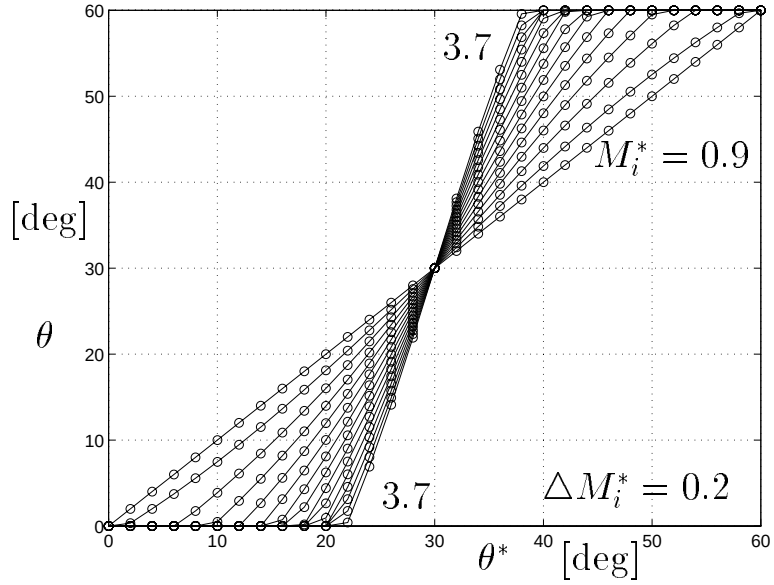

Figure 5.9: SVPWM (-) and MMEPWM (o) $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

$$\theta_{MMEPWM} = \beta = -\frac{\pi}{3} + \arctan\left(\frac{\pi}{2\sqrt{3}M_i^* cos(\theta^* + \frac{\pi}{3})}\right) \tag{5.3}$$

Although (5.2) and (5.3) are different in form, their numerical evaluation which is shown in Fig. 5.9 reveals the fact that their performance is the same. This result indicates when implemented with the triangle intersection technique, the SVPWM method provides very fast (one step optimal) dynamic overmodulation response. The MMEPWM methods employed in practice are complex and computationally involved [131, 181]. The triangle intersection SVPWM, however, can be implemented in hardware or software with minimum complexity.

In the SVPWM method two modulation signals always have the same magnitude and opposite polarity. Furthermore, these phases always have larger magnitude than the third. Therefore, in the overmodulation at least two modulation signals saturate simultaneously. In addition to aiding the explanation of the phase lag (in the first half of the first inverter hexagon segment) and phase lead (in the second), these characteristics appear to be the reason for the one-step-optimal overmodulation behavior. Perhaps, this characteristic can be proven by rigorous algebra. However, with the numerical results being satisfactory and illustrating the importance of this characteristic, no serious attempt is made towards a mathematical proof of this claim.

The DPWM methods of which their waveforms were shown in Fig. 3.7 have found application in high performance current controlled drives due to their low switching loss characteristics and low current ripple characteristics [62, 68]. Dynamic overmodulation characteristics of these modulators can be modeled depending on their zero state partitioning which was summarized in Fig. 3.9. A zero state partitioning of $\zeta_0 = 1$, which corresponds to DPWM0 and DPWMMIN in the first hexagon sector, provides the following phase relations.

$$\theta_{DPWM0} = \arctan\left(\frac{\frac{6}{\pi} M_i^* \sin\theta^*}{2 - \frac{2\sqrt{3}}{\pi} M_i^* \sin\theta^*}\right) \tag{5.4}$$

For DPWM2 and DPWMMAX the zero state partitioning in the first hexagon sector is zero ($\zeta_0 = 0$) and the dynamic overmodulation angle relations are calculated as follows.

$$\theta_{DPWM2} = \arctan\left(\sqrt{3}\frac{1 - \frac{2\sqrt{3}}{\pi}M_i^* \cos\left(\theta^* + \frac{\pi}{6}\right)}{1 + \frac{2\sqrt{3}}{\pi}M_i^* \cos\left(\theta^* + \frac{\pi}{6}\right)}\right) \tag{5.5}$$

Since in DPWM1 the zero state partitioning is $\zeta_0 = 0$ for $0 \leq \theta^* \leq \frac{\pi}{6}$ and $\zeta_0 = 1$ for $\frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3}$, the overmodulation phase relations are calculated from (5.4) and (5.5) in the following.

$$\theta_{\text{DPWM1}} = \begin{cases} \theta_{DPWM2} & 0 \leq \theta^* \leq \frac{\pi}{6} \\ \theta_{DPWM0} & \frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3} \end{cases} \tag{5.6}$$

The dynamic overmodulation characteristics of DPWM3 are found with the same approach in the following.

$$\theta_{\text{DPWM3}} = \begin{cases} \theta_{DPWM0} & 0 \leq \theta^* \leq \frac{\pi}{6} \\ \theta_{DPWM2} & \frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3} \end{cases} \tag{5.7}$$

The following phase error, $\triangle\theta$, definition aids the discussion on the modulator dynamic overmodulation characteristics.

$$\triangle\theta = \theta^* - \theta \tag{5.8}$$

The reference and output voltage vector phase relations of DPWM0, DPWM1, DPWM2, and DPWM3 are shown in Figures 5.10, 5.11, 5.12, and 5.13 for various M_i^* values. In DPWM0 the output vector always leads the reference voltage

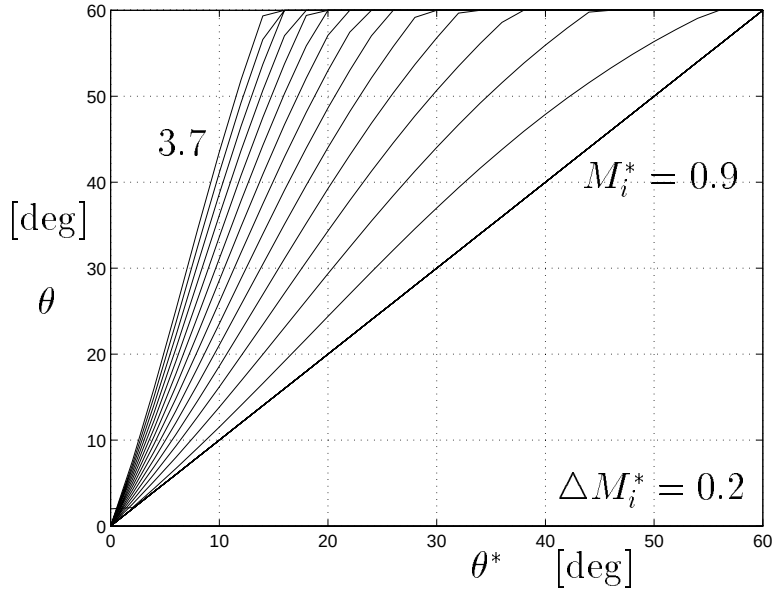

Figure 5.10: DPWM0 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 1$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

vector while for DPWM2 the opposite is true. Since DPWM1 is a combination of DPWM0 and DPWM2, in this case the output vector lags the reference for the first 30° segment of the sector and leads in the following 30° segment. Note the phase error of SVPWM also changes polarity at 30°, however the change is smoother and the error magnitude is smaller. As Fig. 5.13 illustrates, DPWM3 follows the opposite pattern of DPWM1 and both in DPWM1 and DPWM3 the output voltage vector experiences a jump near the midsection of the hexagon sector (avoiding the vector at $\frac{\pi}{6}$). For all the discussed methods the behavior in the first 60° is repeated periodically in the remainder of the sectors. In all the methods, an increase in the modulation index results in phase error increase and the error is the largest in DPWM1.

In the SPWM, THIPWM1/4 and THIPWM1/6 methods, the modulator

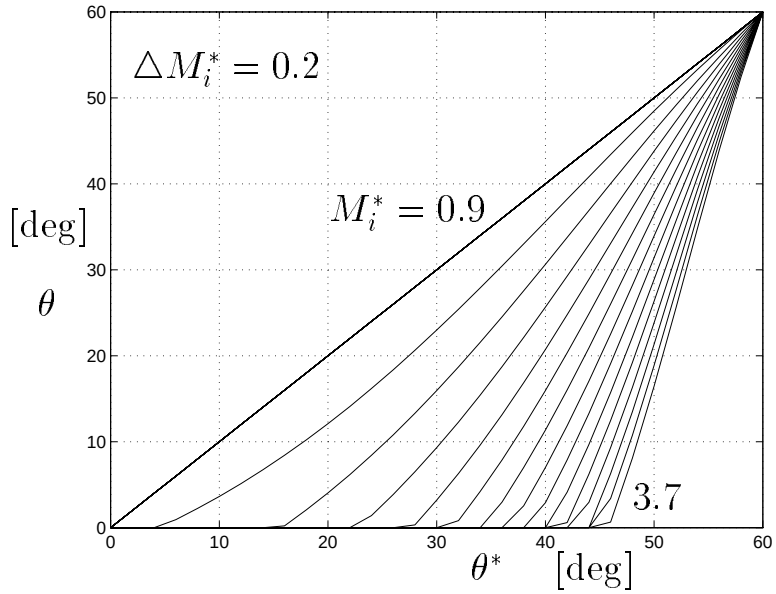

Figure 5.11: DPWM2 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 0$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

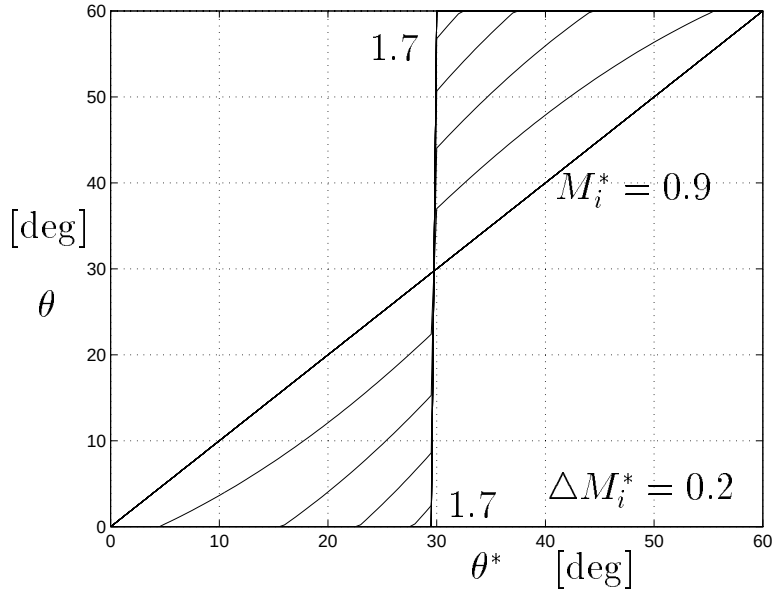

Figure 5.12: DPWM1 $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

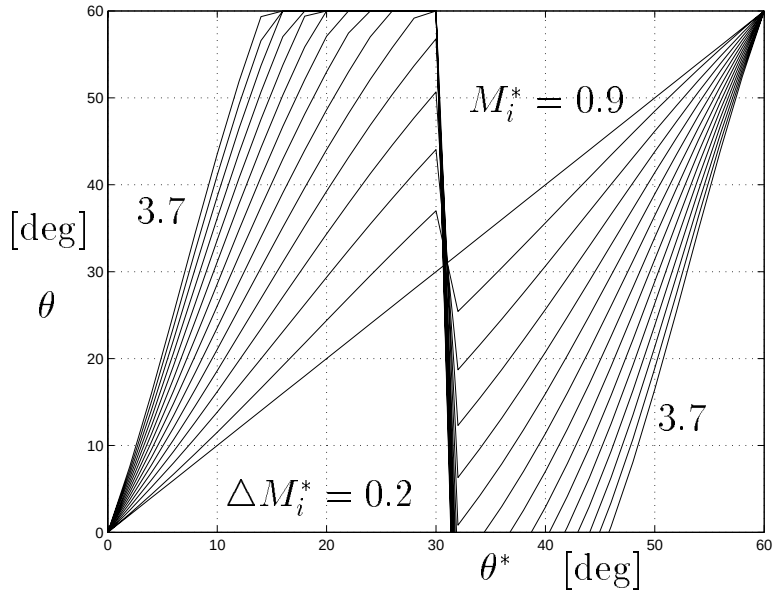

Figure 5.13: DPWM3 $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

phase and magnitude relations are more involved. The per carrier cycle voltage linearity boundaries of these modulators are smaller than the inverter hexagon. These boundaries can be analytically calculated and graphically illustrated. Due to the 60° vector space periodicity, illustration of the boundaries in the first hexagon segment is sufficient. For example, in SPWM the linearity boundaries can be calculated in the following. In the $0° \leq \theta \leq 30°$ segment, phase "a" modulation wave has the largest magnitude. Equating the voltage linearity limit $\frac{V_{dc}}{2}$ to this modulation signal, the voltage linearity boundaries in this region can be easily calculated. In the $30° \leq \theta \leq 60°$ segment, phase "c" has the largest magnitude and determines the linearity boundaries. These relations are summarized in the following.

$$M^{L}_{iSPWM} = \begin{cases} \frac{\pi}{4\cos\theta^*} & 0 \le \theta^* \le \frac{\pi}{6} \\ -\frac{\pi}{4\cos(\theta^*+\frac{2\pi}{3})} & \frac{\pi}{6} \le \theta^* \le \frac{\pi}{3} \end{cases} \tag{5.9}$$

In the THIPWM1/4 and THIPWM1/6 methods the linearity boundaries are calculated in a similar approach, and the results are as follows.

$$M^{L}_{iTHIPWM1/4} = \begin{cases} -\frac{\pi}{4(\cos(\theta^*+\frac{2\pi}{3})-\frac{1}{4}\cos 3\theta^*)} & 0 \le \theta^* \le \frac{\pi}{6} \\ \frac{\pi}{4(\cos\theta^*-\frac{1}{4}\cos 3\theta^*)} & \frac{\pi}{6} \le \theta^* \le \frac{\pi}{3} \end{cases} \tag{5.10}$$

$$M^{L}_{iTHIPWM1/6} = \begin{cases} -\frac{\pi}{4(\cos(\theta^*+\frac{2\pi}{3})-\frac{1}{6}\cos 3\theta^*)} & 0 \le \theta^* \le \frac{\pi}{6} \\ \frac{\pi}{4(\cos\theta^*-\frac{1}{6}\cos 3\theta^*)} & \frac{\pi}{6} \le \theta^* \le \frac{\pi}{3} \end{cases} \tag{5.11}$$

Evaluating the above formulas, the per carrier cycle voltage linearity boundaries of these methods can be found. Figure 5.14 illustrates these boundaries in detail (only the first quadrant of the vector space shown). The internal hexagon is the voltage linearity boundary of SPWM method. The THIPWM1/6 method has elliptic boundaries, while the THIPWM1/4 linearity boundaries resemble the shape of a star with twelve edges. It is apparent from the diagram the per carrier cycle voltage linearity characteristics of these methods are inferior to SVPWM and the DPWM methods. Therefore, SVPWM and DPWM methods are preferred in high performance drives. For the sake of completeness, the non-linear phase and magnitude relations of SPWM and THIPWM methods will be discussed in the following.

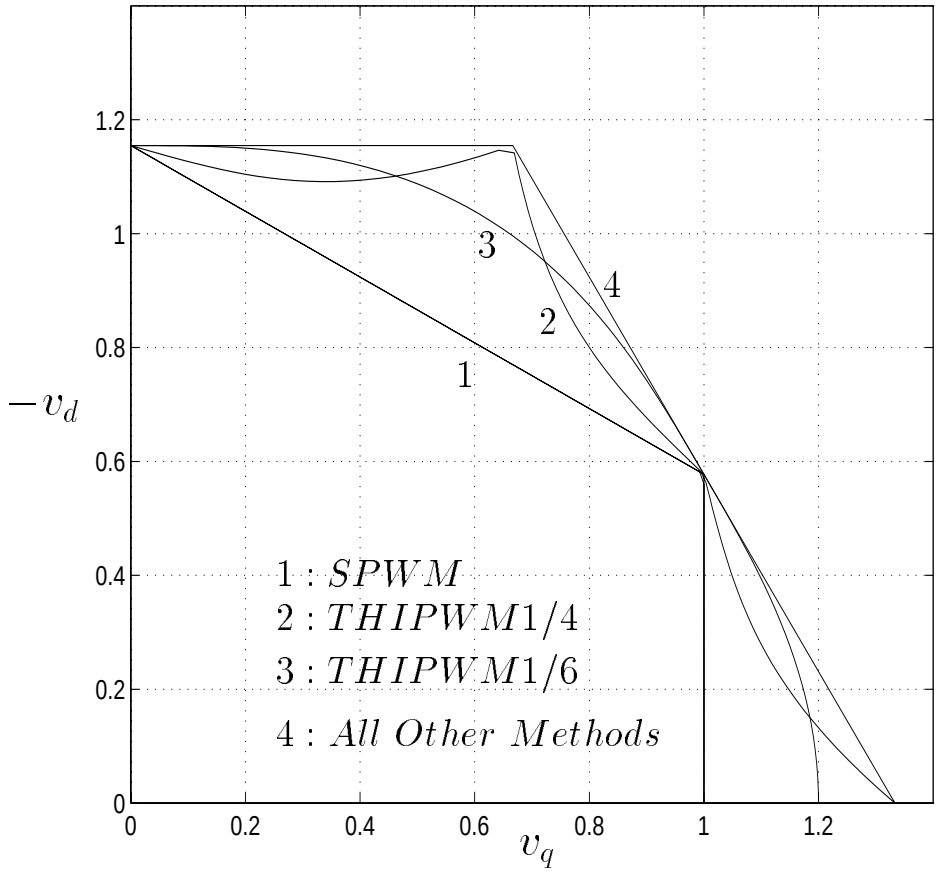

Figure 5.14: Vector space illustration of the modulator per carrier cycle voltage linearity limits. All voltage vectors are normalized to $\frac{V_{dc}}{2}$.

In the SVPWM method, in the overmodulation intervals the modulation waveforms of at least two phases saturate simultaneously. In the DPWM methods, in the linear modulation region one of the three modulation signals clamped to the positive or negative peak of the triangle. In the overmodulation intervals at least one more modulation signal is saturated simultaneously. Therefore, in SVPWM and the DPWM methods overmodulation implies saturation of two phases or three phases. However, in the SPWM and THIPWM methods, a mode with only one phase saturation also exists. For each method and each mode a unique overmodulation phase and magnitude formula exists.

In SPWM, as the modulation signal magnitude increases and becomes larger than $\frac{V_{dc}}{2}$ the one phase saturation mode begins. Further increase in the reference voltage magnitude results in the two phase saturation mode. As the magnitude is further increased the three phase saturation mode is reached. In all the modes the output voltage magnitude is always smaller than the reference voltage magnitude. However, the phase relations are not clear and an analytical investigation is required.

With the reference modulation index defined as a parameter, the dynamic overmodulation phase relations of SPWM can be characterized in three regions. With the SPWM waveforms having space symmetry in a hexagon segment (symmetry about the 30° line), only the first 30° segment need be modeled. The first region covers the $\frac{\pi}{4} \leq M_i^* \leq \frac{\pi}{2\sqrt{3}}$ range and in this region only one phase may saturate (in the first half of the first sector phase "a" saturates). In this region

the phase relations of SPWM are as follows.

$$\theta_{\text{SPWM1}} = \begin{cases} \arctan\left(\frac{3M_i^* \sin\theta}{0.5\pi + M_i^* \cos\theta}\right) & 0 \le \theta^* \le \theta_{b1} \\ \theta^* & \theta_{b1} \le \theta^* \le \frac{\pi}{6} \end{cases} \tag{5.12}$$

$$\theta_{b1} = \arccos\left(\frac{\pi}{4M_i^*}\right) \tag{5.13}$$

The second region covers the $\frac{\pi}{2\sqrt{3}} \le M_i^* \le \frac{\pi}{2}$ range and in this region one or two phases may simultaneously saturate. The relations are calculated in the following.

$$\theta_{\text{SPWM2}} = \begin{cases} \arctan\left(\frac{3M_i^* \sin\theta}{0.5\pi + M_i^* \cos\theta}\right) & 0 \le \theta^* \le \theta_{b2} \\ \arctan\left(\frac{\sqrt{3}(M_i^* \cos(\theta^* - \frac{2\pi}{3}) + \frac{\pi}{4})}{(\frac{3\pi}{4} - M_i^* \cos(\theta^* - \frac{2\pi}{3}))}\right) & \theta_{b2} \le \theta^* \le \frac{\pi}{6} \end{cases} \tag{5.14}$$

$$\theta_{b2} = -\frac{2\pi}{3} + \arccos\left(-\frac{\pi}{4M_i^*}\right) \tag{5.15}$$

The third region covers the $M_i^* \ge \frac{\pi}{2}$ range and in this region two or three phases may simultaneously saturate. The equations are as follows.

$$\theta_{\text{SPWM3}} = \begin{cases} 0 & 0 \le \theta^* \le \theta_{b3} \\ \arctan\left(\frac{\sqrt{3}(M_i^* \cos(\theta^* - \frac{2\pi}{3}) + \frac{\pi}{4})}{(\frac{3\pi}{4} - M_i^* \cos(\theta^* - \frac{2\pi}{3}))}\right) & \theta_{b3} \le \theta^* \le \frac{\pi}{6} \end{cases} \tag{5.16}$$

$$\theta_{b3} = \frac{2\pi}{3} + \arccos\left(-\frac{\pi}{4M_i^*}\right) \tag{5.17}$$

Figure 5.15 illustrates the dynamic overmodulation phase relations of SPWM for various modulation indices. As Fig. 5.15(a) indicates, in the first region, the output vector leads the reference vector in the first 30° segment of the hexagon, and lags in the second 30° segment. However, in this region the phase error is small. As Fig. 5.15(b) indicates, in the second region, the phase error polarity is the same as in the first region. However, the phase error increasingly becomes large. Further increase of the modulation index results in error reduction and as the phase error approaches zero, this region expires. As Fig. 5.15(c) indicates, in the third region, the phase error becomes substantial and in the first 30° segment a lag, in the second a lead occurs. Since at high modulation index values the SPWM and SVPWM modulation signals are similar, in the third region the SPWM phase error behavior approaches the SVPWM phase error behavior. With its phase and magnitude errors being significantly larger than the SVPWM and DPWM method cases, the SPWM method clearly exhibits poor dynamic overmodulation characteristics throughout its overmodulation region.

The phase and magnitude relations of the THIPWM methods can be calculated in a similar manner to the SPWM and SVPWM methods. With its waveform being quite similar to SVPWM, the THIPWM1/6 method has similar dynamic overmodulation characteristics to SVPWM. However, as the fundamental component voltage gain comparisons, and the per carrier cycle voltage linearity boundary comparisons indicated, THIPWM1/6 is slightly inferior to SVPWM and is more difficult to implement. In the region that is outside the THIPWM1/6 ellipse and inside the inverter voltage hexagon the THIPWM1/6

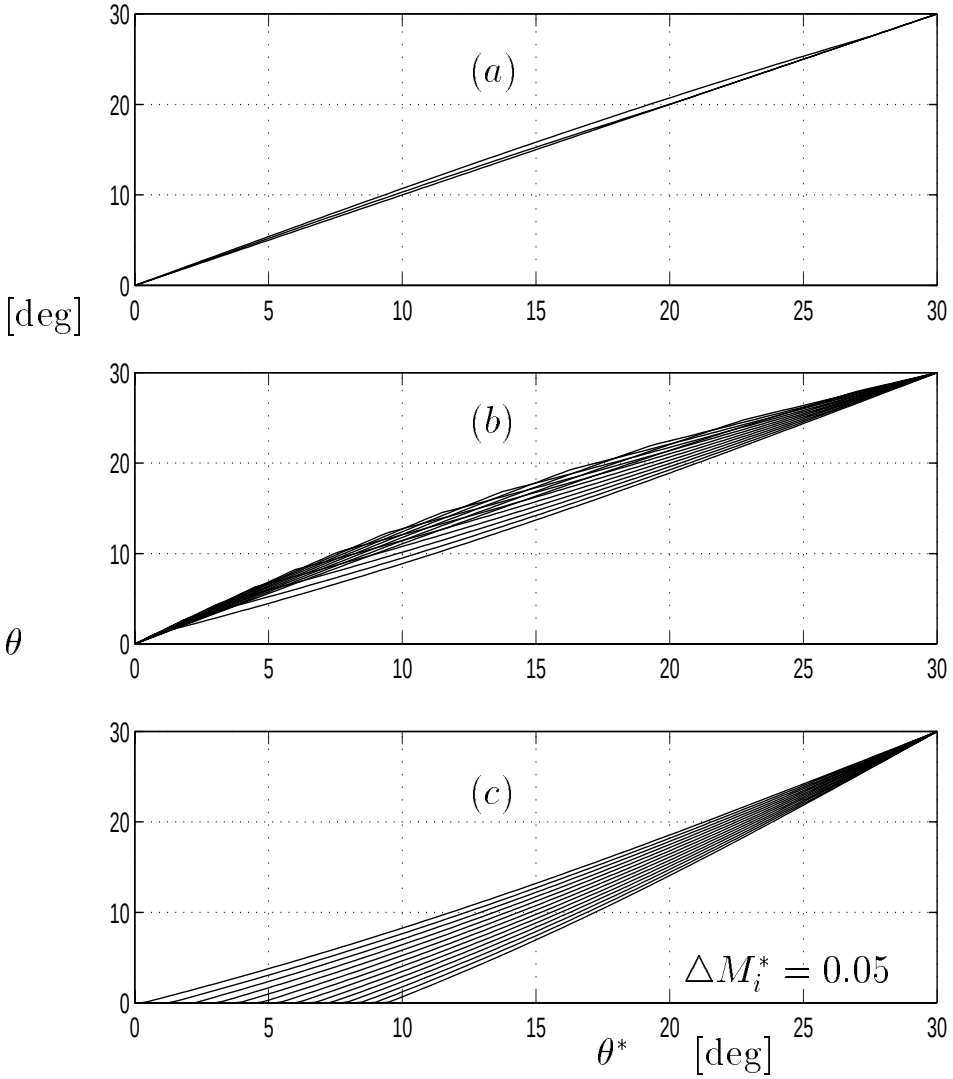

Figure 5.15: SPWM $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.785 and increments with 0.05 units.

has some small phase and magnitude error while SVPWM is linear. Also, outside the hexagon, SVPWM is one step optimal while the THIPWM1/6 is not exactly so. The THIPWM1/4 method has smaller linearity region and its characteristics are inferior to SVPWM and THIPWM1/6. The phase relations of the THIPWM methods will be omitted.

In practice, the theoretical modulator linearity boundaries are further reduced due to the inverter blanking time and/or minimum pulse width constraint of the inverter drives. In the previous chapter it was shown these constraints can strongly affect the fundamental component voltage gain of a modulator. The blanking time and minimum pulse width constraints also affect the dynamic overmodulation characteristics of a modulator. If a narrow voltage pulse is eliminated, the output voltage magnitude becomes larger than the theoretical value and the phase error increases. The phase and magnitude errors are dependent on the minimum pulse width to the carrier cycle ratio and increase with it. Analytical modeling of these second order effects will not be included in this work.

Since the phase error completely determines the dynamic overmodulation performance of a modulator, the $\theta = f(\theta^*)$ (or $\triangle\theta = f(\theta^*)$)relations are the main characteristics in predicting the modulator dependent drive dynamic behavior. The next section discusses the influence of these characteristics on the drive behavior.

5.5 Drive Dynamic Overmodulation Behavior

The dynamic overmodulation performance of an AC motor drive or an AC line connected PWM-VSI is determined by the modulator phase error characteristics, the drive control algorithm, and load characteristics. In the following we first discuss the SFCR design, then investigate the system (SFCR-modulator-load) level overmodulation behavior.

Since the conventional SFCR design assumes modulator linearity, in the overmodulation region significant delays and overshoot can result. The oscillation magnitude may become so large that the drive may become unstable and immediately disabled due to an overcurrent fault. To minimize the performance degradation, antiwindup controllers which bound the integrator outputs of the PI controllers are employed, and selecting a proper integrator limit value is vital in maximizing the dynamic performance [9]. The theory of advanced antiwindup controllers is involved and will be omitted from this work. A relatively simple approach that is based on recalculating the SFCR integrator variables from the output voltage vectors on the modulator voltage linearity boundary [88, 182] has been found adequate for the purpose of the study in this chapter. In this approach, shown in Fig. 5.16, the SFCR discrete time signal flow diagram antiwindup limiters are only activated in the overmodulation region. During the (n)'th carrier cycle, the (n+1)'th cycle reference voltages v_{qe}^* and v_{de}^* are calculated and transformed to stationary frame *"abc"* variables. In the modulator block, a zero sequence signal is injected to the *"abc"* voltages to form

the modulation signals. These signals are passed through the saturation limits of Figure 5.8 and rotated to the synchronous frame to predict the (n+1)'th cycle output voltages v_{qe} and v_{de}. If the reference and output signals are different (indicating a dynamic overmodulation condition), then the antiwindup signals reset the integrators to the boundary values ib_{qe} and ib_{de} (signal flow through "NL"), otherwise the linear modulation operating mode resumes (signal flow through "L"). In the overmodulation region, the "q" and "d" channel integrators are reset to $v_{qe} - v^*_{qeff}$ and $v_{de} - v^*_{deff}$ values so that in the following carrier cycle the calculated reference voltage vector is close to the hexagon boundary. With this approach, if the error reverses polarity, the linearity region is immediately re-entered. If the error is zero or its polarity does not change, then the reference voltage remains near the modulator linearity boundary, however may be at a different point. This intuitive method is apparently simple and has implementation advantage over computationally involved methods.

Along with the modulator and SFCR with antiwindup, the inverter DC voltage source and AC load characteristics define the system overmodulation behavior. Perhaps the most intuitive explanation of the drive behavior is to consider the effect of the phase error on the synchronous frame reference and output voltage vector "d" and "q" components. Depending on the modulator phase error value, during a dynamic overmodulation condition the inverter output voltage vector may lead or lag the reference voltage vector, and the lead and lag conditions result in different "de" and "qe" axis voltages. As a result the drift of the "de" and "qe" axis currents from the reference values may be

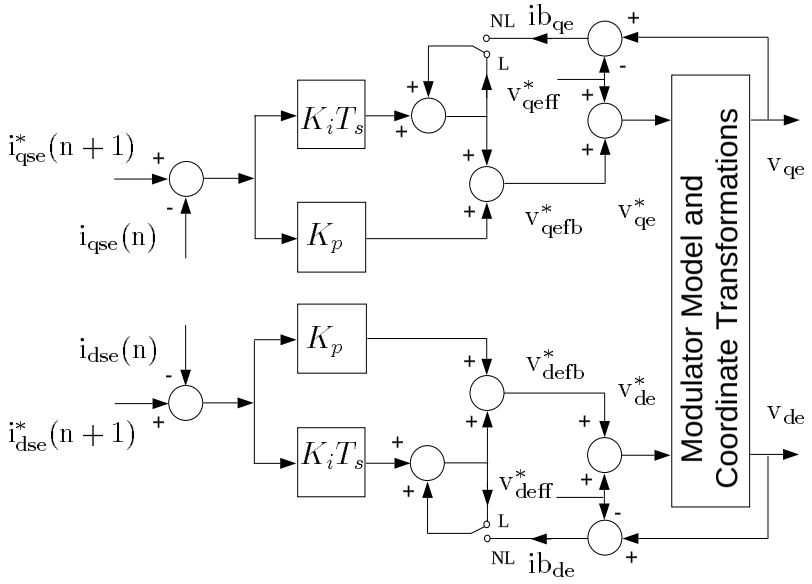

Figure 5.16: Discrete time signal flow diagram of the synchronous frame PI current controller with anti-windup.

quite different in the lagging and leading conditions. Therefore, the currents drift from the reference values according to the modulator phase error characteristics. For example, with SVPWM the drift always yields the smallest current error vector every carrier cycle and therefore SVPWM is suitable for applications where the inverter AC side current error minimization is of prime interest. However, in most cascade controlled motion control systems (from the outmost to the innermost loops, position-speed-current control loops form the cascade control system) the primary goal is to maintain the motion quality. A dynamic overmodulation condition implies an increase in the demanded torque and torque maximization is the prime concern. Since the torque maximization criteria and current error minimization criteria may require two different voltage vectors, the influence of the modulator phase error on the drive motor

torque must be clearly understood. Therefore, the motor dynamic behavior has to be considered. In this work mainly the induction motor behavior will be discussed. However, the dynamic overmodulation behavior of other motor types and utility interfaced PWM-VSI have similar characteristics and the results of this investigation can be interpreted for such applications.

To establish an intuitive background for the drive dynamic overmodulation study, the steady state behavior of the Rotor Flux Oriented (RFO) field oriented induction motor will be briefly discussed first. Then the deviation from steady state and entrance to the overmodulation region will be considered. As shown in Fig. 5.17, during steady state, the reference and output voltages of the RFO-IFOC drive are in phase and they have equal magnitude. The inverter output voltage balances the motor emf and the voltage drop across the equivalent impedance [145]. Since the EMF is on the qe axis and it increases with speed, at higher speeds the qe axis reference voltage becomes significantly larger than the de axis reference voltage. Therefore, as the speed increases the de axis voltage margin decreases and it becomes increasingly difficult to maintain/build the torque producing current. In field/flux weakened AC machines, the flux producing component of the stator current is decreased in a manner to provide a sufficient de axis voltage for torque producing current regulation [99, 100, 180]. As a result, overmodulation is avoided as much as possible. However, field weakened drives with rapid acceleration requirements and including such drives most current controlled motor drives under DC bus and load torque

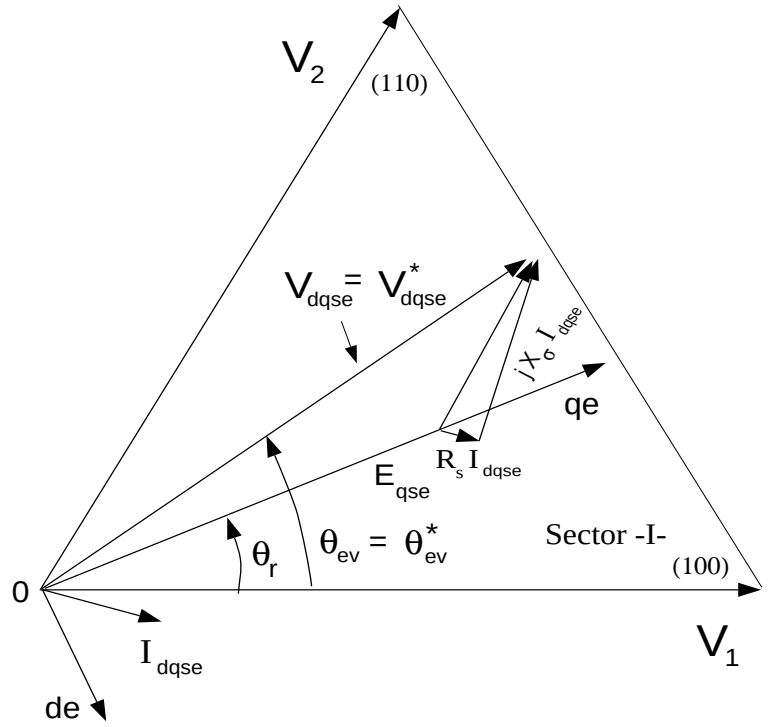

Figure 5.17: Synchronous frame rotor flux oriented induction motor voltage vector diagram illustrated along with the inverter voltage vector diagram.

disturbance conditions enter the overmodulation region and performance degradation results.

As shown in Fig. 5.18, the rotor flux oriented synchronous frame induction motor overmodulation voltage vector diagram indicates during overmodulation condition the "qe" and "de" axis stator voltages are different from the reference values and as a result the "qe" and "de" axis currents drift from their reference values. Thus, the motor torque linearity is lost ($T_e = K_{te}(i_{qse}\lambda_{dse} - i_{dse}\lambda_{qse})$) and motion quality degrades. For example, if v^*_{dqse}, v_{dqse} and the "qe" axis are

in the first 30° segment of a hexagon sector, and v_{dqse} lags v^*_{dqse}, then the overmodulation condition results in a smaller v_{dse} and larger v_{qse} compared to the phase error lead condition. As a result i_{qse} becomes larger and i_{dse} smaller than the lead case. Although this dynamic field weakening condition may transiently increase the drive torque, motion quality degrades due to the loss of torque linearity. As the current regulation becomes poor and the field orientation condition is lost, the rotor flux varies and dynamics are excited. Beyond this point the dynamics can not be described with the steady state equivalent circuit of the motor drive; therefore a full dynamic model is required for a detailed investigation. However, the above discussed simple model illustrates the importance of the modulator phase error and also aids in explaining the influence of the phase lag and lead conditions. The most important conclusion of this intuitive example is that with a strong dynamic field weakening condition or the opposite effect the drive performance may significantly degrade. Therefore, the modulator phase error must be controlled in a manner to maintain good drive performance as much as possible.

Triangle intersection PWM methods exhibit unique phase error characteristics; therefore, it is expected that a drive perform differently with different modulators. Since the current controller antiwindup limiters bound the reference voltage magnitude (i.e. M^*_i), the phase error magnitude is also practically bounded. With the proportional and integral gains of the current controller selected according to the technical optimum criteria, the dynamic overmodulation

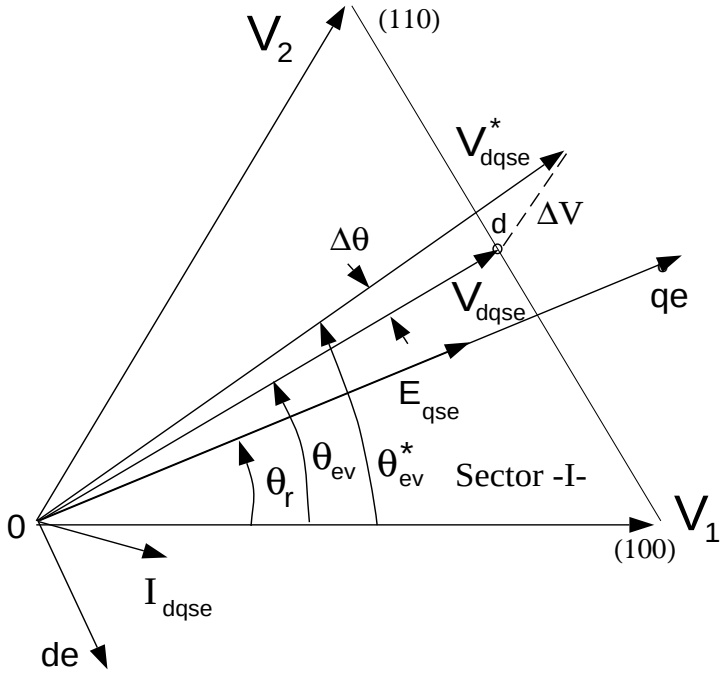

Figure 5.18: Synchronous frame rotor flux oriented induction motor voltage vector diagram representing an overmodulation condition.

conditions can result in reference voltages vectors with a magnitude comparable to the inverter hexagon boundaries. Therefore, the phase errors are also limited by the antiwindups and this limits strong dynamic transients and oscillations. Thus, the antiwindup limiters are essential in avoiding unwanted dynamics. However, the antiwindup limiters may not be sufficient to obtain high performance (any motor torque is a strong function of the phase error and even a small phase error may result in a strong dynamic condition) and a system level study is required. In the following section, detailed induction motor drive simulations address these performance issues.

5.6 Computer Simulations

The theoretical modulator characteristic study has been supported by detailed induction motor drive simulations. A 5 HP, 1745 RPM, 460 V, 6.9 A, 4 pole induction motor with the lumped equivalent circuit parameters of $r_s = 1.97$ Ohm, $r_r = 1.73$ Ohm, $L_{ls} = L_{lr} = 11.2$ mH, $L_m = 275.6$ mH is driven through a PWM-VSI drive. The inverter DC bus voltage is 620 V (stiff DC bus voltage is assumed), and the carrier frequency is 5 kHz. The drive employs an indirect field orientation control algorithm [145], and a fully digital synchronous frame PI current controller with voltage feedforward and antiwindup provides high performance current regulation. The digital current controller employs the synchronous sampling technique with 5 kHz sampling rate (once per carrier cycle feedback current sampling and once per carrier cycle PWM signal

write-out). The current controller bandwidth is 250 Hz. The rated synchronous frame stator "d" and "q" axis currents are $I_{dseR} = 3.38$ A, and $I_{qseR} = 9.12$ A. The drive speed is controlled with a digital PI controller with antiwindup (the previously described antiwindup method) and the antiwindup limit equals the inverter maximum current capability (150 % rated motor current). The speed controller sampling rate is 1 kHz and the speed loop has a 25 Hz (electrical) bandwidth. The drive total inertia is $J_m = 0.05 kgm^2$.

The computer simulation of Fig. 5.19 illustrates the drive linear modulation range dynamic performance with SVPWM. While the drive is operating at 1000 RPM and no load, a transient condition is generated with a speed reference change and application of a load torque. A speed ramp command, ω_r^*, at t=0.65 [s] increases the speed from 1000 RPM to 1050 RPM in 12 ms, and the load torque, T_L, increases at t=0.71 [s] from zero to 25% of the rated motor torque. As the figure illustrates, both the speed regulation and torque disturbance rejection capabilities of the drive are satisfactory. A small overshoot in the speed and torque regulation occurs. However, the error rapidly decays to zero and steady state operation resumes. Since during the transient the modulator remains in the linear modulation region, the influence of the modulator type on the dynamic performance is negligible. Therefore, modulators with the same voltage linearity boundaries as the SVPWM linear modulation boundary (i.e. all the DPWM methods) exhibit the same dynamic performance. For this reason, the linear modulation region dynamic behavior of the DPWM methods is not illustrated and will not be discussed.

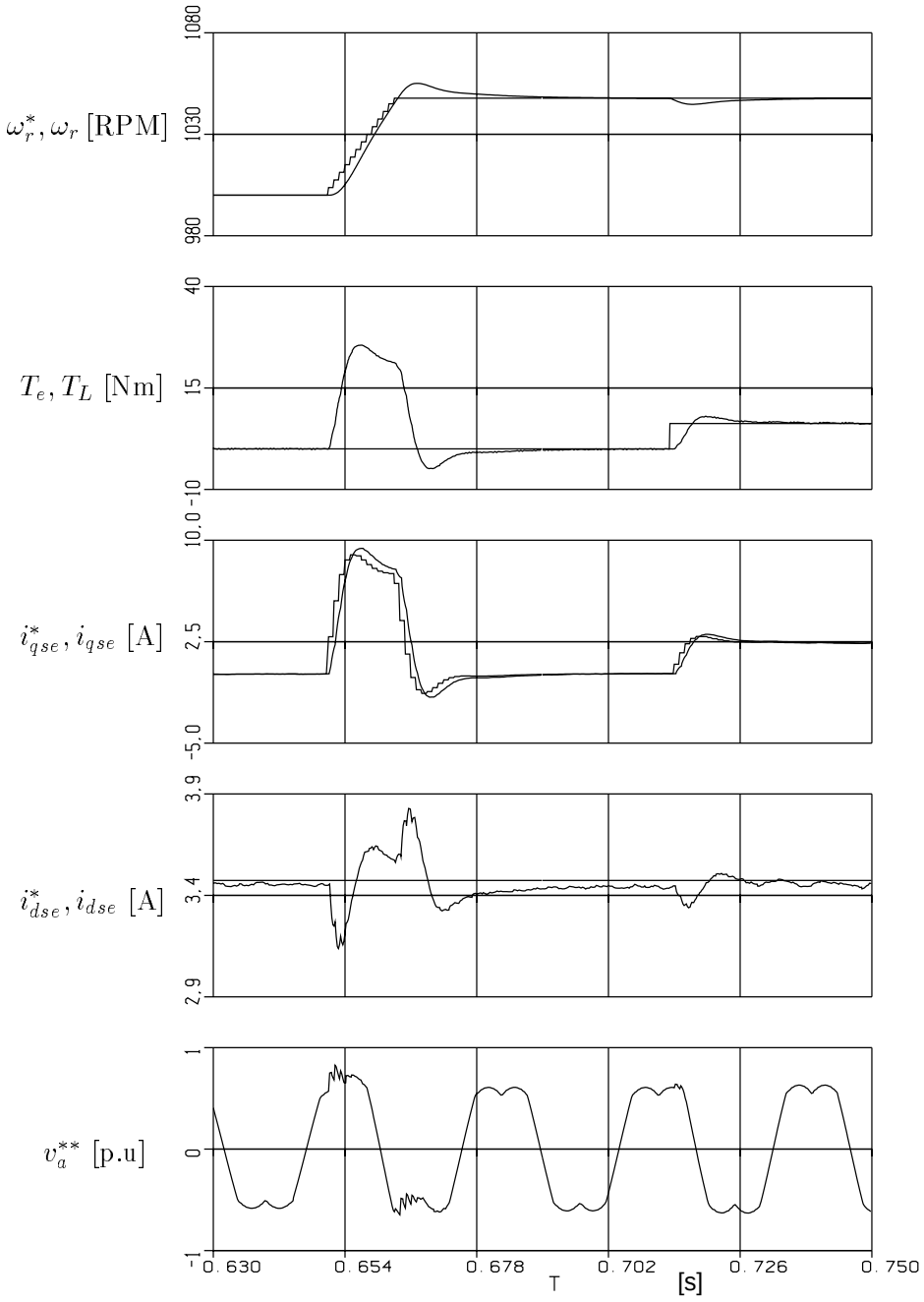

Figure 5.19: Induction motor drive SVPWM linear modulation behavior under speed reference ramp change and load torque step change.

The computer simulations of Figure 5.20 to Figure 5.23 illustrate drive overmodulation performance with various modulators. While the drive is operating at 1500 RPM and no load, an overmodulation condition is generated with a speed reference change and application of a load torque. A speed ramp command, ω_r^*, at t=0.65 [s] increases the speed from 1500 RPM to 1600 RPM in 24 ms, and the load torque, T_L, increases at t=0.71 [s] from zero to 50% of the rated motor torque. Figure 5.20 illustrates the dynamics with SVPWM. The voltage vector phase error polarity and magnitude vary according to Figure 5.9. The current controller antiwindup channels keep the reference voltage vector near the hexagon boundary (M_i^* of (7) is kept small) and the SVPWM method selects a vector close to the reference vector (one-step-optimal) resulting in a small phase error. As Figure 5.20 indicates, SVPWM provides good performance.

Shown in Figure 5.21, the DPWM0 modulated system always has a negative phase error, consistent with the theoretical prediction. As the output voltage vector leads the reference voltage vector more than the SVPWM case, the field current experiences poorer regulation. Although results show an increase in torque and slightly better speed response, the oscillatory behavior can eventually result in a drive failure under certain operating conditions. Shown in Figure 5.22, the DPWM1 modulated system exhibits similar behavior to SVPWM, however its phase error magnitude is larger and the field current regulation capability degrades as in the DPWM0 case. Although DPWM1 has a substantially higher fundamental component gain than the other modulators [64], its

dynamic performance is poorer than SVPWM. Therefore, it becomes clear that the open loop drive overmodulation performance criteria which suggests the modulator with the highest voltage gain is superior to the rest, and the closed loop system dynamic overmodulation performance criteria which suggests the modulator with the best speed response (in speed regulated drives) and disturbance rejection is superior to the rest, are different and result a in different modulator selection.

Shown in Figure 5.23, the DPWM2 modulated system simulations illustrate the dynamic overmodulation performance deficiency of this method. The phase error is large and always positive (lagging); the field current increases and results in reduced torque, hence very poor dynamics. Although in induction motor drive applications the linear modulation range switching loss characteristic of DPWM2 is superior to other modulators [62], its overmodulation performance is quite poor. Therefore, in current controlled drives operation of this modulator in the overmodulation region should be prohibited and further control algorithm modifications are required.

The above simulation results indicate the SVPWM dynamic overmodulation performance is superior to all the other triangle intersection PWM methods. The modulator generates an output voltage vector with a small phase error and its one-step-optimal current regulation characteristic can successfully manipulate most dynamic conditions. However, very low inertia and very abrupt dynamic conditions could still not be properly manipulated and sufficiently large

phase error intervals may result in unstable behavior and unacceptable drive performance. Therefore the modulator choice must be carefully made.

Since the above simulation studies suggest the DPWM methods have poor dynamic overmodulation characteristics and their large phase errors result in strong unwanted dynamics, it becomes inevitable to make modifications to the drive control algorithm when employing such modulators. Since the DPWM methods have superior linear modulation range switching loss and waveform quality characteristics, their utilization in many applications is favorable and a moderate increase in the control algorithm complexity and drive cost can be easily compensated with the performance gain. In this work two modification methods are suggested.

In the first approach, the DPWM method of choice is combined with SVPWM and when a dynamic overmodulation condition is detected, SVPWM is activated while in the linear region the DPWM method resumes control. Figure 5.24 illustrates the drive dynamic behavior with this algorithm. As the simulation waveforms indicate, in the linear modulation region DPWM2 is active, however as a dynamic overmodulation condition occurs the SVPWM signals are activated and the dynamics are rapidly manipulated. Since recent commercial drives often employ SVPWM and a DPWM method in combination to improve the linear modulation range waveform quality (for small M_i SVPWM and for large M_i DPWM is selected) and reduce switching losses [62], the modulation signal generating blocks may already exist in a drive and only an additional

loop and re-calculation of the modulation signals is required. In particular implementing such an algorithm in a DSP based controller is an easy task.

In the second approach a more complex and higher performance algorithm, the dynamic field weakening method can be adapted from the direct digital technique [88, 182]. As shown in Figure 5.6, in this approach, the motor back EMF, $\hat{E}_{dqe}$, (calculated from the estimated stator flux) and the PI current controller outputs V^*_{dqefb}, are vectorially added and the intersection point with the hexagon (point "c" in the figure) is the tip point of the vector that forces the current error vector to move in the controller reference direction. By employing this algorithm, the reference voltage vector which is outside the inverter hexagon, is modified and returned to the inverter hexagon with a corrected phase such that any modulation method will exactly match the modified reference vector. Therefore, the modification algorithm performs equivalently with all the triangle intersection modulation methods. The simulation waveforms in Figure 5.25 illustrate the performance of DPWM2 combined with the dynamic field weakening method. When a dynamic overmodulation condition occurs, the dynamic field weakening algorithm is activated and the reference vector is modified and returned to the hexagon boundary such that DPWM2 exactly generates this vector. Note that this method generates a significantly small phase error and the field current experiences less transients than the SVPWM case. Also note the phase error alternates and during the speed ramp the field current increases for a short time interval. Due to this reason, a better term for the method would be "a phase error regulation method." This method however

is fairly complex and requires substantial amount of calculations for relocating the reference voltage vector. Hence, only suitable for high performance fully digital drives with fast DSP controllers.

It should be noted for rapid torque regulation purposes, the SVPWM method provides a superior dynamic overmodulation response compared to all other methods due to its inherent one step optimal current regulation attribute. However, with SVPWM the rotor flux experiences more oscillations than DFW and under longer dynamic overmodulation transients, the SVPWM torque response superiority is lost.

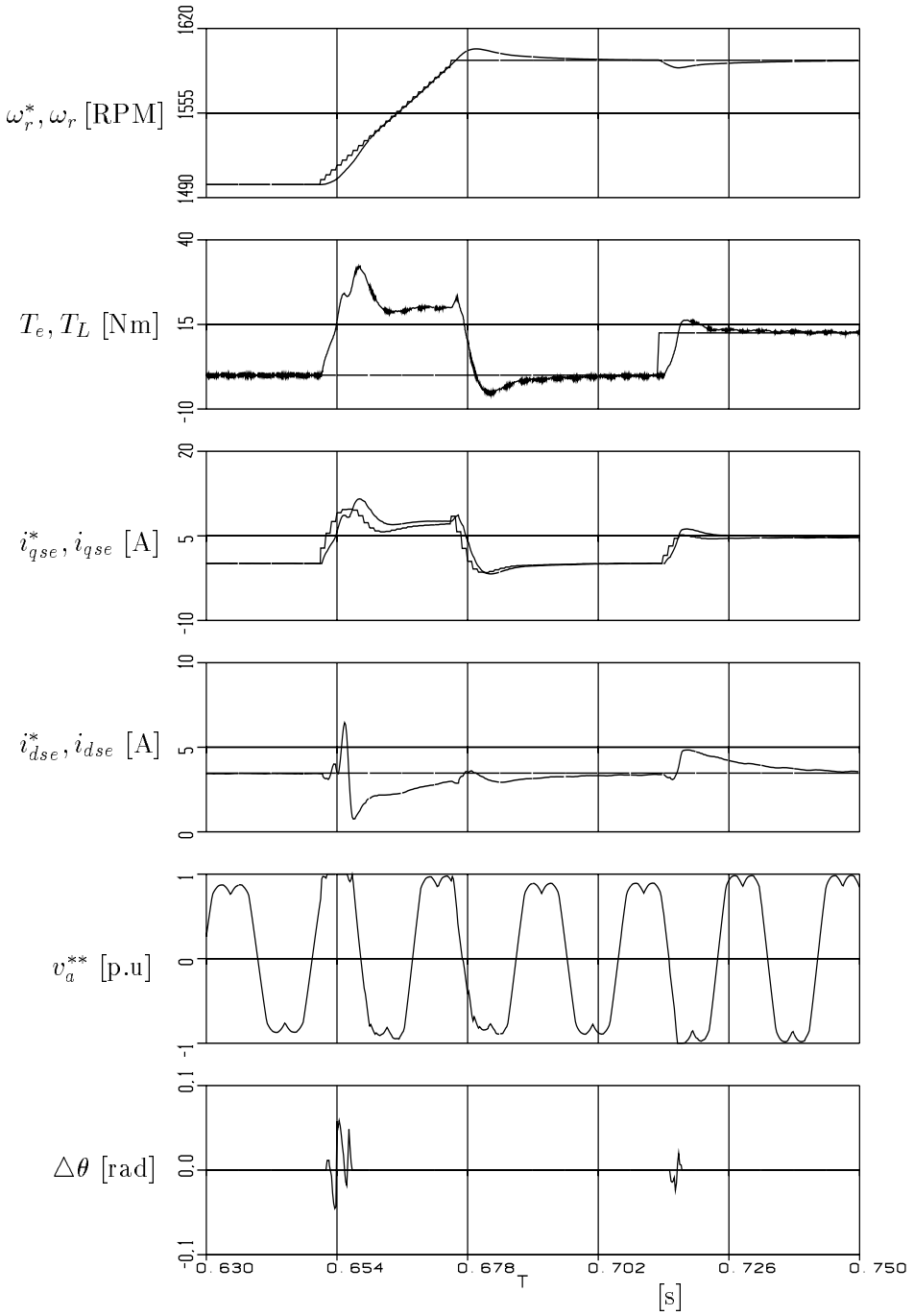

Figure 5.20: Induction motor drive SVPWM dynamic overmodulation behavior under speed reference ramp change and load torque step change.

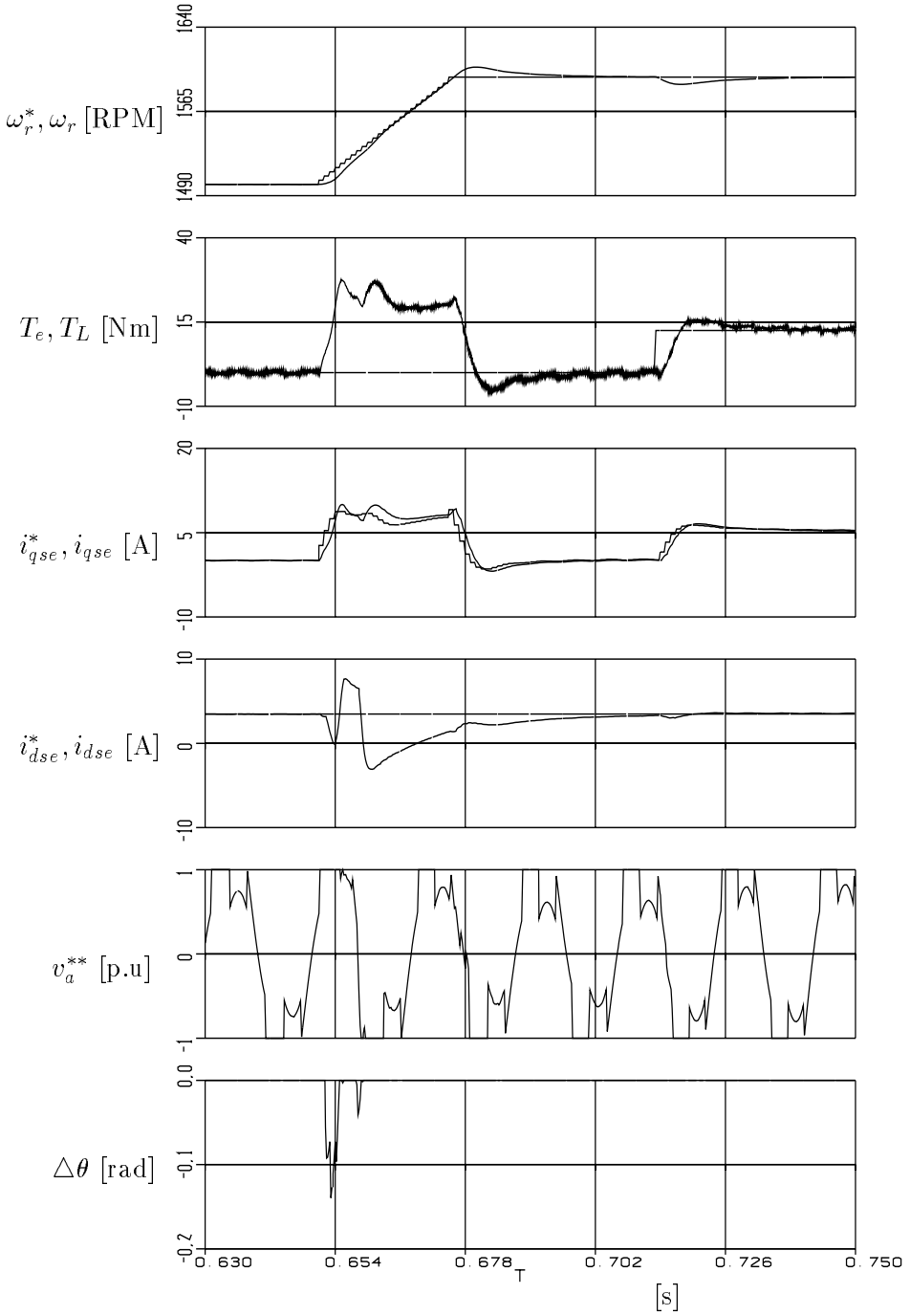

Figure 5.21: Induction motor drive DPWM0 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

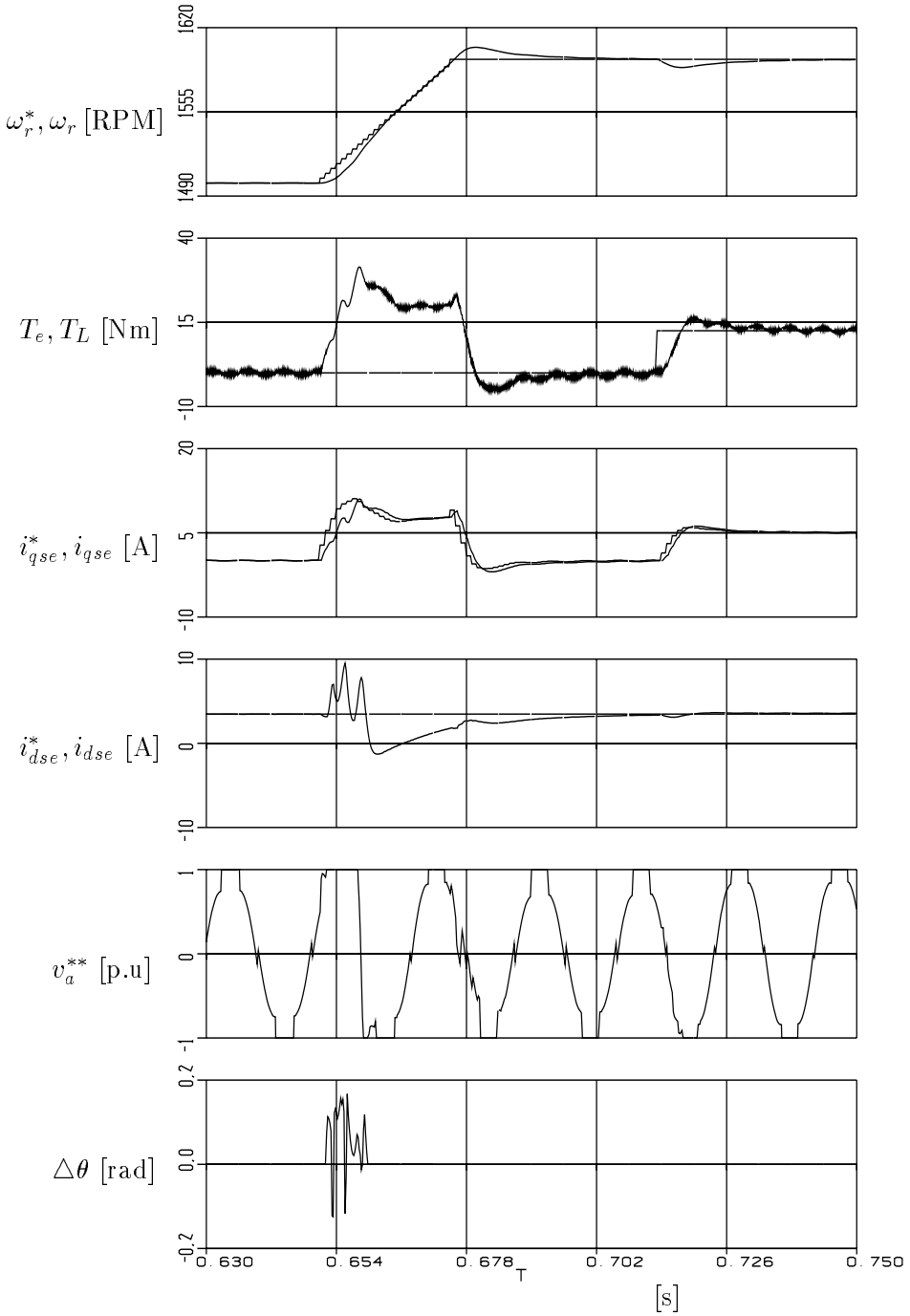

Figure 5.22: Induction motor drive DPWM1 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

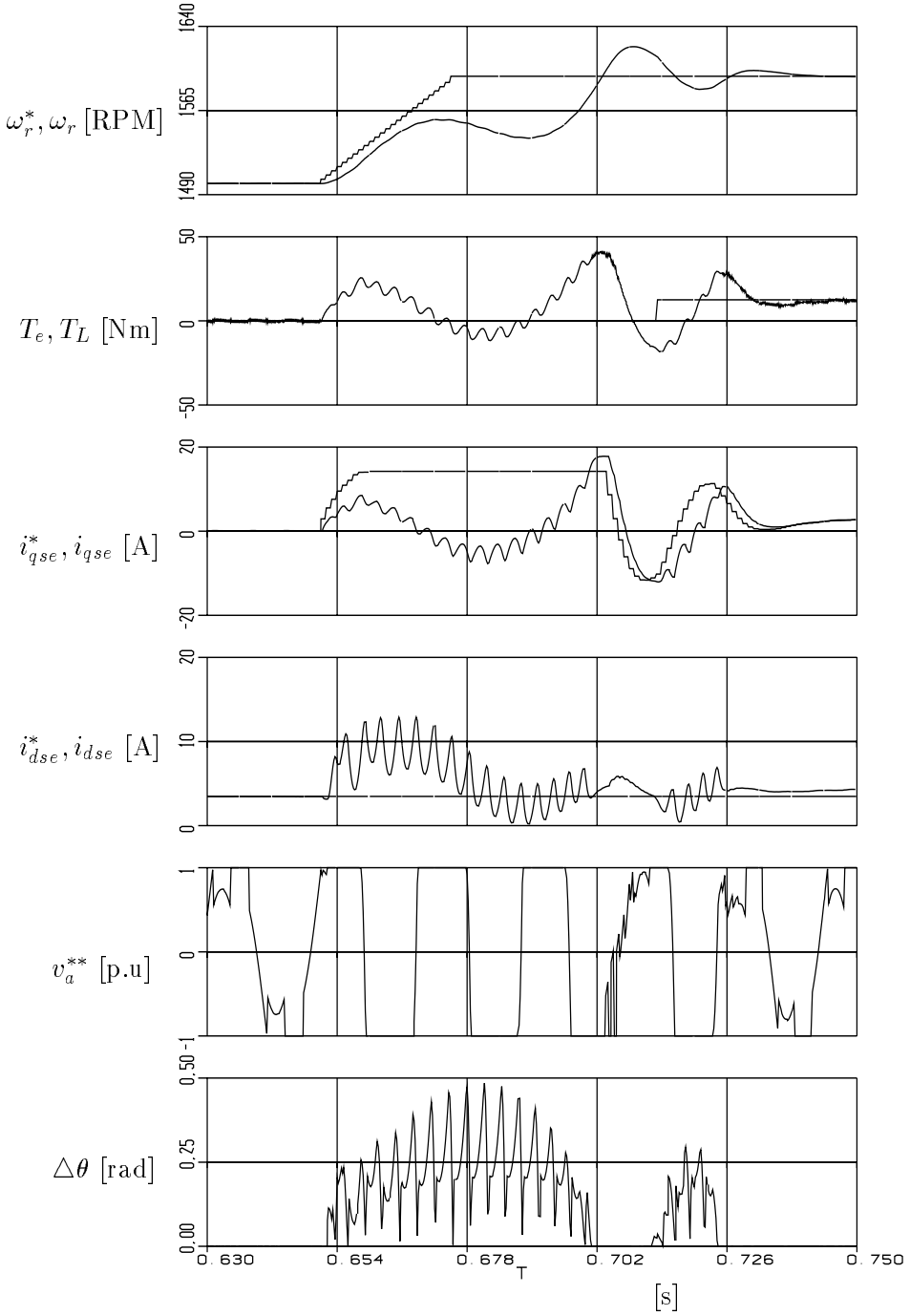

Figure 5.23: Induction motor drive DPWM2 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

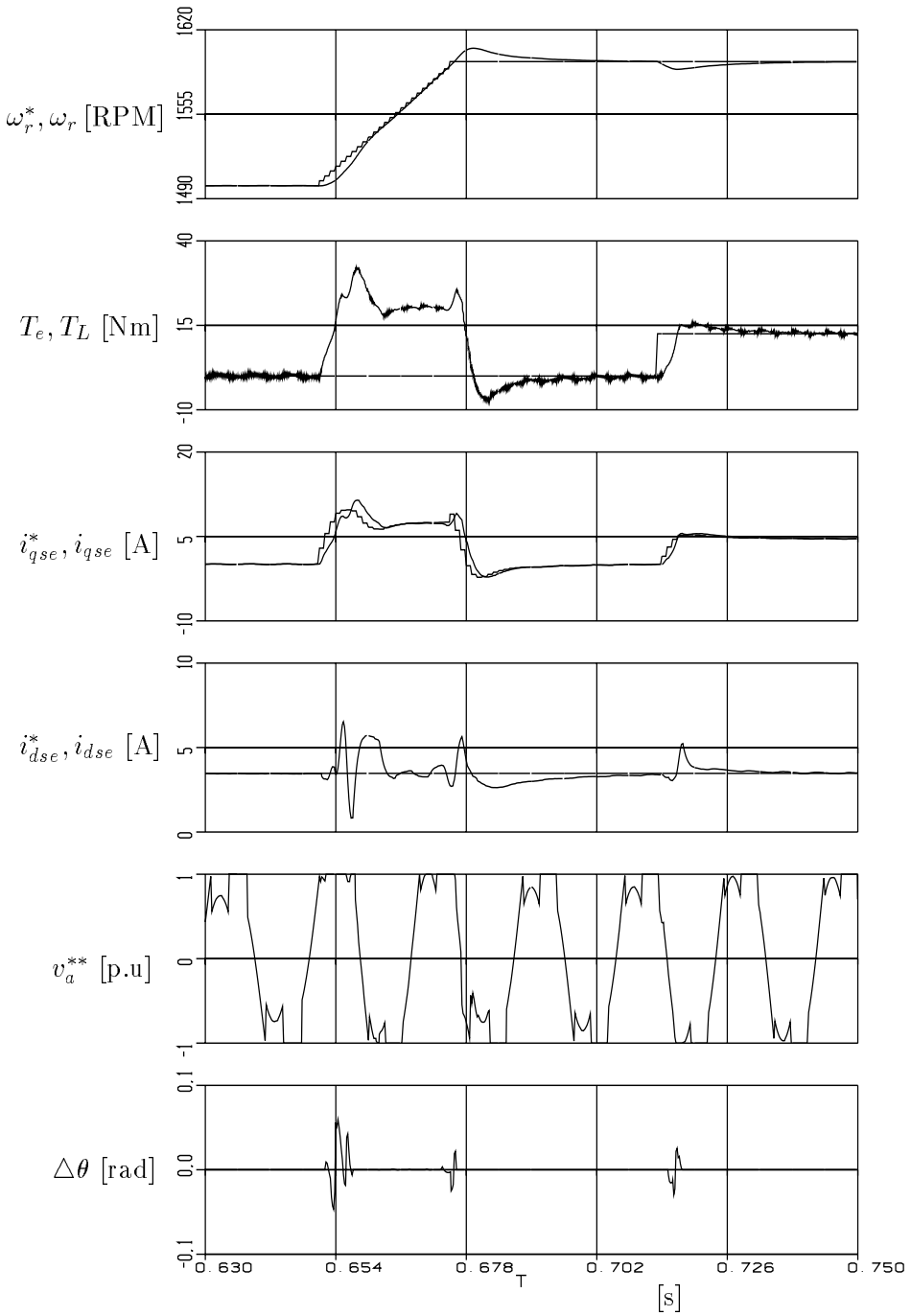

Figure 5.24: Induction motor drive DPWM2 (linear mode) and SVPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

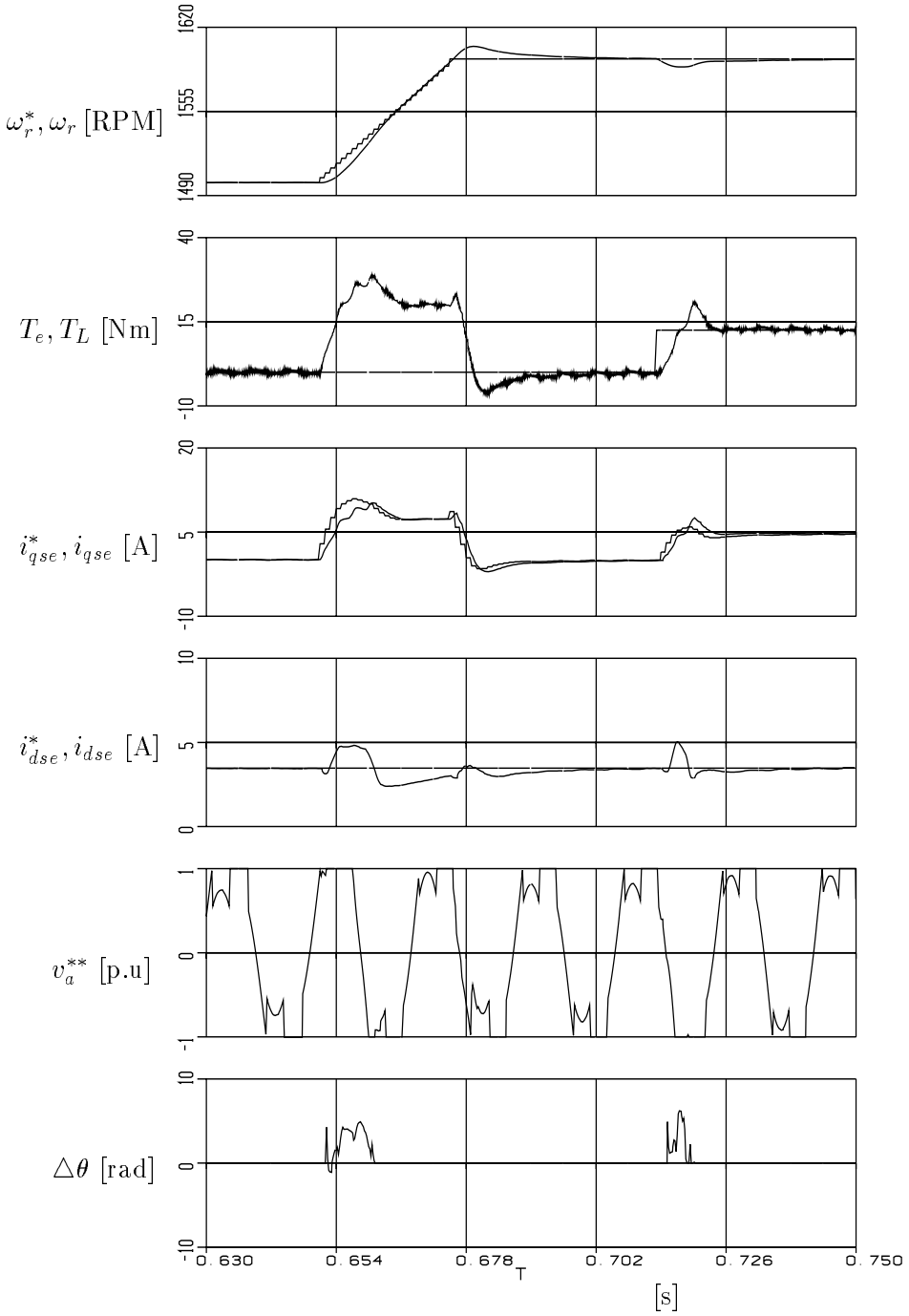

Figure 5.25: Induction motor drive DPWM2 (linear mode) and DFWPWM (overmodulation) combined algorithm dynamic overmodulation behavior.