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CARRIER BASED PWM-VSI DRIVES IN THE OVERMODULATION REGION

By

Ahmet M. Hava

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Abstract

Pulse Width Modulated Voltage Source Inverters (PWM-VSI) are widely utilized in motor drive and other three-phase power conversion applications as voltage/current sources with controllable output frequency and magnitude. The choice of pulse width modulation method strongly affects the inverter energy efficiency, waveform quality, and voltage linearity. However, the dependence of these performance characteristics on the modulator type is not well understood.

This thesis attempts an in-depth analysis of switching loss, waveform quality, and voltage linearity characteristics of the modern PWM methods. The analytical results aid the development of simple, yet highly efficient modulation strategies and control algorithms. A Generalized Discontinuous PWM method (GDPWM) which minimizes the switching losses and provides a wide voltage linearity range has been developed. Algorithms which combine the superior performance characteristics of the GDPWM method with other high performance PWM methods have been established. Modulator voltage linearity characteristics have been thoroughly investigated. Both the per carrier cycle voltage linearity and per output voltage fundamental cycle voltage linearity characteristics have been analytically modeled. In the nonlinear modulation (overmodulation) range, the influence of the modulator nonlinearity on the drive steady state and dynamic performance has been thoroughly investigated. As a result high performance overmodulation algorithms could be developed for various drives

and applications. With a strong emphasis on the overmodulation region performance of both open loop voltage feedforward controlled drives and closed loop current controlled drives, all the performance characteristics could be enhanced by employing the novel modulation methods and control algorithms. The theory has been supported with computer simulations and laboratory experiments and strong correlation has been obtained.

In addition to developing new modulation methods and control algorithms, this thesis establishes analytical and graphical methods for the study, performance evaluation, and design of the modern PWM methods. Also simple techniques for generating the modulation waves of the high performance PWM methods are described.

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The ten years I spent at the University of Wisconsin-Madison as a graduate student were rather difficult. Many years of exhaustive search for a useful thesis research topic rendered me quite exhausted. I am indebted to my family and friends for all the support and encouragement they gave me throughout these years. Without them, I could not find the inner strength to survive these years.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

The twentieth century is the most rapid technology advancement era in human civilization history. The substantial progress of the physical sciences in the preceding two centuries, in particular discoveries relating to electricity and magnetism, indicated devices operating with electric energy could offer significant advantages over human being's physical abilities. As a result, the twentieth century witnessed the invention of tremendous amount of devices most of which generate or utilize electric energy and provide service to the society. From food processing, textile, construction, metal industry etc. to transportation, communication, computer, education, entertainment etc. most necessities of today's society and environment involve electric energy and devices utilizing it.

In the early decades of the twentieth century the constant frequency constant voltage magnitude balanced three phase Alternating Current (AC) electric power source was found to be the most economical type for generation and transmission and was considered to be the most useful form of electric energy for many applications. Therefore, industrial loads have been supplied with three phase AC power sources and residential costumers with single phase AC power

sources (by balanced distribution of the three phases among various residential areas) through large power grids and interties reaching even the most remote habitation areas of the globe. Until now, the constant frequency and magnitude AC power has remained generally superior to other forms for generation and transmission purposes. However, it has been long recognized that this form of power is not suitable for many industrial processes and residential applications. For example, many chemical processes require controllable Direct Current (DC) voltage source, and most AC motors require three phase AC voltage with controllable frequency and magnitude. In addition, many precision machines and strategically important devices require constant frequency constant magnitude AC voltage source with high reliability and continuous power flow regardless of the utility line unbalances and fault conditions. Therefore, in most of these applications the utility line power can not be directly utilized; interfaces and devices to convert the form of the line power are necessary. The strong demand for power conversion and conditioning devices to achieve these tasks has lead to the establishment of the power electronics field early this century. High performance semiconductor power switches, efficient power converter circuit topologies, and intelligent control algorithms have been invented. As a result of this evolution, today's many industrial and residential loads are connected to the AC power line through cost effective power converter circuits which enhance the overall performance, efficiency, and reliability.

Of all the modern power electronics converters, shown in Figure 1.1, the Voltage Source Inverter (VSI), is perhaps the most widely utilized device with

power ratings ranging from fractions of a kilowatt to megawatt level. The VSI consists of six power semiconductor switches with anti-parallel feedback diodes. It converts a fixed DC voltage to three phase AC voltages with controllable frequency and magnitude. Since the VSI has discrete circuit modes for each set of switch states, generating an output voltage with correct frequency and magnitude requires an averaging approach. In the widely utilized Pulse Width Modulation (PWM) methods, the inverter output voltage approximates the reference value through high frequency switching. In AC motor drive applications, typically a rectifier device converts the AC three phase line voltages to DC voltage. Following the rectifier voltage passive filtering stage (typically capacitive filtering with/without DC reactor), the PWM-VSI interfaces the DC source with the AC motor to control the shaft speed/position/torque. In regenerative drive applications and AC-to-DC power conversion applications and also in Uninterruptible Power Supply (UPS) applications, the PWM-VSI provides reliable and high quality bidirectional power flow. When utilized in such applications, the device is often termed as converter (opposite of inverter), hence PWM-VSC. In all cases, power flow is controlled by the inverter switching device gate signals in a manner to obtain high performance, improved efficiency, and reliable operation.

Although its main circuit topology is quite simple, a modern PWM-VSI drive involves an overwhelming level of technology and intelligence. From the semiconductor power switching devices such as Insulated Gate Bipolar Transistors (IGBTs) operating at frequencies as high as many tens of kilohertz to

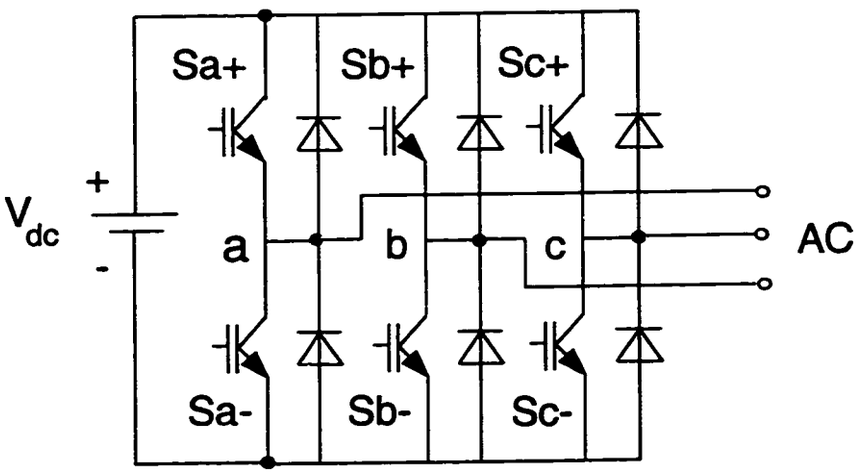

Figure 1.1: The main power structure of a VSI employing IGBT devices.

the microcontrollers and Digital Signal Processors (DSPs) that process the control signals at speeds beyond many tens of megahertz, most components of a state of the art PWM-VSI drive involve advanced technologies. The costumer's increasing demand for multifunctionality, precision performance, efficiency, reliability, and user friendliness has motivated engineers to build a significant amount of intelligence into the microcontrollers and DSPs of the PWM-VSI drives. Load parameter estimation, fault diagnostics, high performance vector control, observer based shaft encoderless speed control, energy efficiency optimization etc. algorithms have been developed and built into the modern PWM-VSI drives. With their global production rate above millions per year, the power ratings ranging from fractions of a kilowatt to megawatts, and the applications ranging from simple house applicances such as air-conditioning units

to heavy industries such as steel mills, PWM-VSI drives are modern technology devices which have been experiencing a rapid progress over the last three decades. This rapid progress is partially due to the great effort of many academic and industrial researcher's attempts to respond to the costumers demand for increasing efficiency, reliability, and enhanced performance. And, it is partially due to the substantial progress in the enabling technologies, such as the semiconductor micro and macro electronics technology.

Although the global effort to enhance the performance and maximize the performance to cost and kilowatts to volume ratios of the PWM-VSI has resulted in remarkable progress and various technologically advanced products have been marketed and found large number of applications, the technology is far distant from a complete maturation stage. Several remaining fundamental issues are summarized in the following.

Perhaps shaft encoderless operation of AC motor drives (at/near zero stator frequency) and PWM-VSI size reduction issues (by employing intelligent power modules, reducing the filter components, integrating a motor with an inverter, etc.) are the two most challenging and globally recognized and investigated issues at the present time. Additionally, the electromagnetic compatibility and reliability issues of AC drives with high speed switching devices such as IGBT's (widely utilized in PWM-VSI drives) are significant and await feasible solutions. The academic and industrial research and development effort spent on these subjects over the last decade is substantial. However, performance issues

involving the PWM techniques are as important and yet not fully understood and addressed.

Operating an inverter drive beyond the modulator voltage linearity limits, i.e. in the overmodulation region, is problematic. The voltage and current harmonics substantially increase and the dynamic performance is lost. Frequent overcurrent fault conditions occur and the drive performance and reliability degrade. Therefore, the operating range and power rating is constrained.

The linear modulation region switching loss and waveform quality characteristics of the conventional PWM methods are not well understood, and high performance controllers/modulators with implementation simplicity need be developed in order to increase the inverter efficiency and power quality.

Perhaps, the above several paragraphs summarize only a few of the many issues relating to the present state of the commercial PWM-VSI drives. Additionally, the ride-through performance, the unbalanced operating performance, switching device thermal performance, etc. all need be enhanced. It can be concluded from this discussion that the modern PWM-VSI drives have not completed their evolution and the opportunity to further enhance their performance is still vast.

This thesis attempts to address several of the above indicated problems, in particular, those relating to the pulse width modulators. In a PWM-VSI drive, the drive control algorithm generates the voltage reference signals and the modulator programs the inverter switching device gate logic signals. When the logic

signals are applied to the inverter switch gates, the switches commutate and an inverter output voltage which approaches the reference voltage over a predetermined carrier cycle is generated. As the gate logic signal source to the power semiconductor switching devices, the pulse width modulator forms the heart of an inverter drive. The choice of the switching sequence, number of switchings, the pulse widths etc. strongly affect the switching losses, inverter output voltage and current waveform quality, and the voltage linearity. Therefore, the modulator selection and design procedure of a high performance drive requires extreme care. On the other hand, choosing a modulator among a large variety is a challenging task. The modulator behavior is difficult to understand due to the nonlinear dependency of the modulator waveform quality, switching loss, and voltage linearity characteristics on several variables. With strong emphasis on voltage linearity characteristics, this thesis investigates the important modulator performance characteristics in detail, develops high performance modulation methods and provides modulator selection and design guidelines.

The fundamental contributions of this thesis are fourfold. First, modern modulators are grouped and characterized. A thorough investigation indicates the equivalency of various modulation methods. An attempt to unify the modern modulation methods successfully reduces their count and yields general rules for modulation signal generation. With the number of methods reduced to less than a handful, the characterization and comparison of their performance becomes a reasonable task. Establishing simple and accurate performance indices,

the important modulator linear region performance characteristics (the waveform quality and switching losses) are rigorously analyzed. Graphic illustration of these characteristic functions aids visual learning and understanding the modulator behavior intuitively. In addition, the algebraic performance indices simplify the modulator comparison, selection, and design.

Second, a high performance Generalized Discontinuous PWM (GDPWM) method with on-line controllable characteristics has been developed and its characteristics analytically investigated. Simple to implement, GDPWM can be closed loop controlled to maintain high performance (reduced switching losses and waveform distortion etc.) as opposed to the conventional modulators with predefined performance characteristics.

The third important contribution involves the overmodulation region performance investigation of voltage feedforward controlled open loop constant volts per hertz ($\frac{V}{f}$) drives. Detailed fundamental component voltage gain and waveform quality characterization of all modern modulators reveals the advantageous nature of a discontinuous PWM method in the linear high modulation and overmodulation regions. The inverter blanking time and the minimum pulse width constraints are shown to have substantial effect on the modulator linearity and the degradation is shown to be minimal with the discontinuous PWM methods.

The fourth important contribution of this thesis involves the dynamic overmodulation region behavior of closed loop current controlled high performance AC drives such as field oriented AC motor drives and PWM-VSC drives. The

detailed theoretical and experimental investigations show the strong interaction between the modulator and current controller can lead to drive instability and failure. The degree of instability is shown to strongly depend on the modulator type. Therefore the dynamic overmodulation characteristics should be considered in the modulator design process. Also steady state overmodulation in current controlled drives is studied and the performance issues discussed. The studies of this section aid the closed loop controlled high performance drive modulator design and control algorithm development process. High performance algorithms enhance the drive power output capability and the drive dynamic performance.

Overall, this thesis attempts an in-depth modulator analysis and the study yields precise design rules and high performance control algorithms for modern PWM-VSI drives. The emphasis of the thesis is on the overmodulation region. However, during the thesis evolution stage, a substantial effort was spent towards understanding the linear modulation region behavior. This effort yielded several important contributions to the linear modulation subject. Therefore, a substantial portion of the thesis also involves the linear modulation region behavior analysis and performance enhancement. The thesis clarifies most of the common misconceptions about PWM and simplifies the design and performance prediction task. With the novel high performance modulator and control algorithms, it enhances the PWM-VSI drive performance. As a result, the modern PWM-VSI drives advance one step closer towards becoming ideal power electronic converter devices.

The organization of this thesis is in the following order. In the second chapter, a detailed literature survey and state of the art assessment is provided. The in-depth survey reveals the importance of several neglected publications and illustrates some common misconceptions about modulators. The linear modulation and overmodulation region performance issues of the state of the art PWM-VSI drives are discussed in detail. A broad survey of the overmodulation operating region performance issues prepares the reader to recognizing the difficulty involved in operating in the overmodulation region.

The third chapter classifies the modern PWM methods, develops efficient methods to generate their modulation waves, and analytically investigates their waveform quality and switching loss performances with simple performance indices. The chapter also involves development and performance analysis of the GDPWM method. The superiority of this method over conventional modulators is illustrated both by theory and laboratory experiments.

The fourth chapter involves the overmodulation region characteristics of open loop voltage feedforward controlled drives. The fundamental component voltage gain characteristics are analytically derived and waveform quality investigated. The narrow pulse problems are discussed and finally performance comparison and modulator design are discussed.

The fifth chapter addresses the dynamic overmodulation region performance issues of closed loop current controlled drives such as the high performance field oriented motor drives. Following the modulator per carrier cycle dynamic

behavior analysis, an intuitive explanation supported with computer simulations and experimental work illustrate the performance issues of several popular PWM methods and solutions to the problem are investigated. The steady state overmodulation performance issues of current controlled drives are also studied and detailed computer simulations illustrate the performance limitations of such drives.

The sixth and final chapter summarizes the research results and recommends further investigations on subjects related to this thesis.

Since this thesis has contributions in various weakly related areas of modulation and drive technologies, the experimental investigations are discussed at the relevant stages of the associated chapters instead of being discussed all together in a separate chapter. Therefore, experimental work of each subject is discussed in the associated sections immediately after establishment of the theory.

Chapter 2

Literature Review and State Of The Art Assessment

2.1 Introduction

The one and a half century of progress in the electric machines field, about three quarters of a century of progress in the power electronics field, and about half a century of progress in the micro-electronics/macro-electronics and control fields are inherited in the state of the art PWM-VSI drives. Mostly occurring at different time frames, the breakthroughs experienced in each field have strongly and positively influenced the evolution of today's various types of cost effective, efficient, compact, and reliable high performance PWM-VSI drives. Since they involve various disciplines of engineering and there has always been a strong demand for them in the market, PWM-VSI drives have continuously drawn the attention of many researchers all around the world. Therefore, in parallel with this progress, a substantial amount of literature relating to electric drives has been accumulated. In particular, the literature involving the PWM methods

and drive control algorithms has surpassed thousands. Following a brief review of the early drives history, state of the art PWM-VSI drives will be described and the fundamental contributions to the area will be discussed in detail in this section.

2.2 A Brief History of Inverter Drives

Following the discoveries of electricity and magnetism laws in the preceding two centuries, the nineteenth century witnessed the invention of the DC machine, synchronous machine, the induction machine (1885 Ferraris, 1887 Tesla [7]) and the squirrel cage rotor induction machine (1890, Dobrowolsky). In particular, the last two inventions recently have found wide range of applications and the induction machine has become the workhorse of industry. From the early period to the present time the electric machines field experienced a continuous progress. Machines with improved structure and performance characteristics could be manufactured at reduced cost. As the machine characteristics have been investigated in detail and better understood, high performance control methods could be developed.

DC machine speed regulation by armature voltage control was established by Ward Leonard in 1891 [153], and in the following years high performance speed/position/torque control of DC machine methods were established. The constant $\frac{V}{f}$ operation principle of voltage feedforward controlled open loop AC

induction motor drives was established in the first half of the twentieth century. High performance induction machine control methods, however, were not developed until late 1960's. Since the induction machine dynamic behavior is more involved than the DC machine, mathematical methods were needed for understanding the dynamics and establishing high performance control methods. Following the establishment of the space vector theory in the 1950's [108], the Field Orientation Control (FOC) method was established by Hasse [61] and Blaschke [15, 16] in the late 1960's for high performance induction motor control. Since the FOC induction machine drive could approach or outperform a high performance DC machine drive, and offer cost reduction and ruggedness, it could replace DC drives in most applications. Permanent Magnet (PM) AC machines have recently emerged as a superior solution (to the DC machine predecessors) for high performance servo drive applications due to their high energy density, high efficiency, and reliability [183]. With the increasing energy cost, the PM machines are also becoming attractive for many industrial drive applications. Also, observer based shaft encoderless motion control methods for AC machines have been under development since the late 1970's. Therefore, the progress in the field of electric machines and their control has been continuous and at an increasing rate. However, all the advanced control methods require involved controllers and more importantly power sources with controllable characteristics, i.e. power electronic converters. Therefore, the developments in the electric machines area have generally been in parallel to the power electronics, control theory, and analog/digital microelectronics fields.

The power electronics field was established early in the twentieth century. By the middle of the century, power converters such as the mercury valve rectifiers, thyratrons, metal tank rectifiers, cycloconverters, load commutated inverters, current source and voltage source inverters, etc. were invented. Capable of controlling the flow rate and the form of electric energy, these power converters could regulate the electric machine motion and could control processes requiring electric power in AC or DC form. In particular, the invention of the three phase VSI was significant as it proved to be a high performance and cost effective device. The early development years of power converters (including the VSI), have been discussed in detail in [13, 128, 152, 154, 204]. Owen reviews the history of inverters and credits D. Prince for the invention of the earliest inverter device in 1925 [152]. He suggests the name "inverter" was given to this device for its operating characteristics are the reverse of the rectifiers; instead of AC to DC voltage transformation, DC to AC. The first practical application of three phase inverters is claimed to be in textiles [154]. However, inverters did not find widespread applications until the development of the modern power electronic switches.

Perhaps, the modern power electronics era began with the invention of the thyristor device in 1957. Overcoming the size, cost, efficiency, reliability, and performance deficiencies of the previous power converter switching devices, the

solid state semiconductor made thyristor gained immediate acceptance. In particular, its application in power converter circuits with inherent natural commutation characteristics such as cycloconverters, phase controlled rectifiers, reactive power compensators, etc. has been the most practical solution to the present date. However, lacking self commutation capability, the thyristor would require involved commutation circuits in forced commutation applications, rendering the drive bulky, expensive, and complex. Therefore, its utilization in forced commutation power electronic converters, in particular in the VSI applications, was limited and become obsolete with the invention of gate-turn-off solid state semiconductor devices such as the Bipolar Junction Transistor (BJT), Metal Oxide Silicon Field Effect Transistor (MOSFET), Insulated Gate Bipolar Transistor (IGBT), and at high power the Gate Turn Off (GTO) thyristor. In particular, the IGBT switches have become the most widely utilized devices and have revolutionized the PWM-VSI drives.

The switching frequency of the early power electronic converters was typically low. For example a VSI would operate in the six-step mode, yielding a switching frequency equal to the output voltage fundamental frequency. The intelligence involved in generating the gate signals was not significant and the control could be implemented with analog circuits. However, the low switching frequency would result in large amount of low frequency harmonic voltages/currents and therefore large amount of motor harmonic losses, torque ripple, etc. would be generated. With the continuously increasing switching frequency capability of the solid state semiconductor devices, the power electronic

converters could transfer energy to the load in small and controlled quantities such that the harmonics and their detrimental effects are substantially reduced. For example, in the VSI the output voltage could be synthesized of controlled width pulses such that the low frequency harmonics are substantially reduced. Therefore, large number of intelligent power electronic switching algorithms, most of which could be classified as PWM methods and on-off principle based current control, have been developed in parallel with the semiconductor device and control theory developments. Beginning in the early 1960's, the PWM field has been exhaustively investigated, and many methods have been developed for various types of converters and various applications. Although the early implementations involved analog circuits, with the increasing pulse pattern complexity and the demand to reduce the control circuit size and cost have lead to the development of the cost effective fully digital controllers which employ high performance microcontrollers, DSPs, and Application Specific Integrated Circuits (ASICs). Large volume production of these microelectronic chips with advanced manufacturing techniques continuously reduced the cost and the performance has been continuously enhanced with the clock speeds surpassing tens of megahertz.

As the historical review indicates the PWM-VSI drives are the product of nearly one and a half century of progress. They first become practical with the availability of the semiconductor switching devices thyristor and BJT, and the progress in the last three decades in the switching device, digital microcontroller and the control methods has lead to today's modern PWM-VSI drives. In the

following, we describe the state of the art PWM-VSI drives and discuss the progress made over the last three decades, i.e. in the modern drives era.

2.3 State Of The Art Modern PWM-VSI Drives

2.3.1 The Power Circuit Structure

Modern PWM-VSI drives have a wide range of residential and industrial applications. Since the power rating, performance, cost, size, etc. criteria of each application is different, the inverter drive design and control philosophies of different applications significantly vary. Therefore, a variety of PWM-VSI drives exists.

Generally, the voltage and current ratings required by the application of a PWM-VSI determine its power circuit design. The power circuit topology, type of the switching devices and passive filtering components, the cooling method, etc. are selected based on the drive voltage and current ratings. The higher the power rating, the more emphasis on efficiency, the more the auxiliary circuits and the more complex the cooling requirements. The voltage and current ratings also determine the drive hardware protection circuit complexity. The higher the power the more sophisticated protection circuitry. Finally, the controller and sensor choice is influenced by the performance requirements of the application. The higher the dynamic performance (bandwidth), the higher the

controller complexity and the higher the sensor count, bandwidth, and resolution. Therefore, as the power rating and the bandwidth requirements increase, the overall complexity increases.

With the cost being the driving factor, general purpose PWM-VSI drives with low kilowatt ratings (fractional to several tens of kilowatts) are generally designed with minimum component count and complexity. In AC motor drive applications, shown in Fig. 2.1 (a) a single/three phase diode bridge circuit rectifies the AC input voltage and a DC link capacitor filters the rectified voltage forming a stiff DC voltage source. The PWM-VSI converts the DC voltage to three-phase AC voltages with controllable magnitude and frequency via a PWM method. Below about hundred volts MOSFETs and at higher voltages IGBT power semiconductor switching devices are utilized in the VSI, and the switching frequency can be as high as many tens of kilohertz. The power circuit may also contain a DC link capacitor pre-charging circuit, a small EMI filter, and transient voltage suppression devices.

With the AC utility line power quality regulations becoming more stringent, at power ratings higher than several tens of kilowatts the input rectifier device performance becomes important. As shown in Fig. 2.1 (b), an inductor (DC reactor) is inserted in series with the rectifier in order to reduce the harmonic content on both the AC line and the DC link capacitor. Alternatively, a three phase reactor may be inserted in series with the AC line to suppress the harmonics. Also a dynamic brake formed by a resistor and a gate turn-off switch

is connected across the DC bus capacitor in order to limit the DC bus voltage under transients and during regeneration (Fig. 2.1 (c)). In regenerative applications with emphasis on energy efficiency back-to-back connected thyristor bridges or more commonly a PWM-VSC can be utilized (Fig. 2.1 (d)). However, with the PWM-VSC a relatively large and therefore expensive three phase reactor is required. Therefore, this solution is the most expensive approach. Up to near a megawatt the switching device choice remains to be IGBT due to its cost and performance advantages.

In higher power non-regenerative applications 12-pulse rectifiers together with input transformers with star primary and star-delta secondary windings are frequently utilized to reduce the input current harmonic distortion. In the megawatt power range, the PWM-VSI may be formed from parallel inverters, inverters with parallel devices, or more complex inverter device structures such as the three level VSI [79, 113, 140]. In regenerative applications back-to-back connected thyristor bridges may be utilized or a GTO based PWM-VSC can be utilized. The power semiconductor devices can be IGBT's, GTO's or some of the recently developed high voltage IGBT's and other new devices [188]. Due to the switching losses and the thermal issues associated with them, the switching frequency of the PWM-VSI decreases from tens of kilohertz at lower tens of kilowatts level to less than a kilohertz at the megawatt level. At increasing power levels, typically snubber circuits are added to reduce the commutation losses and the peak stresses on the devices.

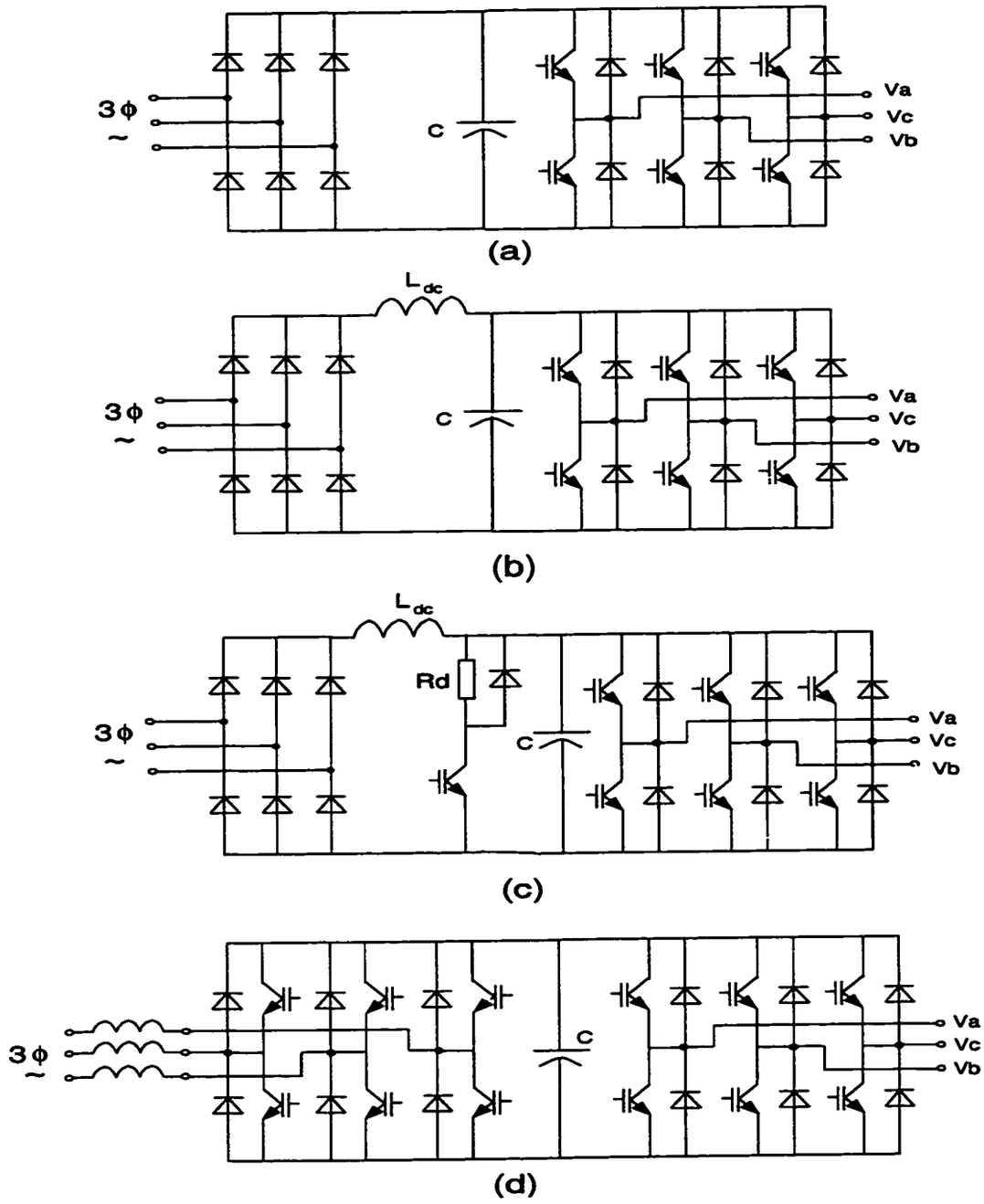

Figure 2.1: The power converter structure of various PWM-VSI drives.

The DC link structure is also application dependent. In applications such as the electric vehicle drives or UPS systems a stiff DC voltage source (battery etc.) is employed, hence no large DC link filter capacitor is required. The UPS application also differs from the motor drive application with the demanding filtering requirements in the AC output. Relatively large L-C-R filter elements are connected between the inverter outputs and the output terminals of the UPS.

From the simplest low power PWM-VSI drives to the most sophisticated high power VSI drives, all inverter drives employ hardware inverter overcurrent detector, DC link overvoltage detector, switching device saturation voltage detector, ground fault detector, heat sink temperature detector, and line voltage surge suppressor. With the increasing power rating, additional protection devices and sensors are involved. To rapidly interrupt the drive and protect both the load and the PWM-VSI after a fault condition, all the protection is normally implemented in hardware. Additional intelligent software protection and diagnosis algorithms can also be employed to enhance the reliability.

As the above summary indicates, the PWM-VSI hardware structure may significantly vary depending on the application. However, the main functionality of all the PWM-VSI drives remain the same; generating three phase voltages with controllable magnitude and frequency from a DC voltage source. Therefore, the switching device gate pulse pattern generation method determines the performance of a VSI. Discussed in the following, various PWM and control methods

result in unique drive types with advantageous performance characteristics.

2.3.2 The Drive Type

The controller choice of a PWM-VSI drive is determined by the requirements of the application. Low dynamic performance AC motor speed control applications may employ a simple control algorithm while high performance AC motor drives and utility interfaces may employ involved vector control algorithms. Although the control algorithms of various drive types are generally different, for the same power ratings, their power converter structure varies only slightly. Therefore, it is typical to design a common power structure for all applications and select the controller type, the sensors, and interfaces depending on its application. It is possible to integrate the sensor, interfaces, and controllers of all possible applications in one drive and allow the user to configure a control method suitable to the application. However, this approach has only recently become practical and in the traditional approach the commercial PWM-VSI drives were generally offered in various types mainly based on the controller functionality. In the following these drive types are briefly reviewed.

a)Constant Volts Per Hertz Control

The largest application area of PWM-VSI drives is AC motor control. Three phase AC induction machines, permanent magnet or wound field synchronous

machines, synchronous reluctance machines, etc. can be driven from a PWM-VSI to obtain torque, speed, and/or position regulation. Similar to Ward Leonard's method of DC motor speed regulation by armature voltage control, the constant volts per hertz ($\frac{V}{f}$) method is an effective method for AC motor drive speed regulation. In this method, the inverter output voltage is varied proportionally to the reference frequency such that constant stator flux is maintained. In particular in an induction motor drive, this operating mode results in shunt speed-torque characteristics (linear portion of the torque-speed curve), yielding low slip frequency and therefore high energy efficiency and good speed regulation. Therefore, the method gained wide acceptance in many industrial and residential induction motor drive speed regulation applications. The early applications of $\frac{V}{f}$ controlled VSI drives were reported in [26, 133, 134] and the feasibility of such drives proven by the late 1960s. These drives have had a large share of inverter drives market. However, the $\frac{V}{f}$ method is seldom implemented in its naive form, and additional algorithms and control loops are included in the control algorithm to enhance its performance. Slip frequency compensation methods to improve the load overhaul characteristics, voltage boost methods to compensate for the resistive voltage drop at low speed, and frequency skipping techniques to avoid the unstable operating regions are widely established and utilized [110, 135, 138].

State of the art $\frac{V}{f}$ inverter drives perform satisfactorily in a wide speed range (from 1 : 20 to better than 1 : 40) with 5% or better speed accuracy [44] and higher resolution can be obtained with shaft encoder feedback. However they

exhibit limited speed response (less than a couple of hertz bandwidth), poor load torque disturbance characteristic, and inferior low speed characteristics (they can not perform well below several hertz). Also, they have unstable voltage-frequency operating regions which should be avoided by carefully designing the $\frac{V}{f}$ curve. Typical application areas of $\frac{V}{f}$ drives are pumps, ventilation systems, etc. which have passive torque-speed characteristics (with inherent damping) and no precise speed regulation requirement.

b) Vector Controlled Drives

Many high performance motion control applications require precise position, speed or torque regulation. In elevator drives start-up, acceleration, constant speed vertical travel, and deceleration must be smooth for a comfortable ride. Motion quality must be retained regardless the mechanical or electrical disturbances to the system [137]. In printing press and winding machines precise tension control is mandatory. Pick and place type applications such as packaging require precise positioning. Spindle tools require a wide speed operating range with rapid acceleration characteristics. High precision machining processes require high servo performance with very high resolution position control. In these and many other demanding applications the performance of $\frac{V}{f}$ drives is not satisfactory. Although installing a shaft encoder feedback enhances the steady state speed regulation, the encoder feedback does not cure the dynamic performance notably, neither does it provide precision position control.

Such applications traditionally have employed DC machines with shaft encoder. However, the continuous progress in AC machine control theory, power electronics, and digital microelectronic controllers yielded the modern vector controlled AC machine drives which can match or surpass the performance and reliability characteristics of DC drives and cost less.

Modern vector controlled AC induction motor (typically squirrel cage rotor type) and synchronous motor (typically below hundreds of kilowatts surface mount or interior permanent magnet machines and at higher power ratings wound field machines) drives meet the demanding performance criteria of most high performance motion control applications. Although high performance control method of the wound field synchronous motors which is based on the vector control principle was established in the 1930s [6, 144], the concept could not be easily extended to induction motors. Due to the coupling between the stator and rotor circuits, the induction machine formed a complex system with difficult to manipulate dynamic transients. However, with the aid of vector coordinate transformations and intuitive modeling, the machine behavior could be better understood and lead to the development of the vector control theory based Field Orientation Control (FOC) method which most modern high performance induction motors employ [145].

The principles of high performance induction motor control were established about 25 years ago. The Indirect Field Orientation Control (IFOC) method was developed by Hasse [61] and employs a shaft encoder to close the speed

loop. The Direct FOC (DFOC) method was developed by Blaschke [15, 16] and it employs flux sensors/observers. In FOC, the magnetizing flux and torque producing components of the stator currents are properly and independently distributed both during steady state and dynamic conditions. Independently regulating each component with a high performance current controller, the drive torque can be controlled in the same precise manner as the DC machine [145].

Since installing flux sensors in the stator or the airgap of a machine is difficult, and the operation is not reliable, the DFOC method is practically rarely employed in its original form. Employing flux observers, the DFOC method provides high performance torque control, in particular in the high speed region where the stator resistance voltage drop is small compared to the stator EMF and the stator flux observer is highly accurate. The stator flux oriented DFOC method is attractive for traction, spindle tool etc. applications which require operation in a wide field weakening region. However, near zero speed the stator flux observer estimator error becomes substantial due to the dominance of the stator resistive voltage component over the nearly zero EMF and the DFOC method looses performance.

In a large number of applications requiring high performance in the low speed operating region the rotor flux oriented IFOC method is utilized. Since the rotor flux oriented IFOC method utilizes the rotor time constant to build the rotor flux observer, the method is sensitive to the rotor resistance and inductance variations and a suitable parameter adaptation method is employed [51, 176].

With accurate parameter adaptation, the IFOC based induction machine drives can provide servo performance in a wide speed region, and only in very wide field weakening applications their performance at high speed becomes unacceptable. In such very wide operating region applications, hybridization of the DFOC and IFOC methods has proven to yield an overall superior performance, however at the cost of increasing controller complexity. The combined algorithms established by Jansen et al. transition from IFOC at low speed to DFOC at high speed seamlessly, yielding precise motion control [84].

Modern permanent magnet synchronous machine drives employ the same vector control principle as in FOC. However, in this case the controller axis is precisely aligned with the rotor magnet or magnetic reluctance axis. Therefore, with the rotor position measured or estimated accurately, the control method is straightforward. In surface-mount permanent magnet rotor synchronous machines the stator current flux producing component (the direct axis current) is normally zero, and the torque is proportional to the stator current. In the buried (internal) and inset magnet rotor synchronous machines and in the synchronous reluctance machines both direct and quadrature axis currents exist and must be properly controlled to obtain high torque per ampere, superior dynamics, and wide speed range. The surface-mount magnet synchronous machines are widely utilized as AC servo drives, while the buried and inset magnet PM machines are utilized in wider speed range applications due to their superior field weakening capability. Also synchronous reluctance machine drives have been developed for integral horsepower lower cost applications.

Since the torque regulation quality of an FOC induction motor drive or vector controlled synchronous machine drive is mainly dependent on the current controller accuracy and bandwidth, high performance motion control requires high performance current regulators. Of the various current control algorithms, the Synchronous Frame Current Regulator (SFCR) [174] and its stationary frame equivalent [166, 167] have superior steady state and dynamic performance and they have been widely employed in high performance AC motor drives and also in UPS and PWM-VSC applications. In these controllers the proportional and integral components operate on the current errors and generate voltage references in which are translated to switching signals by a PWM method. The hysteresis type current controllers which have superior dynamic performance have not gained acceptance in motor drives due to the difficulty in controlling their switching frequency and significant waveform distortion.

Employing high switching frequency IGBT devices and high performance digital signal processors or microprocessors, high performance current controlled drives provide high torque/speed bandwidth, hence high motion quality. As a result, the state of the art FOC induction motor drives and vector controlled PM motor drives perform quite satisfactorily. High performance FOC drives have been successfully employed in industrial and servo drive applications for more than a decade [109]. The evolution of FOC drives from concept to industrial products and successful applications has been summarized by Leonhard in [119, 120] in detail. The speed range of state of the art FOC drives surpasses 1 : 3000 and the speed regulation is better than 1 %. With a speed bandwidth

as high as 100 Hz, high start-up torque capability, and wide range of field weakening capability, state of the art FOC induction machine drives exhibit servo performance and continue to replace the DC drives. Vector controlled synchronous PM machines are widely employed in high performance servo drives and their application range continues to expand due to their superior energy efficiency and high power density.

c) Shaft Encoderless High Performance AC Drives

Since the IFOC method requires an encoder and its associated cabling and interface circuits, its utilization in many medium performance applications is cost prohibitive. Furthermore, in certain applications the operating environment is hostile and the encoder, its cabling, and connectors may fail due to extreme stress rendering the drive fault prone. In such applications, various types of shaft encoderless AC motor speed control algorithms which perform between $\frac{V}{f}$ and FOC drives, emerge.

Following the early attempts to enhance the performance of $\frac{V}{f}$ drives and the recognition of their performance limitations [2, 3], the pioneering work in the shaft encoderless motor speed control area was reported by Jötten and Maeder in 1983 [87]. They employed the induction motor fundamental model to estimate the slip frequency and the back emf of the machine and provided a closed loop controller to regulate the slip such that superior dynamic performance could be obtained in a wide speed region, including the field weakening region. Although

a large variety of shaft encoderless control methods have been reported from that time to the present date, only a few found practical applications [67, 78]. Of these, the Direct Torque Control (DTC) method and several other state estimation methods which employ the fundamental model of the induction machine and the vector control principle to estimate the stator/rotor flux, velocity, and position, and often termed as "open loop flux vector" methods have been fully developed (in particular for induction motor drives), commercialized and employed in a wide range of applications.

As the name suggests, the DTC method regulates the motor torque and flux directly. The direct torque control principle was established in the early 1980's by Török [195] and further developed by Takahashi and Noguchi [190] and Depenbrock [43]. In the DTC approach, the torque reference is compared to the estimated motor torque and the reference stator flux is compared to the estimated stator flux, both employing hysteresis controllers. The torque and flux hysteresis controller output logic signals are evaluated in an optimal switching logic table to generate the inverter switching device gate signals. Both the estimated torque and stator flux are calculated from the machine model and measured motor currents, reference voltages, and the DC bus voltage. The method has recently been employed in various industrial applications and its viability proven [34, 123, 143, 193, 194]. With their rapid torque response, and wide band spread switching frequency harmonics (white noise) characteristics, the DTC drives exhibit notable performance differences from the conventional drives.

Several popular state estimation based induction motor control methods employ the fundamental model of the induction machine and provide a parameter adaptation method to account for the parameter variations of the machine. Several methods employ a rotor flux oriented IFOC model in order to approach a FOC drive performance [86, 150, 151]. These methods employ a reference model of the induction machine and the actual rotor flux axis of the machine and the flux axis of the controller are locked so that FO condition is attained. The motor phase currents/voltages (measured and/or predicted) are utilized in the reference model and any misalignment between these axes is minimized by the controller, yielding superior speed regulation. The choice of observer variables depend on the method, and the performance of each method is dependent on how accurate the reference model parameters represent the actual system. The method by Okuyama et al. [151] utilizes the torque current error, $i_{qe}^{*} - i_{qe}$, to calculate the correction angle and a voltage feedforward controller programs the reference voltages that operate the drive under IFOC condition. The method by Ohtani [150] employs the torque current error also, however it involves a rapid current controller and has superior accuracy and dynamic performance. The method by Kerkman et al. [94, 168] employs the direct axis voltage error and with accurately measured voltages, it can provide superior angle correction yielding superior performance, in particular in the lower speed region. All the practical methods also employ adaption algorithms to account for machine parameter variations [173]. However, all these methods have limited performance near zero speed. This fundamental limitation has lead to the investigation of

alternative methods [17, 41, 56, 82, 83, 179] which may be combined with the above methods to provide a wider operating range.

The DTC and open loop flux vector methods have recently been successfully employed in many industrial applications with no stringent near zero speed performance requirements. With their superior load and DC bus voltage disturbance rejection capability, they provide high quality motion control. Impact loads and load overhaul condition are better manipulated than $\frac{V}{f}$ drives. They provide high accuracy speed regulation and sufficient dynamic response in a wide speed range. State of the art open loop flux vector controlled induction motor drives can provide as wide as a 1:1000 speed range, a speed loop electrical bandwidth as high as 15 Hz, a speed regulation better than 0.1% and can supply more than 150 % starting torque in wide power range from fractions of a kilowatt to several hundred kilowatts [44, 130, 150, 173].

In addition to induction machines, PM synchronous machines (in particular, machines with large magnetic saliency) have also been successfully operated without speed sensor down to zero speed [164].

d) Multi-purpose, Universal, and Integrated Drives

Many modern inverter drives have the capability of operation with any of the above discussed three different drive control methods. In such user configurable drives the motor can be controlled in any of the above modes by simply selecting the desirable mode through the user interface. The interface, controller memory

size, and current/voltage sensor requirements of such drives are designed for the highest performance IFOC operating conditions. Therefore the component cost is higher than all above. However, the modularity and multi-functionality, reduced design and assembly cost and reduced hardware cost of these drives yield better performance to cost ratio and therefore these drives have gained wide acceptance. Such drives have been advertized as universal drives, general purpose drives, multi-purpose drives [201] and have found wide range of applications.

In addition to modularizing the control board of inverter drives, the switching devices are also modularized and intelligent power modules with enhanced reliability and reduced hardware requirements have been developed. Furthermore, the integration of motors and inverter drives has resulted in additional space and cost reduction. In particular, the fractional and integral horsepower range integrated induction motor and inverter drives have been offered as compact and low cost drives with superior performance [11, 55].

Many industrial processes have been employing programmable logic devices to program the motion required for an industrial process. Several recent inverter drives are built with such capabilities and they eliminate the additional wiring and device cost/maintenance. As this and all the above examples illustrate, the strong influence of the digital microelectronic technology on inverter drives has been continuing at an increasing rate.

e) Voltage Source Converters and UPS Applications

In addition to being utilized in motor control applications, PWM-VSI drives are also employed in AC/DC power conversion applications such as regenerative motion systems, UPS and utility interface of DC voltage loads. Although several important design differences and performance requirements exist, generally these drives employ vector control principles in order to achieve high performance voltage/current/power quality and robustness against disturbances [124].

Back to back VSIs are increasingly being utilized in applications such as elevators which frequently operate in regenerative mode. While the load side VSI provides high performance motion control, the line side VSI provides high power quality and high energy efficiency. Additionally, the DC link capacitor of such drives can be made significantly smaller than the diode rectifiers [5, 170].

2.4 Voltage and Current Regulators

The position, speed, torque, DC bus voltage etc. control loops of all the previously discussed PWM-VSI drives generate voltage or current references that must be matched by the inverter. High performance voltage and current regulators are critical parts of an inverter drive that achieve this task. Depending on the performance requirements, the regulator types vary. Constant $\frac{V}{f}$ drives

employ voltage feedforward, while all the other high performance drives employ closed loop voltage/current regulators. As an exception the DTC method employs torque and flux regulation and the voltages and currents are not directly controlled. High performance FOC induction and synchronous motors and PWM-VSC applications employ current regulators. Within two decades the current regulator technology evolved from the simplest on-off principle based AC current regulator to the present day industry standard high performance synchronous frame current regulators.

The three phase current regulators can be grouped into two classes; on-off principle based (memory-less) regulators and linear control principle based regulators employing carrier based PWM methods. The hysteresis and delta current regulators are the two established on-off principle based current regulators. In the delta current regulators the phase current errors are periodically sampled and the phase current error polarity determines the switch state of the associated inverter leg [186]. If the error is positive the upper device, otherwise the lower device of the inverter leg associated with the regulated phase is turned on. In the hysteresis current regulator the phase current errors are continuously monitored and if the current errors become larger than a predefined tolerance band, commutation takes place in the same manner as the delta regulator. Hysteresis current regulators can be built for each phase individually (scalar method) or in vector coordinates (vector method) with the latter being superior.

The historical development of the on-off principle based current regulators is as follows. Plunkett showed that current regulated drives could have more stable behavior than $\frac{V}{f}$ drives, and implemented a scalar hysteresis current regulator [159]. Brod and Novotny studied the coupling of the scalar method and illustrated its limit cycle behavior [28]. McMurray analyzed the switching frequency characteristics of hysteresis current regulators and illustrated the phase and load parameter dependency of the switching frequency [127].

The on-line predictive method developed by Holtz et al. [76], the table based predictive method developed by Nabae et al. [139], and the synchronous frame based hysteresis current regulator with rectangular tolerance band by Bube et al. [74, 96] are all high performance vector hysteresis current control methods. Intelligently selecting the adjacent inverter states, these regulators provide lower distortion per switching than the scalar method. With these methods a small performance enhancement comes at the expense of significant controller complexity [122, 172]. Both vector and scalar hysteresis methods have poorer waveform quality than the linear control methods employing PWM. In addition to the poor waveform quality, the methods have operating condition dependent switching frequency variation and the output waveform contains significant magnitudes of white noise harmonic spectrum (an inherent feature in on-off principle based regulators) unacceptable in many applications. Therefore, these methods have found limited applications.

As previously discussed, the DTC method employs vector hysteresis controller and the waveform characteristics of DTC controlled VSI are the same as vector hysteresis current controllers. However, the control variables of DTC are the torque and flux, instead of the currents. Although the method has superior torque response characteristic, its waveform quality characteristics are not acceptable in many applications. Therefore, the vector hysteresis flux and torque controller, and the DTC method which utilizes this principle have limited applications.

Most state of the art high performance PWM-VSI drives employ linear current controllers with Proportional and Integral (PI) structure which have superior steady state performance compared to on-off principle based methods. In these methods, the current errors are evaluated in the PI controllers, hence the current errors are translated to voltage references. Voltage feedforward and cross-coupling decoupling terms are added to the reference voltages in order to enhance the controller performance. A PWM method processes the reference voltages to generate the switching signals. In the scalar method, the phase current errors are fed to the PI controllers of the associated phases and the output of each controller forms its voltage reference. In the vector method, the currents are transformed to the controller coordinates (typically the synchronous frame). The direct and quadrature axes PI controllers process the errors and add voltage feedforward and cross-coupling decoupling terms to generate the reference voltage vector. The reference voltage vector is transformed to the stationary

frame and this vector is either directly utilized to compute the device duty cycles, or it is transformed to abc variables and fed to a modulator to generate the switching signals.

Schauder and Cody showed that the vector PI current regulator behavior is dependent on the reference frame it is implemented in [174]. They developed the SFCR method which has zero steady state error and high dynamic performance. Hence, superior performance compared to the stationary frame per phase current regulators. Rowan and Kerkman showed that SFCR can be implemented in stationary frame which allowed a simplified hardware implementation [167]. In addition they provided analytical comparison between stationary and synchronous frame regulator performance and illustrated the superiority of SFCR through the regulator gain versus frequency plots. Shown in Fig. 2.2 both SFCR and its stationary equivalent implementation have been widely utilized due to their high performance characteristics. State of the art SFCRs typically employ additional voltage feedforward and cross-coupling decoupling control to increase the dynamic performance of the drive [50, 93, 118, 121, 160]. References [50, 148] describe the design of high performance SFCRs with sufficient detail. In particular, [50] discusses practical approaches to obtain very high bandwidth current controller performance. The SFCR stationary equivalent structure does not have cross-coupling components and need only voltage feedforward components to obtain high performance. With careful design, the analog implementation of this regulator can yield very high bandwidth. Also recently a complex vector

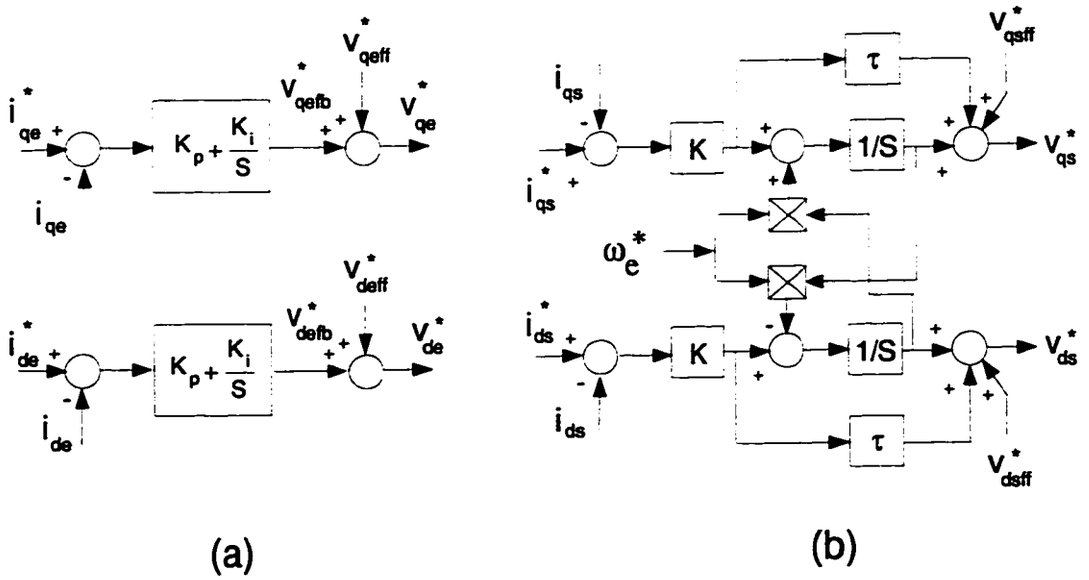

Figure 2.2: Synchronous frame current regulator (a), and its stationary frame equivalent (b). In both regulators the coordinate transformation operators are not shown.

SFCR method was established by Briz and Lorenz [27]. In the modulator linearity range, this controller is exhibits quite similar performance characteristics to SFCR.

Early current regulators were implemented with analog hardware circuits. The SFCR and its stationary equivalent both involved analog/digital hardware circuits that were bulky and expensive. With the development of low cost high performance DSP and microcontrollers the digital implementations rendered the analog controllers obsolete. The early experimental work by Gabriel et al. illustrated the feasibility of microprocessor controlled FOC drives with analog current loops [49]. This study hinted the future trends in implementing the AC drive controllers. As the microelectronics technology advanced and the signal processing speed increased with the cost decreasing, the fast current loops could

also be implemented on a digital platform. Pollmann illustrated the feasibility of fully digital AC drives employing digital SFCR [160]. Although the analog current controllers involved continuous feedback and control signals, the digital implementations involved discrete feedback signals, hence the feedback current sampling issues were important.

In the "synchronous sampling" method, the feedback currents are periodically sampled at the carrier frequency rate. Sampling the feedback currents at the positive and/or negative peak values of the triangular carrier wave (where the switching frequency harmonic currents are negligible) would yield a "switching frequency harmonic free" measurement. The synchronous sampling method has become the industry standard and is widely employed in most fully digital drives [206]. Matsui et al. discussed the feedback current sampling issues in digital current loops and proposed an averaging method which improves the feedback current measurement accuracy [126]. Further improvements on feedback current sampling, signal conditioning, and accurate measurement have been reported in [12, 39, 73, 184].

As a result of this progress, the microprocessor and DSP based digital drive controllers today, are more cost effective and provide better performance than the analog/digital hardware based designs. Design of application specific digital controllers, such as the recently developed VECON and TMS320F240 chips (fast DSP for control, low cost microcontroller for communications and low priority level tasks, PWM generator, blanking time generator, etc. integrated in one

chip) at low cost is expected to accelerate this trend even further [97, 115, 141, 155].

2.5 Modulation Methods

In the on-off current controlled drives and torque/flux regulated DTC drives, the switching signals are available immediately at the controller outputs. However, in PI controller based (linear) current regulated drives, and voltage feedforward controlled drives the switching signals are determined in an additional block termed as the "modulation" block. In this block the reference voltages are evaluated and proper switching device gate logic signals are generated for all the three inverter legs.

Since voltage source inverters employ switching devices with finite turn-on time and turn-off time characteristics, inverter switching losses are inevitable. Because the switching losses strongly affect the energy efficiency, size and reliability of an inverter, a modulation method with high performance is desirable. Therefore, the modulation method choice is significantly important. Of the variety of modulation methods, the carrier based PWM methods and the programmed pulse modulation method are the two most recognized methods.

In the programmed pulse modulation methods the switching patterns are precalculated for a given performance optimization criteria and the commutation angles are stored in a memory array. During operation the memory array

is accessed on-line through the drive controller to generate the inverter gating signals for a given reference voltage phase and magnitude value. Various performance optimization criteria have been considered in generating the commutation angle table. A harmonic elimination method which totally eliminates certain harmonics from the output waveform (typically the unwanted harmonics are the 5th, 7th, 11th, 13th etc.) was first developed by Turnbull [200] and later further investigated by Patel and Hoft [156, 157]. Following this work, Buja and Indri proposed an output current THD minimization criteria for optimizing the pulse pattern [33]. Efficiency optimized pulse patterns [208], and torque ripple minimized pulse pattern [209] have also been characterized. Utilizing such optimal switching patterns as a template, Holtz et al. developed trajectory tracking methods which improve the dynamic performance of voltage feedforward drives [70, 71, 73].

All the programmed pulse methods require large computer memory space and in most methods the number of pulses per fundamental cycle is limited to a small number, typically less than five switchings per phase and per quarter cycle. In particular, in the high voltage utilization range, the optimal angles near the peak of the fundamental component of the voltage become significantly close, with no sufficient room left for commutation or blanking time. Due to this fundamental limitation, the programmed modulation methods can not operate with high switching frequency. Therefore, they can not provide output waveforms with very low harmonic distortion waveform. The application of the programmed pulse methods is usually limited to very high power drives with

power ratings above a megawatt level where low switching frequency is selected for low switching losses.

Unlike the programmed pulse modulation methods, the carrier based PWM methods can operate with high switching frequency and they offer high waveform quality and implementation advantages. Carrier based PWM methods employ the per carrier cycle volt-second balancing principle to program a desirable inverter output voltage waveform. The first important contribution in the carrier based PWM area was done by Schönung and Stemmler [177] in 1964 with the development of the sinusoidal PWM (SPWM) method. As shown in Fig. 2.3, in this method the sinusoidal reference waveform (the modulation wave) of each phase and a periodic triangular carrier wave are compared and the intersection points determine the commutation instants of the associated inverter leg switches. The well established modulation theory indicates that for sufficiently high carrier frequency to modulation wave fundamental frequency ratio, the modulation waveform fundamental component magnitude and the inverter output voltage fundamental component magnitude are linearly related until the modulation wave magnitude becomes large and the sine and triangle intersections begin to disappear [10, 14]. Within the linear modulation range, the sinusoidal PWM method sub-carrier frequency harmonic content is significantly low, and the switching frequency is fixed. Due to its simplicity and its well defined harmonic spectrum which is concentrated at the carrier frequency, its sidebands, and its multiples with their sidebands, the SPWM method has been utilized in a wide range of AC drive applications. However, the method has

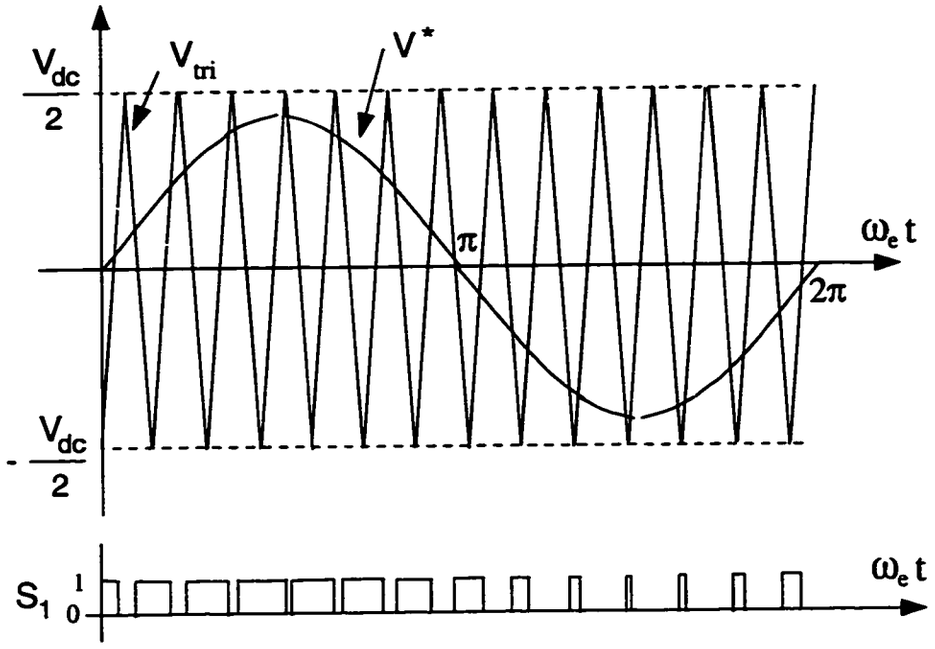

Figure 2.3: Sinusoidal PWM method. The intersection points of the modulation wave and carrier wave define the switching instants.

a poor voltage linearity range, which is at most 78.5 % of the six-step voltage fundamental component value, hence poor voltage utilization. Therefore, the zero sequence signal injection techniques that extend the SPWM linearity range have been introduced for isolated neutral load applications which comprise the large majority of AC loads [32, 101].

In most three phase AC motor drive and utility interface applications the neutral point is isolated and no neutral current path exists. In such applications in the triangle intersection implementations any zero sequence signal can be injected to the reference modulation waves. K. G. King was possibly the first researcher to utilize this concept in a voltage source inverter, and his zero sequence signal choice which will be discussed in the next chapter in detail,

remains to be one of the most popular choices [101]. King realized that a three phase diode rectifier circuit shown in Fig. 2.4 could be utilized to generate a zero sequence signal. His choice of scale which was based on the linearity maximization criteria allowed the converter to extend its linearity range from 78.5% to 90.7% of the six-step voltage. This important invention has been neglected for a long time. This modulation method was later re-invented employing the space vector theory [29, 158]. Since the method in these publications was termed "Space Vector PWM" (SVPWM), in this thesis this name is also adopted for King's method. In addition to developing a digital implementation for SVPWM, Van Der Broeck et al. illustrated the SVPWM method has superior waveform quality compared to SPWM in particular in the high modulation region [29]. Since this implementation involves a vector controlled drive and the reference voltage vector information is directly translated to inverter switch duty cycle information, this method is often termed "direct digital implementation technique," while the implementation involving modulation waves is termed "the triangle intersection technique."

A recent publication re-introduced King's configuration as a new analog hardware SVPWM implementation [66]. Perhaps, the neglect has been due to the difficulty in distinguishing the valuable literature among a large volume as well as the difficulty in understanding his article. However, various other zero sequence signal injection methods with advantageous performance characteristics have been invented between the 1970's and the present time.

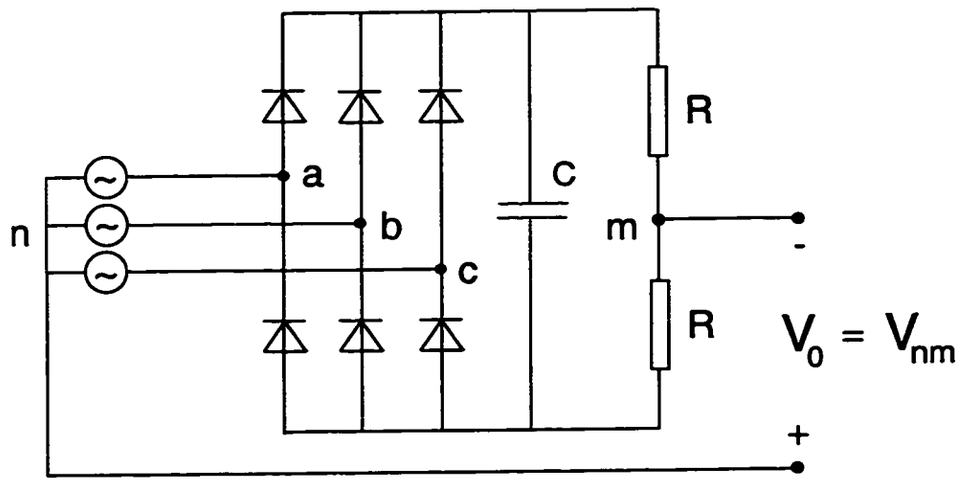

Figure 2.4: King's zero sequence signal generating circuit.

The third harmonic injection PWM method was developed by Buja and Indri [32]. It was shown a triplen harmonic with a magnitude equal to one-sixth of the fundamental component modulation wave would provide maximum inverter voltage utilization. Similar to King's invention, this invention has not gained attention and the method was re-reported many years later with no recognition of the original work [77]. However in this case a digital implementation was described. Bowes and Midoun attempted to compute a modulation wave with minimum RMS harmonic distortion by computer simulations and numerical approaches. They concluded that a third harmonic injection with a magnitude equal to one-fourth of the fundamental component is a numerical optimum value [24]. With the performance optimization criteria being the output waveform harmonic distortion RMS value minimization, Kolar et al. analytically verified

this argument [105, 106]. However, the performance advantage was shown to be only in the high voltage utilization range. Moreover, the advantage over SVPWM and the other methods was shown to be insignificant. Both methods discussed in this paragraphs are constrained to a pure third harmonic signal injection, while King's SVPWM approach naturally included additional triplen harmonics and yielded superior performance. Furthermore, many years before such academic exercises were published, it was well understood that in the high modulation range the above discussed methods were inferior to a special group of modulation signals.

Perhaps, the invention of various Discontinuous PWM (DPWM) methods has been the third most important modulator invention following the invention of SPWM and SVPWM. In the DPWM methods, a zero sequence signal which brings one of the three modulation signals to the same level with the positive or negative peak of the triangular carrier wave is selected. Since the switching in the corresponding inverter leg ceases, the switching losses are eliminated so long as this condition persists. Therefore, the inverter switching losses can be controlled with the zero sequence signal. This fact was first was recognized by Schörner [178]. In his work, Schörner aimed to extend the linearity of SPWM by injecting a zero sequence signal to the sinusoidal modulation wave. However, his choice of zero sequence signal was significantly different than the previously reported. Of the three phase modulation signals, he selected the one with the maximum magnitude for generating his zero sequence signal. Therefore, the top and bottom 60° portion of each sinusoidal modulation signal would be

processed to obtain a zero sequence signal. He generated a zero sequence signal by calculating the difference between the peak value of the sinusoidal modulation signal and its instantaneous value within the associated 60° section. Injecting this zero sequence signal to the sinusoidal references, modulation signals with two 60° flat top segments could be obtained. For modulation depth smaller than 91 % of the six step voltage fundamental component value, the modulation signals are contained within the triangular carrier wave boundaries. However at this end point, the top and bottom segments become equal to $\frac{V_{dc}}{2}$. Therefore, at this operating point, the particular phase ceases switching. Therefore switching discontinues and no switching losses are generated.

In the following years, Depenbrock established a method which provides discontinuous modulation throughout the modulation region and also proposed a simple analog hardware implementation [42]. Similar to King's SVPWM circuit, Depenbrock's DPWM circuit employed a diode bridge rectifier to generate the zero sequence signal. However, additional analog switches were required. The modulation waves of Schörner's method and Depenbrock's method are identical at 90.7 % voltage utilization. However, the latter ceases switching at least for the two 60° segments regardless of the voltage utilization level. Depenbrock quantitatively investigated the switching loss reduction, voltage linearity, and waveform quality characteristics of this DPWM method. He illustrated the performance superiority of this method over SPWM in particular in the high voltage utilization region. As the attributes of this methods were recognized, it has found applications in motor drives and PWM-VSC applications [46, 124, 142].

Since in this method only two phases modulated at a time, the method has been termed as "two phase modulation." Since in this and the following methods modulation of each phase ceases for a certain portion of the fundamental cycle, the methods are more often termed as "Discontinuous PWM" (DPWM) methods. The latter term will be adopted in this thesis. Also, The DPWM method which is described above will be abbreviated with the DPWM1 symbol throughout this thesis.

Although clamping the two center 60° portions of the modulation waves reduces the number of commutations per fundamental cycle and the switching losses (by at least 33 %), depending on the load power factor, the quantitative value of the switching loss reduction may be different than the commutation numbers. Since in a typical semiconductor device the switching losses are proportional to the commutated current, under unity power factor condition DPWM1 has the lowest switching losses compared to different power factor conditions. Ogasawara et al. recognized this fact and developed a modulator suitable for induction motor loads [146] which typically operate near 30° lagging power factor condition. Instead of ceasing modulation at the center portions, they proposed a 30° phase delayed DPWM such that the portion that modulation ceases coincides with the largest phase current. Since it provides significant switching loss reduction compared to DPWM1, this method gained recognition and found wide range of industrial applications. This method will be abbreviated with the DPWM2 symbol throughout this thesis.

The work by Ogasawara et al. utilized the space vector coordinates for analysis and illustration of the effectiveness of the method. The direct digital implementation was utilized and the superiority shown with solid theory and experimental work. The publication by Vukosavic and Stefanovic is another example of re-invention for it repeats the work of Ogasawara et al. with no improvements and no recognition of the original invention [187]. Furthermore, Trzynadlowski and Legowski re-invented the same method for the second time [199].

In addition to establishing the 30° leading DPWM method (opposite to DPWM2), which provides minimum switching loss for 30° leading power factor loads, Kenjo developed an intuitive approach to describe the modulator behavior. Describing the inverter switch duty cycles in the three dimensional Cartesian coordinates, he illustrated the trajectories of different PWM methods, and the projection on a normal plane would correspond to the reference voltage vector in the inverter hexagon [90]. This method was later utilized in [181] for theoretical analysis of certain modulator characteristics.

In addition to the above described methods, several other methods with marginal improvement have been reported in the literature and several survey publications discuss these methods [68, 197]. The method by Kume et al. which provides controllable harmonic spectrum and reduces the carrier frequency sideband harmonics [111], the DPWM method by Taniguchi et al. which has a single 120° clamped segment (as opposed to $2 \times 60°$ clamped segments) [191], the DPWM method by Kolar et al. which has minimum harmonic distortion [107],

and the carrier frequency modulation method by Holtz and Beyer [72] are worth mentioning. Following the invention of SPWM, SVPWM, and DPWM methods the next natural step involved their implementation issues.

The early implementations largely involved analog hardware modulation signal generators and triangular carrier wave generators. In the early development years of the microprocessor technology several of the above modulation signals were often approximated with trapezoid etc. functions such that these signals could be successfully generated with the limited capability microprocessors of that time [23, 24, 25, 149, 198]. These methods could be implemented with the high performance microprocessors and electronic circuits available, and their superior performance was illustrated. However, cost and complexity were prohibitive in most practical applications [22, 129, 171]. However, the rapid progress in the microelectronics technology yielded high performance low cost microcontrollers, DSPs, and ASICs that could implement the high performance modulation methods with high precision [163]. Not only the modulation signal could be generated inside the IC chip, but also digital PWM counters/comparators could be integrated to it, rendering the analog triangular wave generator obsolete. As a result, the recent drives have incorporated high performance low cost digital microelectronic chips and with the implementation of the above discussed modulators superior performance could be obtained [29, 97, 141, 155]. Furthermore, more than two modulators could be incorporated into a single processor and intelligent modulator selection could yield superior performance. For example, in AC motor drive applications, in the low

speed region SPWM and in the high speed region a DPWM method could be employed and seamless transition from one modulation algorithm to another would yield an overall enhanced drive performance.

Although SPWM by Schönung and Stemmler, SVPWM by King, and DPWM1 by Depenbrock utilized simple rules to generate the modulation waves, the direct digital implementation methods have appeared more complex until recently. The calculations involved selection of an inverter hexagon sector, calculating the inverter active state time intervals, and converting to duty cycles. However, recently it has become obvious the earlier approach by King and Depenbrock were superior and have been preferred [50, 62, 63, 98].

In the early implementations, especially at power ratings in the order of tens of kilowatts and above, synchronization between the carrier and modulation signals was mandatory to achieve high waveform quality with the limited switching frequency capability of the inverters. However, the advent of BJT and IGBT devices allowed switching frequencies to become in the order of kilohertz and higher. Therefore, asynchronous PWM became acceptable in most drives except for high power drives and very high speed drives. With this constraint removed, the modulator implementation complexity of most drives has significantly reduced.

With the development of digital modulation methods, the discretization of the modulation signal resulted in a slightly different harmonic spectrum than

the analog (natural) sampling characteristic of analog triangle intersection implementation. These differences were investigated in detail and it was recognized the regular sampling characteristic of the discrete time modulation signals would yield a slightly less harmonic distortion [23, 24]. The performance characteristics of various modulators have also been recently investigated by employing analytical or numerical approaches. Thus, better understanding of the waveform characteristics, switching and conduction loss characteristics, voltage linearity characteristics, peak current stress characteristics, etc. has become possible [30, 31, 63, 68, 69, 107].

At the high power end, alternative to the programmed pulse modulation methods, synchronous PWM methods have been developed to eliminate the sub-fundamental frequency harmonic voltages which cause subsynchronous resonance problems at high power. Zubek et al. developed methods that can dynamically vary the carrier frequency in order to be able to operate in a wide modulation range and achieve smooth transition when changing the carrier to fundamental frequency ratio (also called gear changing)[211]. Utilizing synchronous PWM, they showed that the gear changing has to be at well defined points with respect to the fundamental component waveform in order to avoid unwanted transients. Stanke and Nyland recognized the performance superiority of pulse programmed modulation methods over the synchronous SPWM method in the high modulation region and developed an algorithm which selects SPWM in the low speed region and pulse programming method in the high modulation region. They demonstrated the transition between the two methods

could be achieved with minimum disturbance with the transition points being the peak of the modulation wave fundamental component peak values [185]. Further details were discussed in the publication by Richter [165]. High performance microprocessor implementation of the synchronous SVPWM method on a high power drive was reported in the late 1980s [112]. High performance DSPs and microcontrollers have been widely utilized in high power drives. The present high power drives benefit more from the advanced digital microelectronic technology than the medium and low power drives due to the significant performance to cost ratio levels achieved in high power drives.

As the above summary indicates, the PWM literature is rich and the large variety of methods and their performance characteristics are difficult to completely understand, evaluate and compare. Although the zero sequence signal injection principle is well understood and various high performance zero sequence signals have been developed, interpreting the differences and similarities between various methods has been substantially difficult. With many modulator re-invention examples illustrated in this chapter, the lack of global understanding has been solidly proven. Perhaps, the source of this difficulty lies in the fact that the number of modulators is large, and the waveform quality and switching loss characteristics of each modulator are multivariable functions.

One of the aims of this thesis is to simplify the modulator study task through grouping the methods and methodically analyzing and illustrating their important performance characteristics such as the switching loss, waveform quality,

and linearity. With the aid of rigorous analytical derivations (with simple results) and detailed graphics, the modulator characteristics will be better understood and recognition of the similarities and differences between various PWM methods will lead to a global vision of PWM. Perhaps, this approach will also aid the reader recognize the importance of the not-well-recognized early literature both from the future applications and historical perspective. Developing all the modulator characteristics and definitions with a coherent terminology will also simplify the analytical derivations involved in the remainder of this thesis. Although similar analytical and graphic methods were pursued by various researchers until the present time and the fundamental approach in modeling such characteristics has been established for more than a decade ago [29, 30, 31, 42, 146], lack of coherence and completeness have been a main deficiency [4, 37, 40, 62, 103, 104, 105, 106, 107, 114, 189]. Detailed comparative evaluation and intuitive illustration of the multivariable modulator characteristics through graphics has also not been provided. Therefore, in the modulator review and performance analysis chapter of this thesis, the emphasis will be on the principles and interpreting the results, not on illustrating the details of exhausting algebraic manipulations required for formula derivation.

Since the above discussed conventional modulators have predetermined performance characteristics, selecting a modulator and utilizing it over an operating range generally yields less than optimal characteristics. On the other hand, a modulator with controllable, rather than fixed characteristics would be preferable. This thesis pursues this issue also, and a novel high performance DPWM

method with superior performance characteristics is reported in the third and fourth chapter.

As a result of the above summarized exhaustive research in the PWM area, high performance modulation methods have been developed and todays AC drives widely utilize these matured modulation techniques. However, most of these modulation methods exhibit poor performance in the very high modulation range. For carrier based modulators, the region between the end point of linear modulation region, and the six-step operating point, which is defined as the overmodulation range, exhibits a complex nonlinear behavior. Since the maturation stage of the linear modulation technology, interest has recently been shifted towards understanding the modulator and drive behavior in the overmodulation region, and towards enhancing the drive performance in this region [54, 75, 93]. Being the focus of this thesis, the overmodulation subject will be surveyed and reviewed in the following separate section.

2.6 Inverter Overmodulation

Since the DC link voltage of a PWM-VSI drive has a finite value, the voltage linearity of a modulator is confined to a limited voltage range. Therefore, the reference voltage-output voltage relation of a PWM-VSI drive is linear until the reference voltage magnitude exceeds the modulator linearity limit. As shown in Fig. 2.5, for SPWM, when the reference voltage magnitude exceeds $\frac{V_{dc}}{2}$, or

equivalently 78.5 % of the six-step voltage fundamental component value, the sine-triangle intersections begin to disappear, and voltage pulses are dropped. Although during these intervals the corresponding upper switch operates with 100% duty cycle, it can not match the reference voltage and nonlinear relations result between the reference and output waveforms. The same condition repeats during the negative half of the cycle, and the large negative reference signal can not be matched by the inverter. The term "overmodulation" is adopted to distinguish this nonlinearity of a modulator and the "overmodulation region" is the voltage range beginning from where the nonlinearity begins and ending at the six-step operating point. Similar to SPWM, the other conventional modulators also have nonlinear gain relations in their overmodulation region. Although the range of linearity is wider for the popular zero sequence signal injection modulators, their linear voltage gain relations eventually ends at 90.7 % of the six-step voltage value. As a result, the controller reference voltage $|V^*|$ and the PWM-VSI output voltage $|V|$ are not equal in the overmodulation range of operation for all the conventional carrier based modulators. In addition to this fundamental component gain nonlinearity, the reference voltage and output voltage phase angles are nonlinearly related also. The implication of the phase and magnitude errors can be different and depend on the drive type.

In voltage feedforward controlled constant $\frac{V}{f}$ drives, entrance into the overmodulation region results in waveform quality degradation and voltage gain loss. As a result, the harmonic losses and the current/voltage stress on the VSI active and passive components increase. While in this region, the drive control

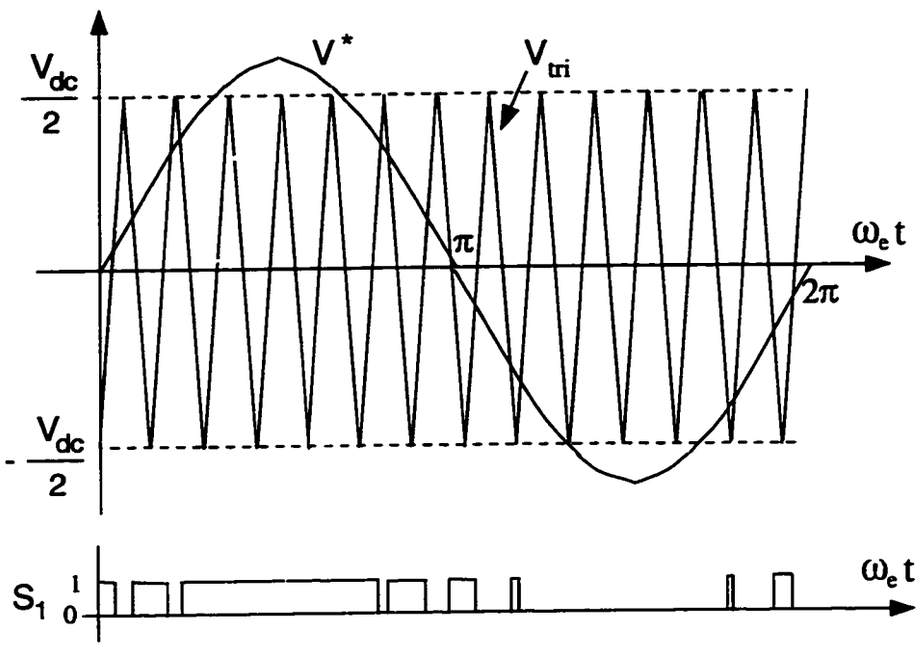

Figure 2.5: Voltage overmodulation mode modulator waveforms and switch signals in sinusoidal PWM.

linearity is lost and due to incorrect motor flux control ($\frac{V}{f}$ value deviates from $\frac{V^*}{f}$) poor performance results. In addition, rapid transition to/from the six-step operating mode results in large transients and frequent overcurrent fault conditions occur. In AC drives with large commutation time, eliminating narrow pulses in the overmodulation region can also cause substantial current transients and lead to drive failure [53]. Although the load side dynamics can be reduced by selecting the drive maximum acceleration/deceleration rate conservatively, DC link voltage disturbances such as line voltage sag conditions in a diode rectifier front end type PWM-VSI drives can not be predicted and avoided. If they occur, they result in transients and poor performance [93].

In current regulated drives, in the overmodulation region the drive torque and/or speed and/or position loop bandwidth is lost, the current waveform quality degrades more significantly than the voltage feedforward controlled drives, and poor and oscillatory performance results [12, 54]. Both on-off principle based and classical PI current controller based drives exhibit poor performance in this region. In an SFCR, the integral controller signals of the d and/or q channels may become significantly large (wind-up) and large settling times and significant overshoots deteriorate the performance. Furthermore, a drive overcurrent failure may occur. The performance can be only partially retained by employing anti-windup controllers. Therefore, operation in the overmodulation region is problematic. However, in current controller drives, operation in this region is inevitable. Since current controlled drives are required to provide precise performance under both mechanical load and AC line disturbances, their

overmodulation region performance requires more attention than the voltage feedforward drives. Furthermore, in high dynamic performance applications the overmodulation region is intentionally utilized in order to obtain maximum acceleration. In particular, at high speeds, where the machine back emf voltage is high and a little voltage margin remains for torque control, utilizing the overmodulation region voltage becomes significantly important. Therefore, the subject needs immediate attention.

To avoid undesirable operating conditions under disturbances, to obtain high steady state performance in the overmodulation range, and to obtain high dynamic performance during rapid acceleration/deceleration, the overmodulation range behavior must be well understood, and proper measures must be taken. If possible, from zero voltage to the six-step voltage the full voltage range should be available with maximum performance. However, the present drives do not have such capabilities, and their operating voltage range is constrained due to significant performance loss in the overmodulation range. Although most PWM issues have been significantly researched and reported over the last three decades, the overmodulation region performance issues have not been well recognized and the literature on this subject is scarce. Perhaps, this is due to the difficulty in modeling and understanding the overmodulation nonlinearity of the modulators. However, with the increasing demand for performance and following the maturization of the PWM technology (mainly, the linear mode) attention has recently been focused on the overmodulation subject. The relevant literature is discussed in detail in the following.

Following the recognition of the linearity limits of SPWM and the zero sequence signal injection principle based modulators [20, 101], the problematic behavior of the modulators in the overmodulation region was immediately recognized [53, 102]. Kliman and Plunkett recognized the waveform distortion of SPWM in the overmodulation range and introduced a modification to the modulation waves to improve the current waveform quality [102]. Grant investigated the problems in operating the constant $\frac{V}{f}$ drives in the overmodulation range. He illustrated that abrupt pulse dropping in the overmodulation region could induce significant current transients. He developed a pulse limiting method where the narrowing voltage pulses are held at a minimum value and shifted to the sides of the modulation wave such that the adverse effects of the narrow pulses could be reduced [53].

Rowan et al. investigated the SPWM modulator nonlinearity and utilized the fundamental component voltage gain formula to analyze the current controlled drive overmodulation region behavior [169]. They utilized the SPWM gain function [147] to evaluate the performance of the stationary PI current regulator and SFCR to predict the drive behavior in the overmodulation range. They demonstrated that associated with the gain loss, both current regulators exhibited degraded performance. However, the stationary regulator performed poorly compared to SFCR in the overmodulation range.

Xu and Novotny studied the overmodulation issues by simulating several current regulator structures in the high modulation range and indicated that

on-off current regulators which operate on an instantaneous basis provide less voltage utilization than those that modulate by accounting for the full fundamental cycle [205]. Through experiments and simulation studies, they showed that the on-off regulators have significant phase delay and magnitude error. They indicated increasing the switching frequency of an on-off current regulator increases bus utilization. They also recognized the influence of the induced EMF voltage on the current regulator performance, and suggested that for carrier based PWM, the feedforward command increases the bus utilization.

Holtz et al. developed a space vector based feedforward PWM method for the overmodulation operating range [75]. The method divides the overmodulation region into two sub regions, each of which has a unique overmodulation characteristic (space vector trajectory). Similar to [169], the work focuses on the per fundamental cycle characteristic. Therefore, the fundamental component gain concept is implied. In this modulation method the reference voltage vector is pre-processed through a look-up table based gain and/or angle adjuster. In the first overmodulation region, only the magnitude of the reference vector is modified and it is multiplied by a gain and the resulting vector is processed by the conventional space vector modulator. In the second region both the angle and magnitude of the reference are modified by the pre-processor and then the resulting vector is processed by the conventional modulator. The method is computationally complex, requires a mode selection loop and relatively large look-up tables. Essentially being a fundamental component gain adjuster, the method has dynamic performance limitations, therefore it is not suitable for

current controlled drive applications. However, the space vector approach is very attractive from the perspective of vectorially illustrating the overmodulation range behavior of VSIs. Through vector diagrams, the voltage limit of the inverter becomes geometrically visible, and intuition can be gained on the overmodulation range behavior.

Recognition of SVPWM as a superior modulation method which fully utilizes the inverter voltage hexagon [29] has been followed by the development of several space vector overmodulation methods. Gaining intuition from the inverter hexagon geometry, several researchers developed various overmodulation methods for both voltage feedforward and current controlled drives.

The vector space based overmodulation method developed by Habetler et al. selects the largest voltage vector that is aligned with the reference vector (minimum angle error method) [57, 58] and it was utilized in a dead beat current controlled drive. Another intuitive approach developed by Mochikawa et al. selects the voltage vector that is vectorially closest to the reference (minimum magnitude error method) [131] by projecting the reference voltage vector tip point on the closest inverter hexagon side. The one step optimal control characteristic of this approach was later recognized by Seidl et al. [181], and the authors developed a neural network hardware implementation as opposed to the original implementation which involved computation of the algebraic exact equations by numeric approximation. While the minimum angle error method

is limited in voltage capability (its output voltage is less than 95 % of the six-step voltage), the minimum magnitude error method requires additional neural network hardware circuit or a high performance signal processor.

Jul-Ki and Sul compared the above discussed two graphic methods and developed a method with superior performance characteristics [88]. In this method, the vector formed by the superposition of the feedforward voltage vector and the PI current controller output vector is intersected with the hexagon side. The intersection point of the PI controller vector with the hexagon side defines the tip point of the modified reference voltage vector. In an induction motor application, this approach typically yields a vector which is located in between the minimum magnitude error vector and minimum angle error vector. The method has better performance than the other methods. However, it is complex and its performance improvement over the previous two is not significant.

Another intuitive method which was proposed by Tenti et al. [192], projects the reference vector tip point on the inverter voltage vector closer to the reference vector. The point on the hexagon side which the projection line intersects is selected to be the modified reference vector. The method is inferior to the one step optimal method and its implementation difficulty is comparable.

Kerkman et al. utilized the nonlinear inverter gain function model to remove the adverse effect of the nonlinear gain on the regulator performance by multiplying the inverter gain by its exact inverse which is calculated from the gain

formula and stored in a look up table [91, 93]. They applied this principle to voltage feedforward type regulators and to the feedforward channel of the current regulators. They illustrated that the gain compensation method enhances the DC bus voltage disturbance characteristics and improves the overmodulation region performance. They showed that the modulator would have similar switching patterns to the pattern of the feedforward method suggested by Holtz et al. [75].

Similar to some of the developments of this thesis, a couple most recent publications investigate the modulator overmodulation characteristics [59, 60, 161]. The work by Pop and Kelemen investigates the harmonic characteristics and the narrow pulse issues of DPWM methods and compare to other methods [161]. However, no in depth analysis is provided. Haras also recognizes this issue [59, 60], and also focuses on the space vector overmodulation method developed in [75]. However, this work also has limited focus and in particular the influence of the modulator characteristics on the drive performance has not been recognized, and the modulator characterization study is superficial.

Recently in Europe several studies on the high modulation range (including overmodulation range) performance issues of high power traction drives have been investigated in detail [8, 48, 185]. In such drives in the low speed range synchronous SPWM or SVPWM method is utilized. As the speed sufficiently increases transition to pulse programmed optimal PWM methods, and as the speed further increases transition to the six-step mode follows. Since in such

drives the switching frequency is limited, typically transition from one method or one voltage level to the next may result in large current spikes and oscillatory behavior. Therefore, sophisticated transitioning methods have been established and relatively smooth transition to/from six-step mode of such drives has been achieved [8, 48, 185]. In most such methods transition is allowed to occur at specific angles with respect to the inverter hexagon, hence the dynamic performance is constrained. The fundamental component current measurement is an issue and involved estimation methods are employed to calculate its value for closed loop current control [48, 70, 71, 73, 185]. Although the current control loop bandwidth is low due to the measurement/estimation delays, it is sufficient in FOC controlled high power drive traction applications with no stringent dynamic performance requirements [47, 48, 185]. However, these methods are not suitable for industrial and servo drives with demanding dynamic performance characteristics and stringent controller cost and performance limitations.

In addition to the above summarized important publications, there have been several other publications involving overmodulation. Employing the complex variable Fourier analysis, Bolognani and Zigliotti analytically re-investigated the voltage vector overmodulation characteristics [18, 19] previously reported in [75] and utilized numerical data to characterize the modulator phase and magnitude functions. Another similar approach was recently reported in [116]. Yasuda et al. re-invented the SPWM voltage gain characteristic [207] and gain compensation method which was reported in [93, 91]. Assuming the overmodulation nonlinearity is a difficult to model complex function, a fuzzy overmodulation

control algorithm was developed in [95].

The above summary of the overmodulation literature indicates continuous and rapid progress in this area. Most of the discussed literature involves the modulator steady state voltage gain characteristics which is generally meaningful for voltage feedforward controlled drives. In particular, the complex plane (space vector) illustration has been widely utilized to analyze the modulator characteristics and to invent new overmodulation methods. However, the overmodulation characteristics of modern triangle intersection PWM methods have not been well understood (with the exception of SPWM). The waveform quality and the fundamental component voltage gain characteristics are not thoroughly analyzed and the behavior is not well understood.

In most of the above summarized publications overmodulation in current controlled drives has not been considered. The overmodulation range performance degradation of current controlled drives has been recognized [205, 169]. However, the literature involving performance study of such drives and techniques to enhance the performance is limited. Voltage margin control methods have been proposed for FOC drives so that overmodulation is avoided as much as possible during field/flux weakening [99, 100, 180]. In these methods the synchronous frame d and q axis voltages are partitioned in a manner to maintain current controller performance. Accounting for the load back emf, these methods allocate a direct axis voltage margin for maintaining the torque producing current controllability and maximize the torque output of vector controlled

drives. They also improve the disturbance rejection characteristics of FOC drives[180]. However, rapid acceleration and abrupt DC bus and load torque disturbances often result in entrance to the overmodulation region.

The overmodulation region behavior of FOC based induction motor drives employing the minimum magnitude error and minimum phase error PWM methods was studied, and a superior overmodulation method was reported in [88, 182]. Also two overmodulation region current control methods with superior performance have recently been developed by Choi and Sul [35, 36]. The minimum time current controller involves a transient time minimization algorithm with given inverter voltage and current boundaries recognized. Involved computations yield the optimal d and q axis voltage references which are on the inverter hexagon boundary[36]. In the cross-coupling current controller, during overmodulation the q axis current error of the SFCR is subtracted from the d axis current reference in order to maintain the torque capability of the drive [35]. In an induction motor application this approach yields dynamic field weakening, and performance is retained as much as possible during transients.

The recently reported and above summarized current controlled drive overmodulation studies are limited in scope, and many performance and implementation issues are open to detailed investigations. In the modern triangle-intersection PWM methods, the interaction between the current controller and the modulator has not been recognized or investigated in detail. The steady

state and dynamic overmodulation performance characteristics of current controlled drives are not well understood. Therefore, the investigation of such characteristics and development of advanced methods is mandatory. The overmodulation chapters of this thesis will attempt to address these and the previously described issues of open loop voltage feedforward controlled drives with rigorous theoretical study and detailed experimental work.

2.7 Summary

This chapter provided a detailed literature survey of inverter drives with emphasis on the modulators and control methods. It has become obvious the inverter drives technology has gone through several major breakthroughs and revolutionized the industrial processes with magnificent performance advancements. With a lot more than a handful of books including at least a sizable chapter on PWM and drives [21, 85, 89, 90, 108, 118, 132, 136, 196, 202, 203], and thousands of articles on PWM and drives in existence, the subject has still not reached a full maturation stage. Due to the significant flexibility in controlling the inverter switches, large number of switching algorithms were developed and some of these have gained wide acceptance and fully developed. However, the performance of modern drives utilizing the modern modulation and control methods is limited. In particular, the overmodulation region performance is poor and further progress is inevitable.

This thesis develops advanced modulation methods and control algorithms with superior energy efficiency, low harmonic distortion, and high dynamic performance. In particular, the overmodulation region performance is investigated in detail.

Before establishing the advanced PWM methods and control algorithms, a detailed review of carrier based PWM methods is provided in the following chapter. This review intends to prepare the reader to the following chapters which involve detailed knowledge of the important PWM methods and their performance characteristics. A novel high performance DPWM method is also introduced in the chapter.

Chapter 3

Review of Carrier Based PWM Methods and Development of Analytical PWM Tools

3.1 VSI Operation and The Volt-Seconds Principle

Shown in Fig. 3.1, the basic circuit structure of the VSI is relatively simple. Each inverter leg consists of two self commutated switching devices (gate turn-on and turn-off devices such as MOSFET, IGBT, GTO, and MCT) with reverse parallel diodes which are often termed as the feedback diodes. In three phase sinusoidal power applications, except during the drive stand-by mode, power-off mode, and blanking periods (also termed as dead time), the upper and lower devices are always gated with complementary logic signals. During commutation both devices are disabled for a short blanking time to avoid short circuit condition across the DC voltage source. Considering the blanking time and the

commutation time are significantly shorter than the normal operating duty cycle of the switches, the switching devices can be assumed ideal in most PWM-VSI performance analysis studies. Since in each inverter leg the switches operate in a complementary manner, under normal operating conditions, at any time three switches are simultaneously in "on state," and three switches are in "off-state." In each inverter leg, depending on the polarity of the associated phase current, either the "on-state" switching device or its reverse parallel diode conducts the current. Combining the possible switch "on" or "off" states, eight unique inverter states are distinguished. These inverter states are generally described with the upper switch Boolean logic signals (Sa+, Sb+, Sc+), and "1" corresponds to on-state condition while "0" corresponds to off-state condition. Of the eight possibilities, (000) and (111) short circuit the output terminals of the three phase load and yield a zero output voltage. Hence they are termed the zero states. The remaining six states are termed active states and numbered with the decimal equivalent of their boolean states.

With its simple structure and switching constraints described above, the VSI generates a low frequency output voltage with controllable magnitude and frequency by programming high frequency voltage pulses. Of the various pulse programming methods, the carrier based PWM methods are the preferred approach in most applications due to the low harmonic distortion waveform characteristics with well defined harmonic spectrum, the fixed switching frequency, and implementation simplicity.

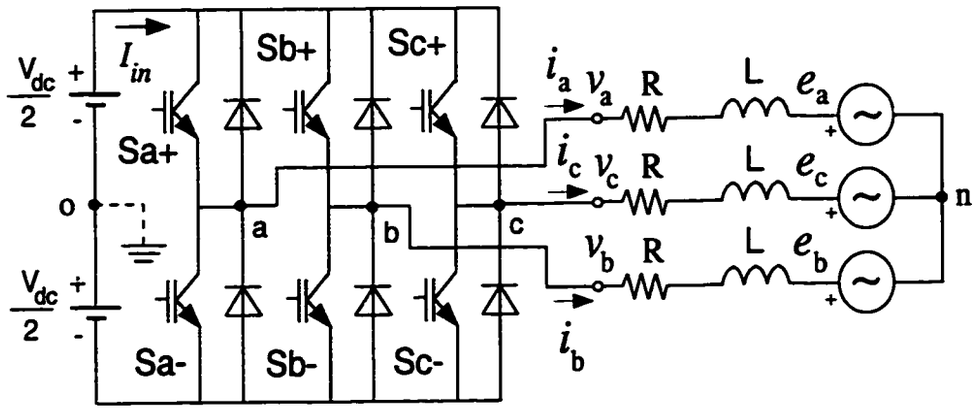

Figure 3.1: Circuit diagram of a PWM-VSI connected to an R-L-E type load.

Carrier based PWM methods employ the "per carrier cycle volt-second balance" principle to program a desirable inverter output voltage waveform. According to this principle, a sequence of inverter states is generated over a carrier cycle in a manner that for each phase the average value of the rectangular pulse output voltage approaches its reference voltage value. This principle has been utilized in DC/DC converters for a long time and is commonly termed as duty cycle control, or PWM control. However, its application to three phase VSI's is not as intuitive as the DC/DC converters. PWM-VSI modulator design and implementation is also substantially more complex than the DC/DC converter duty cycle controllers. This is so, because in a three phase PWM-VSI, the duty cycle of each switch is time variant both under steady state and dynamic operating conditions. In addition, the inverter output line-to-line voltages can not be independently controlled by any switch, i.e. the VSI is a coupled system. Therefore, a detailed modulator study requires a knowledge of both microscopic

(per carrier cycle) and macroscopic (over a fundamental cycle) behavior. Following the description of two carrier based PWM implementation techniques, the microscopic and macroscopic views will be provided.

Two main carrier based PWM implementation techniques exist: the triangle intersection technique and the direct digital technique. In the triangle intersection technique, for example in the Sinusoidal PWM (SPWM) method [177], as shown in Fig. 3.2, the reference modulation wave is compared with a triangular carrier wave and the intersections define the switching instants. Within every carrier cycle, the average value of the output voltage becomes equal to the reference value. In particular, in the digital implementation which employs the regular sampling technique, this result becomes obvious as the reference volt-seconds precisely equals the output volt-seconds. This principle is illustrated in Fig. 3.3 in detail. In the regular sampling technique, the modulation signals are sampled/output at the positive (and/or negative) peak of the triangular carrier cycle and held constant for the remainder of the carrier cycle. Although the early triangle intersection implementations mostly involved analog hardware circuits, the advent of low cost digital electronics rendered the analog solutions obsolete. Most present triangle intersection implementations involve high resolution digital PWM counters and comparators. Therefore, in this work the term triangle intersection is generally not associated with the analog implementations, and typically digital implementation is implied.

The direct digital implementation involves the space vector theory [108].

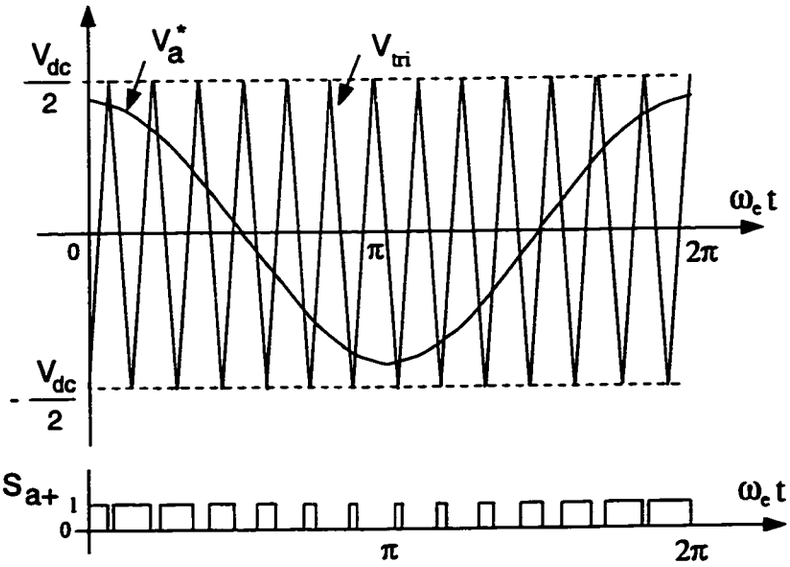

Figure 3.2: Triangle intersection PWM phase "a" modulation and switching signals.

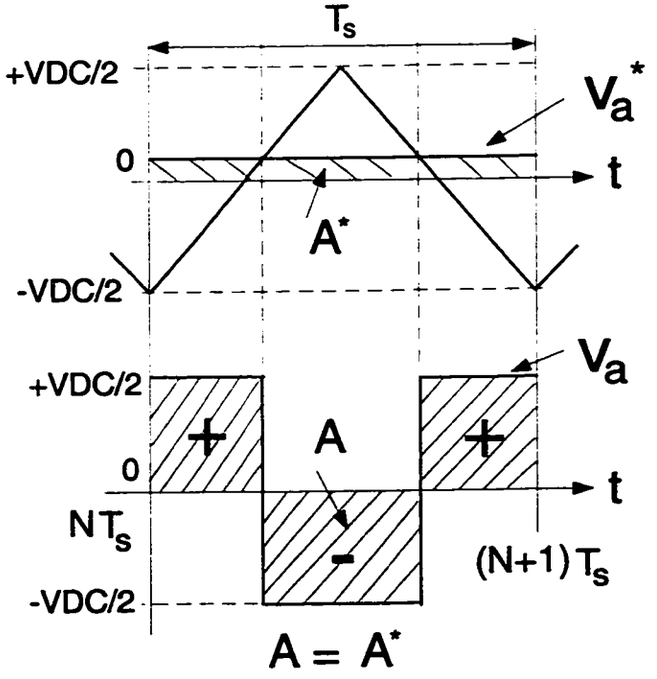

Figure 3.3: An illustration of the per carrier cycle volt-second balance principle.

The space vector theory employs the following complex number transformation which transforms the three phase time domain variables x_a, x_b, x_c, to a time parametric complex number variable, i.e. a space vector X.

$$X = \frac{2}{3}(x_a + ax_b + a^2x_c) \tag{3.1}$$

In the transformation equation "a" represents the conventional 120° rotation operator, $e^{j\frac{2\pi}{3}}$, and "j" represents the imaginary axis unit. Applying this transformation to the seven discrete inverter states, the inverter voltage vectors, and the hexagon which the tip points of these vectors form are obtained. The inverter voltage vectors and the hexagon are illustrated in Fig. 3.4 in detail. This diagram is commonly termed as the space vector diagram. Applying the transformation to the three phase voltage references generated by the controller of a PWM-VSI drive, a reference voltage vector is also obtained. In the direct digital approach, the time integral of the reference voltage vector and the time integral of a selected sequence of inverter voltage vectors over a carrier cycle are equated. Of the available inverter voltage vectors, the two zero states and the two vectors adjacent to the reference voltage vector are selected to match the reference volt-seconds. The volt-second balance calculation gives the total time length of each adjacent inverter state and the total zero state time length [29, 158]. Figure 3.4 graphically illustrates the complex number volt-second balance in detail. Once the inverter state time lengths are determined, the number and sequence of commutations are selected by the user. Finally, the

switch duty cycles are calculated from the data and loaded to the digital PWM counters to generate the selected output voltages. Since the approach does not involve a modulation signal, it is often termed as the direct digital approach, and this term will be adopted in the remainder of this thesis. Note in this method the duty cycles are precalculated for each carrier cycle, and therefore the regular sampling technique is implied. In both direct digital and triangle intersection methods, with the volt-second balance principle being quite simple, a variety of PWM methods have appeared in the technical literature; each method results from a unique placement of the voltage pulses in isolated neutral type loads. Following a modulation index definition, which will be immediately utilized, the freedom in placing voltage pulses in isolated neutral type loads will be discussed in detail.

Modulation Index: Since the performance characteristics of a modulator are primarily dependent on the voltage utilization level, i.e. modulation index, it is helpful to define a modulation index term at this stage. For a given DC link voltage V_{dc}, the ratio of the fundamental component magnitude of the line to neutral inverter output voltage, V_{1m}, to the fundamental component magnitude of the six-step mode voltage, $V_{1m6step}$, is termed the modulation index M_i [68]:

$$M_i = \frac{V_{1m}}{V_{1m6step}} \tag{3.2}$$

$$V_{1m6step} = \frac{2V_{dc}}{\pi} \tag{3.3}$$

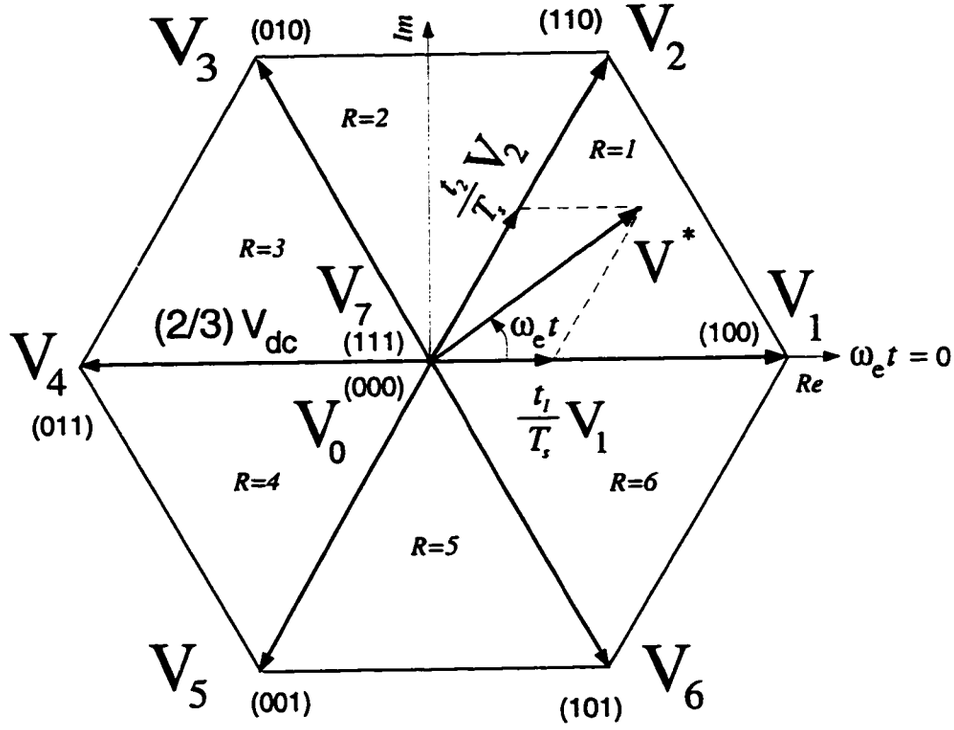

Figure 3.4: The space vector diagram illustrates the direct digital PWM technique implementation principle.

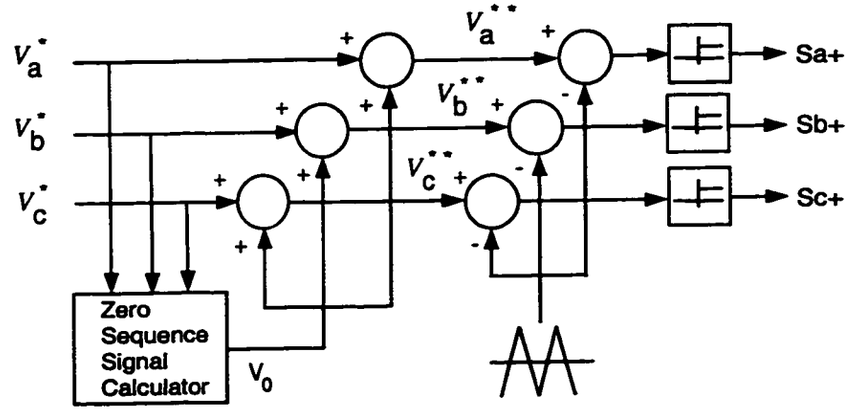

Figure 3.5: The generalized signal block diagram of the triangle intersection technique based PWM employing the zero sequence injection principle.

3.2 The Zero Sequence Signal Injection Principle

In most three phase AC motor drive and utility interface applications the neutral point is isolated and no neutral current path exists. In such applications the neutral voltage can be different from zero. Therefore, in the triangle intersection implementations any zero sequence signal can be injected to the reference modulation waves. Possibly K. G. King was the first researcher to utilize this concept in a voltage source inverter [101]. In the zero sequence signal injection technique, the n-o potential in Fig. 3.1 which will be symbolized with v_0 can be freely varied. This degree of freedom is illustrated in Fig.3.5 with the generalized modulator signal diagram. A properly selected zero sequence signal can extend the volt-second linearity range of SPWM. Furthermore, it can improve the waveform quality and reduce the switching losses significantly. Recognizing these properties, many researchers have been investigating the zero sequence signal dependency of the modulator performance and a large number of PWM methods with unique characteristics have been reported [68]. Detailed research showed the freedom in selecting the partitioning of the two zero states "0" (000) and "7" (111) in the direct digital PWM technique is equivalent to the freedom in selecting the zero sequence signal in the triangle intersection PWM technique [29, 146].

Although it does not affect the inverter line-to-line voltage per carrier cycle

average value, the zero sequence signal of a modulator significantly influences the switching frequency characteristics. Therefore, the per carrier cycle (microscopic) characteristics of different modulators are important and must be accurately modeled and carefully analyzed.

As shown in Fig. 3.6 in the triangle intersection method, the modulation signals are compared with the triangular carrier wave and the intersection points define the switching instants. The duty cycle of each switch can be easily calculated in the following.

$$d_{Sx+} = \frac{1}{2}(1 + \frac{v_x^{**}}{\frac{V_{dc}}{2}}) \qquad for \qquad x \in \{a, b, c\} \tag{3.4}$$

$$d_{Sx-} = 1 - d_{Sx+} \qquad for \qquad x \in \{a, b, c\} \tag{3.5}$$

With the modulation waveforms defined with the following cosine functions, the $w_e t$ time axis of the modulation waves and complex plane reference voltage vector angle $w_e t$ coincide.

$$v_a^{**} = v_a^* + v_0 = V_{1m}^* \cos(w_e t) + v_0 \tag{3.6}$$

$$v_b^{**} = v_b^* + v_0 = V_{1m}^* \cos(w_e t - \frac{2\pi}{3}) + v_0 \tag{3.7}$$

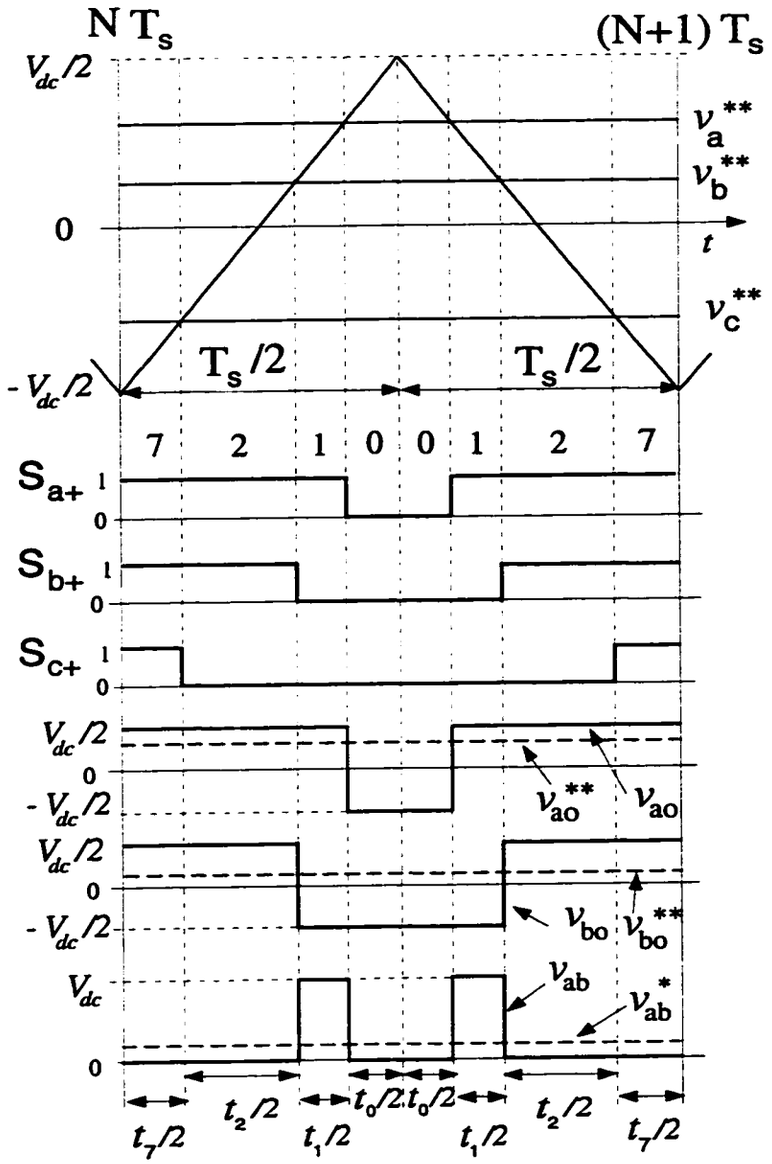

Figure 3.6: The per carrier cycle view of switch logic signals, inverter states, and VSI output voltages for $0 \leq w_e t \leq \frac{\pi}{3}$ $(R = 1)$.

$$v_c^{**} = v_c^* + v_0 = V_{1m}^* \cos\left(w_e t + \frac{2\pi}{3}\right) + v_0 \tag{3.8}$$

For the above defined modulation functions and $0 \leq w_e t \leq \frac{\pi}{3}$, the inverter states of the triangle intersection PWM methods are 7-2-1-0-0-1-2-7 as shown in Fig. 3.6. This symmetric switching sequence is superior to other sequences due to its low harmonic distortion characteristic. Therefore, this sequence is adopted in the direct digital methods also [29]. As will be later discussed in detail, either the two "7" states at both ends of the carrier cycle, or the "0" states in the middle are often omitted to further reduce the commutation count and therefore to reduce the average switching frequency. The zero state to be eliminated is the state which reduces the switching losses more than the other zero state [146]. Notice that in Fig. 3.6, a zero sequence signal simultaneously shifts the three reference signals in the vertical direction and while it changes the position of the output line-to-line voltage pulses, it does not affect their width. The time length of the active and zero states of the triangle intersection methods are not explicitly calculated in the algorithm. However, for analysis purposes they can be directly calculated from the duty cycle information; Figure 3.6 illustrates these relations. However, in the direct digital technique, the inverter state time lengths are directly calculated employing space vector theory and Zero State Partitioning (ZSP) is selected by the programmer.

In the space vector approach, employing the complex variable transformation, the time domain modulation signals are translated to the complex reference

voltage vector which rotates in the complex coordinates at the $w_e t$ angular speed in the following.

$$V^* = \frac{2}{3}(v_a^* + a v_b^* + a^2 v_c^*) = V_{1m}^* e^{j w_e t} \quad where \quad a = e^{j\frac{2\pi}{3}} \tag{3.9}$$

The complex number volt-second balance equation in the R'th sector of the hexagon in Fig. 3.4 determines the time length of the two adjacent state active inverter states R and $R+1$ ($R = 6 \rightarrow R+1 = 1$) and the total zero state time length in the following.

$$V_R t_R + V_{R+1} t_{R+1} = V^* T_s \tag{3.10}$$

$$t_R = \frac{2\sqrt{3}}{\pi} M_i \sin(R\frac{\pi}{3} - w_e t) T_s \tag{3.11}$$

$$t_{R+1} = \frac{2\sqrt{3}}{\pi} M_i \sin(w_e t - (R-1)\frac{\pi}{3}) T_s \tag{3.12}$$

$$t_0 + t_7 = T_s - t_R - t_{R+1} \tag{3.13}$$

Defined by the following, ZSP of the two inverter zero states, ζ_0 and ζ_7, provides the degree of freedom in the direct digital technique [146].

$$\zeta_0 = \frac{t_0}{t_0 + t_7} \tag{3.14}$$

$$\zeta_7 = 1 - \zeta_0 \tag{3.15}$$

In order to simplify the analytical investigations, the inverter state time lengths can be expressed in terms of per carrier cycle or per half carrier cycle duty cycle in the following.

$$d_R = \frac{t_R}{T_s} = \frac{t_R/2}{T_s/2} \qquad for \qquad R \in \{0, 1, ..., 7\} \tag{3.16}$$

With the degree of freedom in the triangle intersection PWM being the v_0 signal, and in the direct digital technique the ζ_0 partitioning, the modern PWM methods are discussed next.

3.3 Modern PWM Methods and The Magnitude Rules

Although theoretically an infinite number of zero sequence signals and therefore modulation methods could be developed, the performance and implementation constraints of practical PWM-VSI drives reduce the possibility to a small number. Over the last three decades of PWM technology evolution, about ten high

performance carrier based PWM methods were developed and of these only several have gained wide acceptance. Figure 3.7 illustrates the modulation and zero sequence signal waveforms of these modern triangle intersection PWM methods. In the figure, unity triangular carrier wave gain is assumed and the signals are normalized to $\frac{V_{dc}}{2}$. Therefore, $\pm\frac{V_{dc}}{2}$ voltage saturation limits correspond to ± 1. In the figure only phase "a" modulation wave is shown, and the modulation signals of phase "b" and "c" are identical waveforms with 120° phase lag and lead with respect to phase "a."

The modulators illustrated in Fig. 3.7, can be separated into two groups. In the Continuous PWM (CPWM) methods, the modulation waves are always within the triangle peak boundaries. Within every carrier cycle, the triangular carrier wave and the modulation wave intersect and therefore on and off switchings occur. In the Discontinuous PWM (DPWM) methods, the modulation wave of a phase has at least one segment which is clamped to the positive and/or negative DC rail for at most a total of 120° (over a fundamental cycle). Therefore, within such intervals the corresponding inverter leg discontinues modulation. Since no modulation implies no switching losses, the switching loss characteristics of CPWM and DPWM methods are different. Detailed studies indicated the waveform quality and linearity characteristics are also significantly different. Therefore, this classification aids in distinguishing the important differences between CPWM and DPWM methods.

Of the four modern CPWM methods shown in Fig. 3.7, the SPWM method

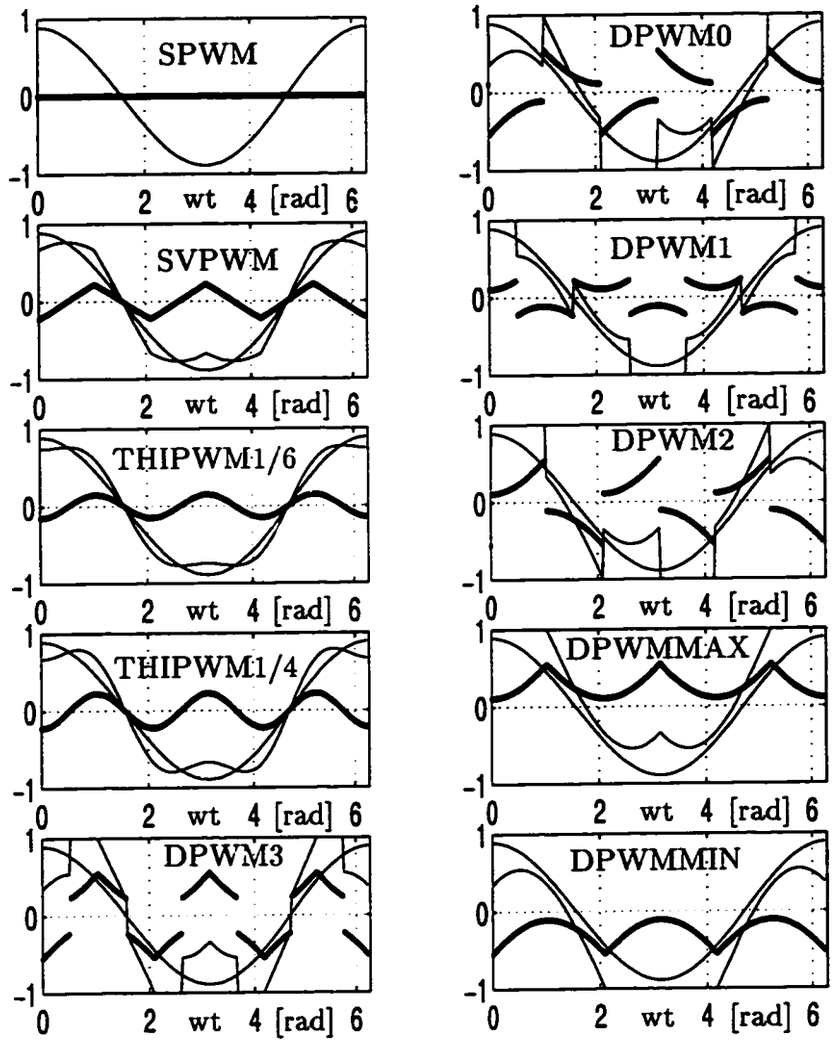

Figure 3.7: Modulation waveforms of the modern PWM methods ($M_i = 0.7$).

[177] is the simplest modulator with limited voltage linearity range and poor waveform quality in the high modulation range. The triangle intersection implementation of the Space Vector PWM (SVPWM) method and the two Third Harmonic Injection PWM (THIPWM) methods are the remaining three popular CPWM methods. These modulators are discussed in the following.

THIPWM: Due to the simplicity of algebraically defining their zero sequence signals, these modulators have been frequently discussed in the literature. With v_a^* defined as in (3.6), the zero sequence signal of THIPWM1/6 is $v_0 = -\frac{V_{1m}}{6}\cos 3w_e t$ [32] and for THIPWM1/4, $v_0 = -\frac{V_{1m}}{4}\cos 3w_e t$ [24] is selected. Both methods suffer from implementation complexity, because generating the $\cos 3w_e t$ signal is difficult both with hardware and software. Trigonometric identities can be utilized to compute $\cos 3w_e t$ from the $\cos w_e t$ signal, however the computational intensity (several multiplications are required) results in loss of significance by several bits and poor resolution is obtained in signal processors with limited wordlength. Often, a large look-up table is employed to store the base function of such modulators and the modulation signals are on-line accessed from this table to compute the modulation signals. Although the THIPWM1/4 has theoretically minimum harmonic distortion, it is only slightly better than SVPWM and has a narrower voltage linearity range [68, 105]. With their performance being very similar to SVPWM and implementation complexity significantly higher, both THIPWM methods have academic and historical value, but little practical importance. Also note when higher order triplen harmonics are added to the THIPWM1/6 signal (such as $\frac{V_{1m}}{9}\cos 9w_e t$), the zero sequence signal

approaches a triangle and the resulting modulation signal approaches SVPWM.

SVPWM [101, 29]: The zero sequence signal of SVPWM is generated by employing the minimum magnitude test which compares the magnitudes of the three reference signals and selects the signal with minimum magnitude [50]. Scaling this signal with 0.5, the zero sequence signal of SVPWM is found. Assume $|v_a^*| \leq |v_b^*|, |v_c^*|$, then $v_0 = 0.5 \times v_a^*$. The analog implementation of SVPWM which employs a diode rectifier circuit to collect the minimum magnitude signal from the three reference signals (was shown in Fig. 2.4) is possibly the earliest zero sequence signal injection PWM method reported [101]. About a decade later, this modulator re-appeared in the literature with direct digital implementation [29]. Since the direct digital implementation utilized the space vector theory, the method was named SVPWM. In addition to its implementation simplicity, the SVPWM method has superior performance characteristics (compared to all other CPWM methods) and is possibly the most popular high performance PWM method. However, its high modulation range performance is inferior to DPWM methods, which also employ similar magnitude rules to generate their modulation waves. In the following the modern DPWM methods and their magnitude rules are summarized.

DPWM1 [42, 178]: The reference signal with the maximum magnitude defines the zero sequence signal. Assume $|v_b^*|, |v_c^*| \leq |v_a^*|$, then $v_0 = sign(v_a^*)\frac{V_{dc}}{2} - v_a^*$. This method has minimum switching losses at unity power factor operating condition, and its waveform quality at high modulation is superior to

SVPWM [42].

DPWM2 [107, 146]: All three reference modulation signals v_a^*, v_b^*, and v_c^* are phase shifted by 30° (lagging), and of the three new signals v_{ax}^*, v_{bx}^*, and v_{cx}^*, the one with the maximum magnitude determines the zero sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (sign(v_a^*))\frac{V_{dc}}{2} - v_a^*$. Adding this zero sequence signal to the three original modulation waves v_a^*, v_b^*, and v_c^*, the DPWM2 waves v_a^{**}, v_b^{**}, and v_c^{**} are generated. This method has minimum switching losses at 30° lagging power factor operating condition, and its waveform quality at high modulation is superior to SVPWM [146].

DPWM0 [90, 107]: All three reference modulation signals v_a^*, v_b^*, and v_c^* are phase shifted by 30° (leading), and of the three new signals v_{ax}^*, v_{bx}^*, and v_{cx}^*, the one with the maximum magnitude determines the zero sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (sign(v_a^*))\frac{V_{dc}}{2} - v_a^*$. Adding this zero sequence signal to the three original modulation waves v_a^*, v_b^*, and v_c^*, the DPWM0 waves v_a^{**}, v_b^{**}, and v_c^{**} are generated. This method has minimum switching losses at 30° leading power factor operating condition, and its waveform quality at high modulation is superior to SVPWM [90, 107].

DPWM3 [105]: The reference signal with the intermediate magnitude defines the zero sequence signal. Assume $|v_b^*| \leq |v_a^*| \leq |v_c^*|$, then $v_0 = sign(v_a^*)\frac{V_{dc}}{2} - v_a^*$. This method has low harmonic distortion characteristics [105].

DPWMMAX [191]: The reference signal with the maximum value defines the zero sequence. Assume $v_b^* \leq v_a^* \leq v_c^*$, then $v_0 = \frac{V_{dc}}{2} - v_c^*$ yields and phase

"c" is unmodulated [191].

DPWMMIN [105]: The reference signal with the minimum value defines the zero sequence. Notice the DPWMMAX and DPWMMIN methods have nonuniform thermal stress on the switching devices and in DPWMMAX the upper devices have higher conduction losses than the lower, while in DPWMMIN the opposite is true.

All the magnitude tests require a small number of computations and therefore can be easily implemented in a microcontroller or DSP. Due to the simplicity of the algorithms, it is easy to program two or more methods and on-line select a modulator in each operating region in order to obtain the highest performance [62, 69]. Similar to SVPWM analog implementation of King [101] and DPWM1 analog implementation of Depenbrock [42], analog or digital hardware implementations of the remainder of the discussed modulators can be easily developed by following the magnitude test computational procedures.

With the exception of THIPWM and SPWM methods, all the above discussed triangle intersection PWM methods can be easily implemented in the direct digital method. Mapping the zero state partitioning of the time domain modulation waves of Fig. 3.7 onto the vector space domain, the direct digital implementation equivalents can be easily obtained. This mapping is illustrated in Fig. 3.8 in detail. Assuming the fundamental component modulation signals of the three phases are cosine functions in time, the origin in the time domain is mapped to the real axis of the complex plane. Therefore, with the aid of

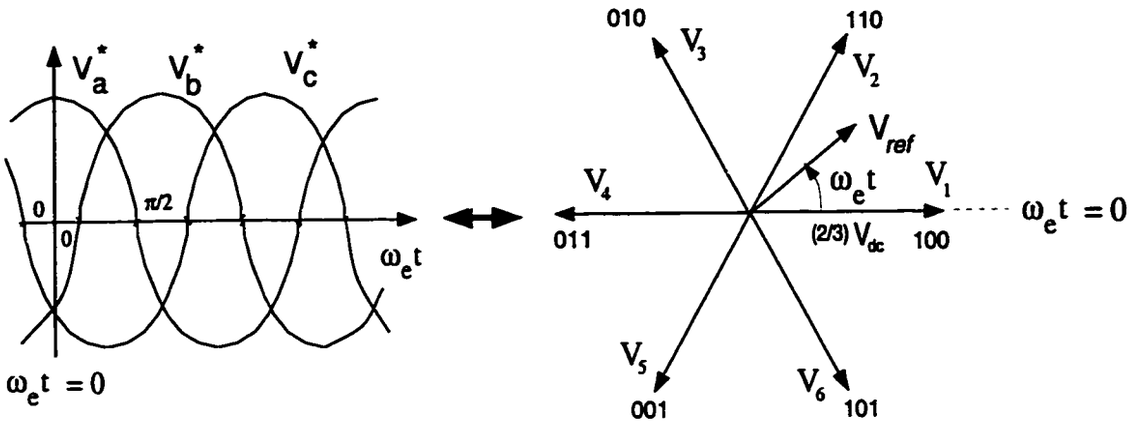

Figure 3.8: Time to complex coordinate mapping aids illustrating the equivalency between the direct digital and triangle intersection PWM methods.

this mapping, the ZSP of each triangle intersection PWM method can be identified. Figure 3.9 illustrates this equivalency and the ZSP of each method. A clear illustration of this equivalency is an important step towards simplifying the learning process.

Due to its simplicity, the magnitude test is a very effective tool for simulation, analysis, and graphic illustration of various modulation methods. For example, the simulation or DSP implementation of the SVPWM method with a direct digital technique is involved: the sector to which the voltage vector belongs has to be identified first, then the time length of each active vector must be calculated, and finally gate pulses must be generated in a correct sequence [29]. Although it is possible to reduce the direct digital PWM algorithms, the effort does not yield as simple and intuitive a solution as the magnitude test [98, 175]. Therefore, employing the magnitude test the triangle intersection PWM

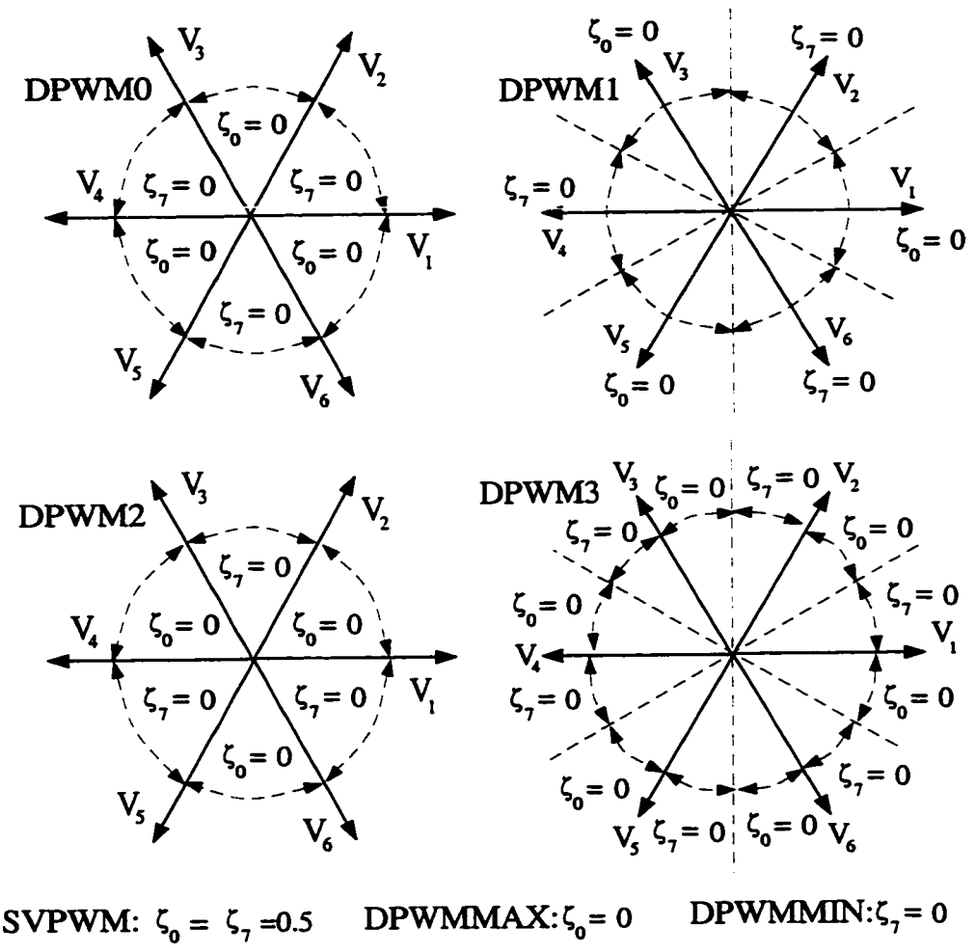

Figure 3.9: Zero state partitioning of the modern PWM methods. DPWMMIN, DPWMMAX, and SVPWM have space invariant partitioning.

method is superior to the direct digital method from a simulation as well as implementation perspective.

In voltage feedforward controlled drives ($\frac{V}{f}$ etc.), often the base modulation signals ($\sin\theta$ etc.) are stored in a table and the data is read on-line and scaled with the modulation index to generate the modulation signals. Since in such an implementation the on-line trigonometric function computations are eliminated, the processor performance requirements can be less stringent. The table of SPWM is a simple sinusoidal function. The SVPWM table can be easily generated by employing the minimum magnitude rule. Although their tables can be generated as easily as the SVPWM method, their poorer performance renders the remaining CPWM methods obsolete. Although CPWM methods can be implemented with this approach easily, the DPWM methods do not have a base function and they can not be easily implemented with table look-up approach. Therefore, applications utilizing DPWM methods require microcontroller or DSPs with computationally superior characteristics and the magnitude rules can be employed for generating the modulation signals.

Since in current controlled drives typically vector control is employed, the sine and cosine functions of the reference voltage vector are normally available for modulation signal generation. Therefore, the modulation signals can be real-time calculated and the magnitude rules can be employed. Therefore, generating the modulation signals with the magnitude rules is the preferred approach in high performance closed loop vector controlled drives.

3.4 A High Performance GDPWM Method

A careful examination of the DPWM0 and DPWM1 modulation waveforms of Fig. 3.7 indicates there exists a 30° phase angle distance between their bus clamped 60° segments. While in DPWM1 the center of each bus clamped segment is aligned with the cosine modulation wave peak, in DPWM0 a 30° phase difference exists. The same relation is true between DPWM1 and DPWM2. The modulation signals of the three methods are similar to each other and furthermore the magnitude rules involved in generating them have the same procedure. The minimum switching loss characteristic of DPWM0 under $-30°$ power factor angle operating condition, of DPWM1 under 0°, and of DPWM2 under 30° is intuitive. In each case, the bus clamped switch conducts the largest current and minimum switching losses are obtained. In fact, this characteristic has been the reason for developing these modulators. However, under different power factor operating conditions from the specified, the performance of these modulators degrades. Following the recognition of the similarities between these modulators, an attempt towards unifying them in this thesis has lead to the development of a high performance Generalized DPWM (GDPWM) method [62].

GDPWM is a DPWM method which covers a range of modulators including the DPWM0, DPWM1, and DPWM2 methods. Figure 3.10 illustrates the zero sequence signal generation method of GDPWM. To aid the description of GDPWM, it is useful to define the modulator phase angle ψ increasing from the intersection point of the two reference modulation waves at $w_e t = \frac{\pi}{6}$ as shown in

Fig. 3.10. From ψ to $\psi + \frac{\pi}{3}$, the zero sequence signal is the shaded signal which is equal to the difference between the saturation line ($\frac{V_{dc}}{2}$) and the reference modulation signal which passes the maximum magnitude test. In the maximum magnitude test, all three reference modulation signals v_a^*, v_b^*, and v_c^* are phase shifted by $\psi - \frac{\pi}{6}$, and of the three new signals v_{ax}^*, v_{bx}^*, and v_{cx}^*, the one with the maximum magnitude determines the zero sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (sign(v_a^*))\frac{V_{dc}}{2} - v_a^*$. Adding this zero sequence signal to the three original modulation waves v_a^*, v_b^*, and v_c^*, the GDPWM waves v_a^{**}, v_b^{**}, and v_c^{**} are generated. For $\psi = 0$ DPWM0, for $\psi = \frac{\pi}{6}$ DPWM1, for $\psi = \frac{\pi}{3}$ DPWM2 correspond to only three operating points on the full ψ range of the modulator ($0 \leq \psi \leq \frac{\pi}{3}$). Due to their superior performance characteristics, these three operating points of GDPWM have found a wide range of applications.

Since the GDPWM zero sequence signal must not be too large to force a modulation wave outside the triangular carrier wave boundaries, the control range of ψ is confined to the interval $[0, \frac{\pi}{3}]$. Within this ψ range, the modulator is linear between $0.0 \leq M_i \leq \frac{\pi}{2\sqrt{3}} \approx 0.907$. Figure 3.11 illustrates the modulation and zero sequence waveforms for four different ψ values and $M_i = 0.7$. Notice that DPWM1 corresponds to $\psi = \frac{\pi}{6}$ and DPWM2 to $\psi = \frac{\pi}{3}$. Note that the DPWM1 region is quite attractive in PWM-VSC utility interface applications and AC Permanent Magnet (PM) motor applications where the load power factor is near unity, while the DPWM2 end provides desirable performance characteristics for lagging loads near 30° such as induction motor drives.

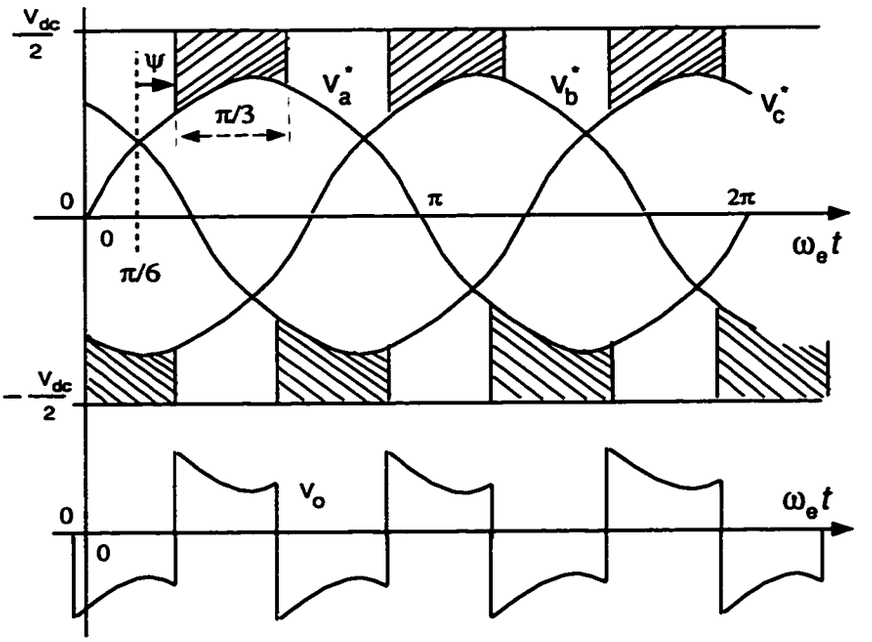

Figure 3.10: Generalized DPWM zero sequence signal generation method: ψ is the only control parameter.

The $\psi = 0$ region is suitable for operating an induction machine as a generator. In all these cases, the phase that conducts the largest current is not switched. Therefore, the inverter switching losses are significantly reduced. As will be shown later in this and the following chapters in detail, the only control parameter of GDPWM, ψ, substantially influences the waveform quality and overmodulation region characteristics also.

A careful observation of Fig. 3.10 indicates a more general approach to forming a DPWM signal is possible. Theoretically, a positive zero sequence signal of $v_{0p} = \frac{V_{dc}}{2} - v^*_{abcmax}$ always clamps the largest positive signal to the positive rail while the other signals are contained within the carrier signal boundaries ($v^*_{abcmax} = max(v^*_a, v^*_b, v^*_c)$). Also, a negative zero sequence signal

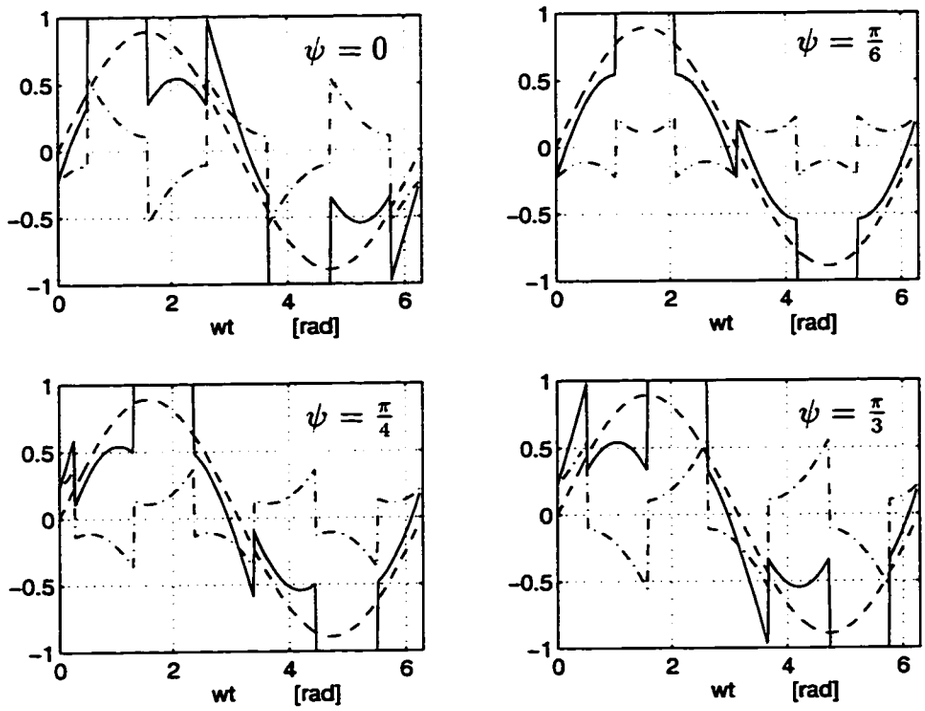

Figure 3.11: GDPWM method modulation waves("–"), their zero sequence signal ("-.") and the fundamental component ("- -") for $M_i = 0.7$ and four different modulator phase angle values.

of $v_{0n} = -\frac{V_{dc}}{2} - v^*_{abcmin}$ clamps the largest negative signal to the negative rail and the other two modulation signals are contained within the triangle wave boundaries. All the DPWM methods are formed by selecting pieces from these two zero sequence signals. Therefore, it is possible, to define more detailed zero sequence signal generation rules than the rules of GDPWM and form a modulator which covers GDPWM, DPWM3 and the other DPWM modulators also. However, such an approach would increase the modulator complexity and become practically infeasible. Furthermore, as will be later illustrated in detail, GDPWM covers the most practical modulators and yields satisfactory results for most applications.

Since it only requires a phase shift operation (rotation) and several comparisons, the GDPWM method is simple and can be easily implemented on a DSP or microprocessor. Although the ψ variable is helpful in the analysis and graphic illustration of this method, in the practical implementation a modified control variable $\psi_m = \psi - \frac{\pi}{6}$ results in reduced computations and is preferable. With this variable, DPWM0 corresponds to $\psi_m = -\frac{\pi}{6}$, DPWM1 to $\psi_m = 0$ and DPWM2 to $\psi_m = \frac{\pi}{6}$ values. Employing d-q transformations and expanding the terms in a manner to minimize the computational requirements, the rotation calculation can be accomplished in the following equations.

$$v^*_{ax} = v^*_a \cos(\psi_m) - \frac{(v^*_c - v^*_b)}{\sqrt{3}} \sin(\psi_m) \tag{3.17}$$

$$v_{bx}^* = v_b^* \cos(\psi_m) + (\frac{1}{2}\frac{(v_c^* - v_b^*)}{\sqrt{3}} - \frac{\sqrt{3}v_a^*}{2}) \sin(\psi_m) \tag{3.18}$$

$$v_{cx}^* = -v_{ax}^* - v_{bx}^* \tag{3.19}$$

Applying the maximum magnitude test to the above signals, the switch to be clamped to the positive or negative rail is defined and the zero sequence calculation is followed by the zero sequence signal injection. With the modulation signal computation stage completed, the duty cycles of the inverter switches are computed from (3.4) and (3.5) and the last stage involves loading the PWM counters with these duty cycle values.

Figure 3.12 shows the space vector coordinate illustration of the GDPWM method. As the figure indicates, in the direct digital implementation the inverter zero states, t_0 (000) and t_7 (111) are interchangeably set to zero for 60° segments. The diagram indicates the direct digital implementation is straightforward. However, it is computationally more involved than the triangle intersection implementation [38, 114, 146]. Therefore, the direct digital implementation is less practical. However, the space vector co-ordinate illustration of the method aids visualization of this modulator characteristics such as the voltage linearity and waveform quality which will be investigated in the following sections in detail.

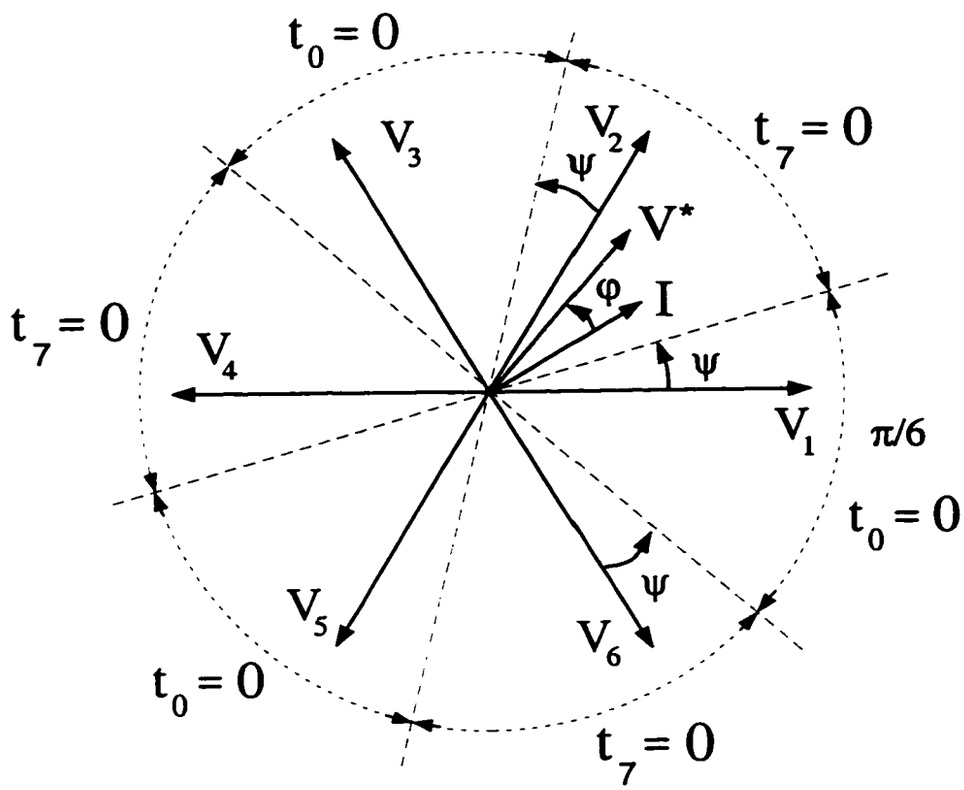

Figure 3.12: The GDPWM method space vector illustration aids the direct digital implementation.

3.5 Waveform Quality

The linear modulation range output voltage of a carrier based PWM-VSI drive contains harmonics at the carrier frequency, at its integer multiples, and at the side bands of all these frequencies which will all be termed as "the switching frequency harmonics." With sufficiently high carrier frequency, f_s, to fundamental frequency, f_e, ratios ($\frac{f_s}{f_e} > 20$) the low frequency reference volt-seconds are programmed accurately and the subcarrier frequency harmonic content is negligible [30]. Since modern power electronics switching devices such as IGBTs and MOSFETs typically meet this requirement, the voltage and current waveform quality of the PWM-VSI drives is determined by the switching frequency harmonics. In high power drive applications where the switching frequency is low, synchronization of the carrier signal with the fundamental component yields very low subcarrier frequency harmonic content. Therefore, the subcarrier frequency harmonic content can be neglected in most applications. Since they determine the switching frequency harmonic copper losses and the torque ripple of a motor load and the line current Total Harmonic Distortion (THD) of a PWM-VSC, the switching frequency harmonic characteristics of a PWM-VSI drive are important in determining its performance. While the THD and the copper losses are measured over a fundamental cycle and therefore require a per fundamental cycle (macroscopic) RMS ripple current value calculation, the peak and local harmonic stresses are properly investigated on a per carrier cycle (microscopic) base. Therefore, first a microscopic and then a macroscopic

investigation is required.

Perhaps, the most intuitive and straightforward approach for analytical investigation of the switching frequency harmonic characteristics of a PWM-VSI is the vector space approach [4, 31, 103, 105]. As illustrated in the vector diagram of Fig. 3.13, in the first sector of the inverter hexagon, selecting the adjacent and zero states to balance the reference volt-seconds results in generating the harmonic voltage vectors V_{1h}, V_{2h}, and V_{0h} within each carrier cycle. As the figure indicates, the magnitude and phase of each harmonic voltage vector is modulation index and space dependent. Along with the harmonic voltage vectors, the duty cycle of the active inverter states and partitioning of the two zero states determine the harmonic current trajectories. Instead of the harmonic current trajectories, the conceptual harmonic flux (time integral of the harmonic voltage vector) λ_h trajectories can be investigated and with the assumption the load switching frequency model is an inductance, the harmonic current and harmonic flux trajectories are only different in scale ($\lambda = Li$). Since the inductance component of the load transient impedance model (an R-L series circuit) dominates the resistance component, this assumption is valid in most applications with $\frac{f_s}{f_c} > 20$). The harmonic flux in the N'th carrier cycle is calculated in the following.

$$\lambda_h(M_i, \theta, V_0) = \int_{NT_s}^{(N+1)T_s} (V_k - V^*)dt \tag{3.20}$$

In the above formula, V_k is the inverter output voltage vector of the k'th

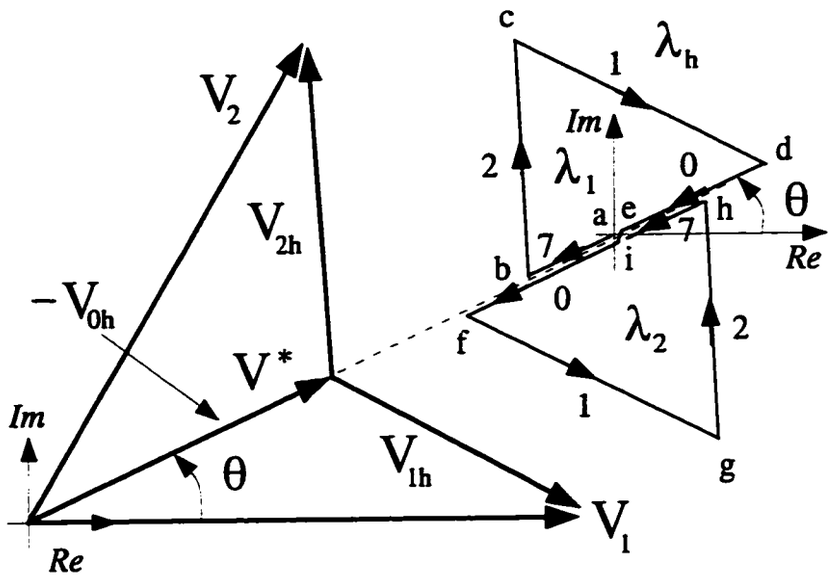

Figure 3.13: Harmonic flux trajectories in the first segment of the hexagon.

state and within the carrier cycle it changes according to the selected switching sequence. For example, in the first segment of the inverter hexagon ($R = 1$), all the modern PWM methods generate the sequence 7-2-1-0-0-1-2-7 and in the DPWM methods the "7" or the "0" states are absent. Note the above harmonic flux calculation requires no load information, and completely characterizes the switching frequency behavior of a modulator. Since for high $\frac{f_s}{f_c}$ values the V^* term can be assumed constant within a carrier cycle, and the V_k terms are constant complex numbers, the above integral can be closed form calculated and the flux trajectories are linear over each state. Assuming its value at the beginning of the carrier cycle is zero, the harmonic flux vector becomes zero at the half cycle point and at the end of the carrier cycle again. Therefore, (3.20) always assumes zero initial value. Since in the triangular intersection and direct digital PWM methods only symmetric switching sequences are generated, the

integral need only be calculated in the first half of the carrier cycle and the second half of the trajectory is exactly symmetrical to the first. As illustrated in Fig. 3.13 for the first segment of the inverter hexagon, the harmonic flux trajectories form two triangles which may slide along the reference vector line in opposite directions with respect to the origin. It is apparent from the diagram ZSP determines the slip of the triangles and affects the harmonic characteristics. Therefore, the harmonic flux trajectories of each PWM method are unique.

Calculating the harmonic flux vector for a half carrier cycle for the first region of the vector space for an arbitrary set of M_i, θ, and ZSP (or v_0) and normalizing to λ_b for further simplification, the following normalized analytical harmonic flux formula $\lambda_1(d, M_i, \theta)$ yields.

$$\lambda_b = \frac{2V_{dc}}{\pi}\frac{T_s}{2} \tag{3.21}$$

$$\lambda_1 = \frac{\lambda_{h1}}{\lambda_b} \tag{3.22}$$

$$\lambda_1 = \begin{cases} -M_i e^{j\theta} d & 0 \le d \le d_7 \\ -\frac{\pi}{3} e^{j\frac{\pi}{3}} d_7 + (\frac{\pi}{3} e^{j\frac{\pi}{3}} - M_i e^{j\theta}) d & d_7 \le d \le d_7 + d_2 \\ -M_i e^{j\theta}(d_7 + d_2) + \frac{\pi}{3} e^{j\frac{\pi}{3}} d_2 + & \\ (\frac{\pi}{3} - M_i e^{j\theta})(d - d_7 - d_2) & d_7 + d_2 \le d \le 1 - d_0 \\ \frac{\pi}{3}(d_1 + d_2 e^{j\frac{\pi}{3}}) - M_i e^{j\theta} d & 1 - d_0 \le d \le 1 \end{cases} \tag{3.23}$$

In the above equation, the "d" variable is inverter state duty cycle over a half carrier cycle ($\frac{t}{\frac{T_s}{2}}$). As the equation indicates, it starts at 0 at the beginning of the half carrier cycle and it becomes 1 at the end of the half carrier cycle. In the second half of the carrier cycle, the harmonic flux can be calculated from the symmetry condition: $\lambda_2(d) = -\lambda_1(1-d)$. However, in this half the inverter state duty cycles must be evaluated in the reverse sequence to the first half of the carrier cycle. The above equation can be easily programmed for any PWM method and the space and modulation index dependency of the harmonic flux/current can be graphically illustrated. Since the inverter hexagon has a six-fold symmetry, only the first segment need be investigated. The duty cycle of the active states d_1 and d_2 in this segment are calculated from (3.11) and (3.12). In the direct digital method the zero states are directly defined, while in the triangle intersection method the modulation waves are utilized to calculate the phase duty cycles from (3.4) and (3.5). For example, for R=1 Fig. 3.6 suggests $d_0 = d_{a-} = 1 - d_{a+}$ and $d_7 = d_{c+}$.

Figure 3.14 illustrates the normalized harmonic flux trajectories which are calculated from (3.23) for various modulators and operating conditions. To allow better visualization and clearer harmonic flux trajectory comparison, only the trajectories in the first half of a carrier cycle are illustrated in the figure and the second half is always the exact symmetric of the first. Figure 3.14 (a) illustrates the space dependency of the SPWM method harmonic flux. As the figure indicates, the "0" and "7" state duty cycles are not always equally split and the varying triangle shapes indicate the space dependency of the harmonic

flux is strong. Figure 3.14 (b) compares SVPWM and THIPWM1/4 for two different angular positions. At $w_e t = 30°$ the triangles are identical, however at $w_e t = 15°$ the triangles have slipped. While SVPWM splits the zero states equally, the THIPWM1/4 method does slide the triangle in the direction that the center of gravity becomes closer to the origin. Since the distance to the origin is equal to the magnitude of the harmonic flux, the trajectories which are closer to the origin result in smaller harmonic flux and the per carrier cycle RMS flux value decreases[106]. Figure 3.14 (c) and (d) compare SVPWM and DPWM1 and illustrate that the DPWM method always skips one of the two zero states. Therefore the DPWM1 flux triangle is quite distant from the origin. However, increasing the carrier frequency shrinks the triangle size and brings the weight center of the triangle closer to the origin and reduces the harmonic flux. When comparing the CPWM and DPWM modulator performances, to account for the reduction in the number of per fundamental cycle switchings of the DPWM methods, a carrier frequency coefficient k_f is introduced in the following.

$$k_f = \frac{f_{sCPWM}}{f_{sDPWM}} \tag{3.24}$$

Employing (3.23), the per carrier cycle RMS value of the harmonic flux λ_{1RMS} can be closed form calculated. Since the first and the second halves of the trajectory have the same RMS value due to symmetry, calculating only the first is sufficient. Involved calculations yield the following M_i and duty cycle

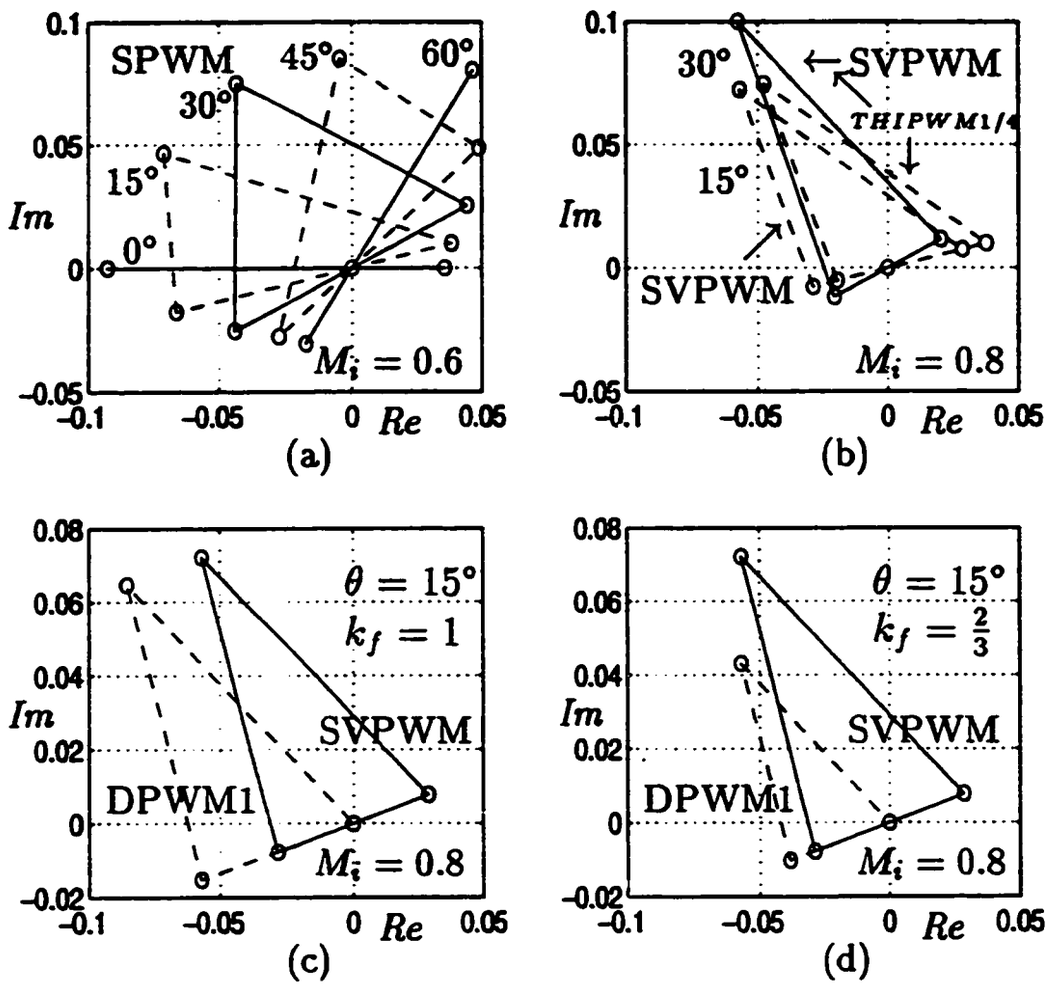

Figure 3.14: The switching frequency harmonic flux trajectories of various PWM methods. (a): SPWM. (b): SVPWM and THIPWM1/4 compared for $w_e t = 15°$ and $w_e t = 30°$ values. (c): SVPWM and DPWM1 compared ($k_f = 1$), (d): SVPWM and DPWM1 compared for $k_f = \frac{2}{3}$.

dependent formula.

$$\lambda_{1RMS}^2 = \int_0^1 \lambda_1^2 dd = \lambda_{11}^2 + \lambda_{12}^2 + \lambda_{13}^2 \tag{3.25}$$

$$\lambda_{11}^2 = \frac{\pi^2}{18} M_i^2 (\frac{1}{3} + d_0^2 + d_1^2 - d_0 - d_1 + 2d_0 d_1) \tag{3.26}$$

$$\lambda_{12}^2 = \frac{\pi^4}{72} [\frac{1}{3}(2d_1^3 - 4d_2^3 - 4d_1^4 + 2d_2^4 + 7d_1 d_2^3 - 2d_2 d_1^3) + d_1^2 d_2^2] \tag{3.27}$$

$$\lambda_{13}^2 = \frac{\pi^4}{72} [-d_1 d_2^2 + d_0 (d_1 d_2^2 - 2d_1^3 + 2d_2^3 - d_1^2 d_2)] \tag{3.28}$$

Employing the above formula, the θ and M_i dependency of λ_{1RMS}^2 of various PWM methods can be easily computed and graphically illustrated. Figure 3.15 and Fig. 3.16 compare the RMS harmonic flux characteristics of the modern PWM methods for two modulation index values. The figures indicate the CPWM methods have lower harmonic distortion than the DPWM methods and the difference is more pronounced at low M_i. The THIPWM1/4 method, which is the minimum harmonic distortion method (the optimality condition can be verified by searching the minimum of (3.25) with respect to d_0 [105]), has only slightly less distortion than SVPWM and only near the 15° and 45° range. Since the DPWM methods have a discrete ZSP (0 or 1), within certain segments the ZSP of various DPWM methods is the same (see Fig.3.9). Therefore, calculating

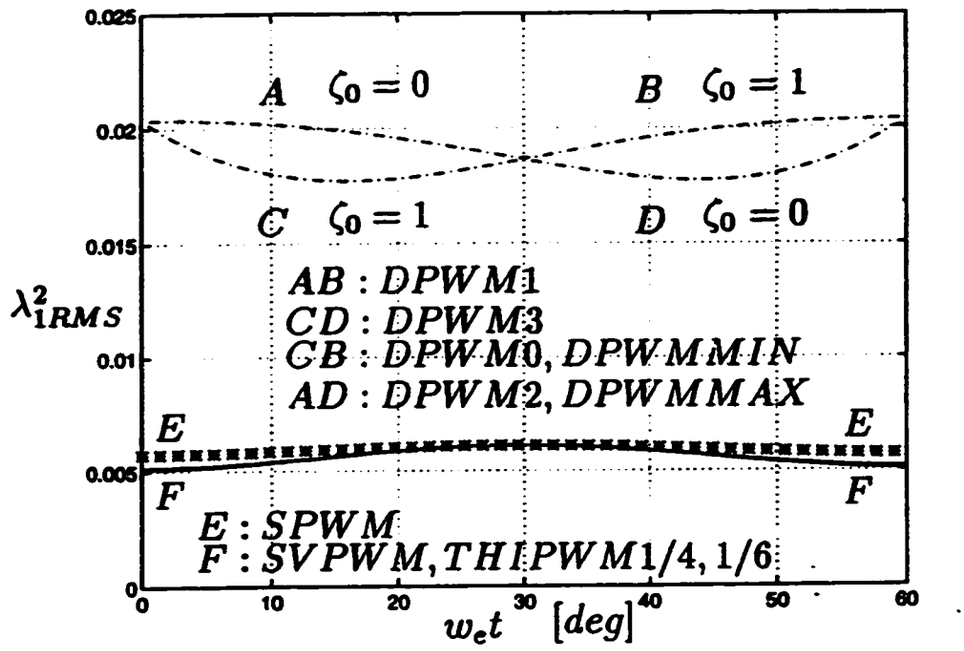

Figure 3.15: The space dependency of the per carrier cycle normalized RMS harmonic flux of the modern PWM methods for $M_i = 0.4$.

the RMS harmonic flux of DPWM methods is a relatively simple task. According to Fig. 3.15, $\zeta_0 = 0$ for segment A and $\zeta_0 = 1$ for segment C are the only two functions required to determine the RMS flux curves of all DPWM methods. The overall comparison indicates that SVPWM provides superior performance in the low modulation range. However, as M_i increases the performance of DPWM methods significantly improves and becomes comparable to SVPWM.

As Fig. 3.15 and Fig. 3.16 clearly illustrate the strong space dependency of the per carrier cycle RMS harmonic distortion characteristics of all the modern

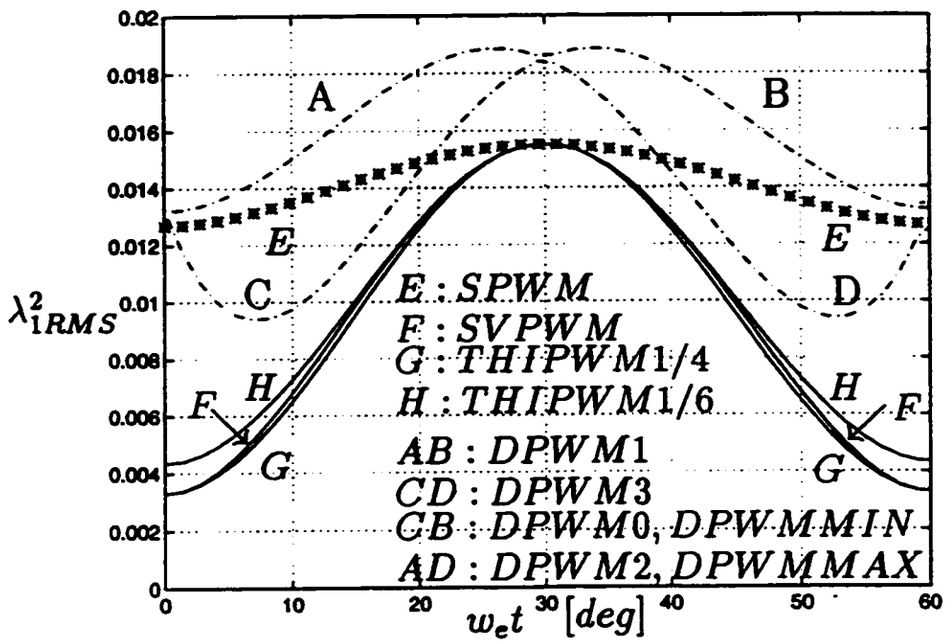

Figure 3.16: The space dependency of the per carrier cycle normalized RMS harmonic flux of the modern PWM methods for $M_i = 0.78$.

PWM methods, it becomes apparent that performance can be gained by modulating the carrier frequency. If the carrier frequency is methodically increased at the high RMS harmonic flux intervals and reduced at the low harmonic RMS flux intervals, then the overall harmonic distortion characteristics can be reduced [72]. Provided the inverter average switching frequency is maintained constant, the switching loss characteristics are not affected by the frequency modulation and performance gain without efficiency reduction becomes possible. Since the frequency modulation techniques are most beneficial to modulators with strongly space dependent RMS harmonic flux characteristics, CPWM methods are more suitable candidates than DPWM methods for this approach. In addition to reducing the RMS harmonic distortion and the peak ripple current, the frequency modulation techniques also flatten the inverter output voltage/current harmonic spectrum. Therefore, they are suitable for high power quality applications that require a flat harmonic spectrum with no dominant harmonic content.

Since it determines the waveform quality and harmonic losses, the per fundamental cycle RMS value λ_{1FRMS} of the harmonic flux is the most important performance characteristic of a modulator. Since the λ^2_{1RMS} characteristics of the modern PWM methods have sixfold space symmetry, the per fundamental cycle (per 60° in space) RMS harmonic flux value can be calculated in the following.

$$\lambda_{1FRMS}^2 = \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \lambda_{1RMS}^2 d\theta \tag{3.29}$$

For each modulator, the above integral yields a polynomial function of M_i with unique coefficients and it can be written in the following M_i dependent Harmonic Distortion Function (HDF) formula.

$$\lambda_{1FRMS}^2 = \frac{\pi^2}{288} HDF = \frac{\pi^2}{288}(a_m {M_i}^2 + b_m {M_i}^3 + c_m {M_i}^4) \tag{3.30}$$

$$HDF = a_m {M_i}^2 + b_m {M_i}^3 + c_m {M_i}^4 \tag{3.31}$$

Calculating a_m, b_m, and c_m of each modulator involves significant algebraic manipulations. The resulting HDF functions of the discussed modulators are summarized in the following.

$$HDF_{SPWM} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{9}{8})(\frac{4}{\pi}M_i)^4 \tag{3.32}$$

$$HDF_{THIPWM6} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{4}{\pi}M_i)^4 \tag{3.33}$$

$$HDF_{THIPWM4} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{63}{64})(\frac{4}{\pi}M_i)^4 \tag{3.34}$$

$$HDF_{SVPWM} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{27}{16} - \frac{81\sqrt{3}}{64\pi})(\frac{4}{\pi}M_i)^4 \qquad (3.35)$$

Notice in all the CPWM methods the first two terms are the same and the third term involves the dominant coefficient of the ZSP of each method. As was shown in Fig. 3.15 and Fig. 3.16, the harmonic flux of DPWM methods consists of a combination of the A, B, C, and D segments. A and B yield equivalent distortion, likewise do C and D. Therefore, calculating the HDF of A and B segments (HDF_{DMAX}), and C and D segments (HDF_{DMIN}) is sufficient in determining the performance of all the DPWM methods discussed. The results are as follows.

$$HDF_{DMAX} = 6(\frac{4}{\pi}M_i)^2 - (\frac{8\sqrt{3}+45}{2\pi})(\frac{4}{\pi}M_i)^3 + (\frac{27}{8} + \frac{27\sqrt{3}}{32\pi})(\frac{4}{\pi}M_i)^4 \qquad (3.36)$$

$$HDF_{DMIN} = 6(\frac{4}{\pi}M_i)^2 + (\frac{45-62\sqrt{3}}{2\pi})(\frac{4}{\pi}M_i)^3 + (\frac{27}{8} + \frac{27\sqrt{3}}{16\pi})(\frac{4}{\pi}M_i)^4 \qquad (3.37)$$

For the same carrier frequency the DPWM methods have less switchings per fundamental cycle than the CPWM methods. Therefore, to account for the carrier frequency effect, the PWM frequency coefficient k_f is included in the HDF formulas of the DPWM methods.

$$HDF_{DPWM1} = {k_f}^2 \times HDF_{DMAX} \qquad (3.38)$$

$$HDF_{DPWM3} = {k_f}^2 \times HDF_{DMIN} \tag{3.39}$$

$$HDF_{DPWM0} = {k_f}^2 \times 0.5 \times (HDF_{DMIN} + HDF_{DMAX}) \tag{3.40}$$

$$HDF_{DPWM2} = HDF_{DPWMMIN} = HDF_{DPWMMAX} = HDF_{DPWM0} \tag{3.41}$$

The relation between HDF and the per phase harmonic current RMS value I_h for a load with a transient inductance L_σ, which can be utilized in calculating the harmonic copper losses, is as follows.

$$I_{xh}^2 = \left(\frac{V_{dc}}{24 L_\sigma f_s}\right)^2 \times HDF(M_i) \qquad for \qquad x \in \{a, b, c\} \tag{3.42}$$

Figure 3.17 shows the HDF curves of all the discussed PWM methods. In the very low modulation index range all CPWM methods have practically equal HDF which is superior to all DPWM methods. As the modulation index increases the SPWM performance rapidly degrades while the remaining CPWM methods maintain low HDF over a wide modulation range. The figure indicates the THIPWM1/4 performance is only slightly better than SVPWM, and the difference is less noticeable from the local differences shown in Fig. 3.14 and Fig. 3.16. In the high modulation range the DPWM methods are superior to SVPWM (Fig. 3.17) and the intersection point of the DPWM method of

choice and SVPWM defines the optimal transition point. Although in the high modulation range the DPWM3 method has less HDF than the other DPWM methods, the improvement is marginal and the modulator selection criteria can be based on the switching loss and voltage linearity characteristics which are stronger functions of the DPWM methods. The HDF function of the GDPWM method is ψ dependent, and varies between curves 5 and 6 of Fig. 3.17. Its HDF can be approximated with the average value of (3.38) and (3.40).

$$HDF_{GDPWM} \approx {k_f}^2 \times 0.25 \times (HDF_{DMIN} + 3 \times HDF_{DMAX}) \qquad (3.43)$$

Since the HDF of each PWM method is unique, harmonic spectrum of each method is also unique. Since the DPWM methods have two less switchings per carrier cycle than CPWM methods, for the same carrier frequency, the switching frequency side band harmonics of the DPWM methods are wider and larger in magnitude. Calculating the individual harmonics and the peak ripple current is involved and will be omitted herein. Having illustrated the superior high modulation range waveform quality characteristics of the DPWM methods over SVPWM, in the next section the switching losses of DPWM methods will be characterized to aid an intelligent modulator choice. Following a brief section on the inverter input current harmonics, the switching losses of the DPWM methods will be analytically modeled and their performance evaluated.

Notice all the PWM switching frequency harmonic calculations performed

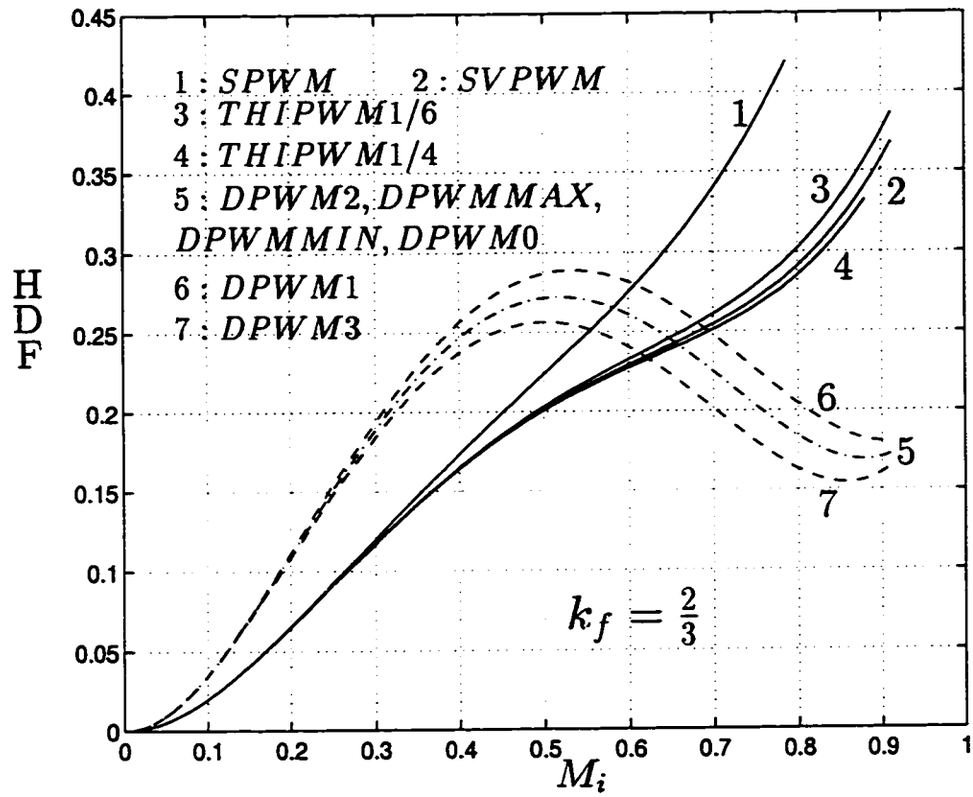

Figure 3.17: $HDF = f(M_i)$ curves in the linear modulation range under constant inverter average switching frequency condition.

until this stage are valid within the voltage linearity range of the corresponding modulators. Therefore, they are valid for SPWM until a modulation index of 0.785, for THIPWM1/4 until 0.881, and until 0.907 for the remainder of the modulators. Outside the voltage linearity range the low frequency harmonic content significantly increases and the performance substantially degrades. These characteristics will be investigated in the next chapter.

3.6 Inverter Input Current Harmonics

The DC link input current of a PWM inverter I_{in} consists of the DC average value I_{dc} which corresponds to the average power transfer to the load, and switching frequency component I_{inh}, which is due to PWM switching. Since during the zero states the DC link is decoupled from the AC load, the RMS value of the ripple current I_{inhRMS}, which is required in DC link capacitor design and loss calculations, is independent of the zero sequence signal and therefore of the modulator type. Since the duty cycles of the inverter active states are independent of the carrier frequency, I_{inhRMS} is also independent of the carrier frequency. Similar to the inverter output harmonic current RMS value calculation, I_{inhRMS} can also be easily calculated by establishing a per carrier cycle RMS value formula and evaluating it over 60° in vector space [103]. The calculation yields the following M_i, load power factor ($\cos\varphi$) and load current fundamental component RMS value (I_{1RMS}) dependent DC link current ripple factor K_{Iin} formula.

$$K_{Iin} = \frac{I^2_{inhRMS}}{I^2_{1RMS}} = \frac{2\sqrt{3}}{\pi^2} M_i + (\frac{8\sqrt{3}}{\pi^2} - \frac{18}{\pi^2} M_i) M_i \cos^2 \varphi \qquad (3.44)$$

Figure 3.18 illustrates the M_i and $\cos\varphi$ dependency of the K_{Iin} factor. The maximum ripple occurs at $\cos\varphi = 1$ and at $M_i = \frac{5\sqrt{3}}{18} \approx 0.48$ (a reasonable design point for capacitor sizing) and the ripple is independent of $\cos\varphi$ at $M_i = \frac{8\sqrt{3}}{18} \approx 0.77$. The closed form approach is intuitive and can aid capacitor design, while the previously reported computer simulation data evaluation based graphic illustration is laborious and not user-friendly [210].

Notice although the RMS value of the ripple is independent of the modulation method, the harmonic spectrum is strongly influenced by the modulation method choice. A recent publication investigates the harmonic spectrum characteristics of various PWM methods for AC/DC/AC PWM-VSI drives [170].

The DC average value of the DC link input current, I_{dc}, can also be closed form calculated as a function of the modulation index, RMS load current, and the load power factor. Assuming steady state operating conditions and sinusoidal load currents with zero harmonics, the average value of the input current can be calculated from the inverter average input power equation in the following.

$$I_{dc} = \frac{3\sqrt{2}}{\pi} M_i I_{1RMS} \cos\varphi \qquad (3.45)$$

Although the above formula may not be useful in design, it helps understand

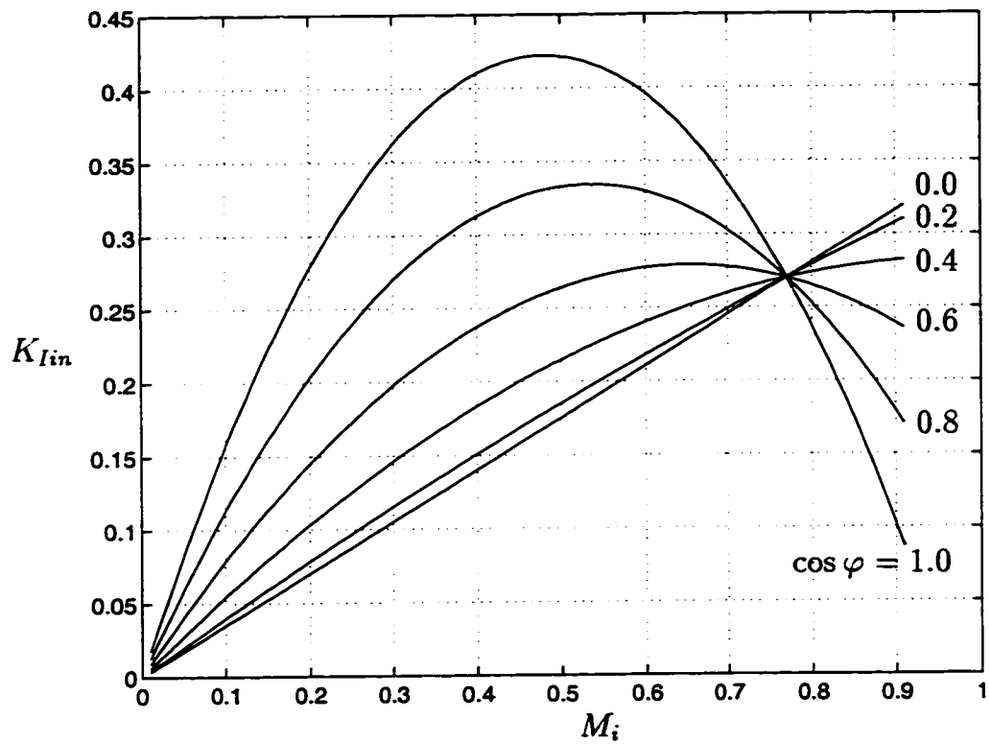

Figure 3.18: Normalized inverter input harmonic current RMS value characteristics $K_{Iin} = f(M_i)$ of PWM-VSI for $\cos\varphi$ as parameter.

the inverter steady state behavior. It indicates DC bus loading linearly increases with the modulation index and the load current active component ($I_{1RMS}\cos\varphi$).

3.7 Switching Losses

The switching losses of a PWM-VSI drive are load current dependent and increase with the current magnitude. Switching device manufacturer's data books (for example, IGBT data books [81]) indicate this relation is approximately linear, i.e. the switching losses are proportional to the current magnitude.

With CPWM methods, all the three phase currents are commutated within each carrier cycle of a full fundamental cycle. Therefore, for all CPWM methods the switching losses are the same and independent of the load current phase angle (power factor angle). With DPWM methods, however, the switching losses are significantly influenced by the modulation method and load power factor angle. Because DPWM methods cease to switch each switch for a total of 120° per fundamental cycle and the location of the unmodulated segments with respect to the modulation wave fundamental component phase is modulator type dependent. Therefore, the load power factor and the modulation method together determine the time interval that the load current is not commutated. Since the switching losses are strongly dependent on and linearly increase with the magnitude of the commutating phase current, selecting a DPWM method with reduced switching losses can significantly contribute to the performance of

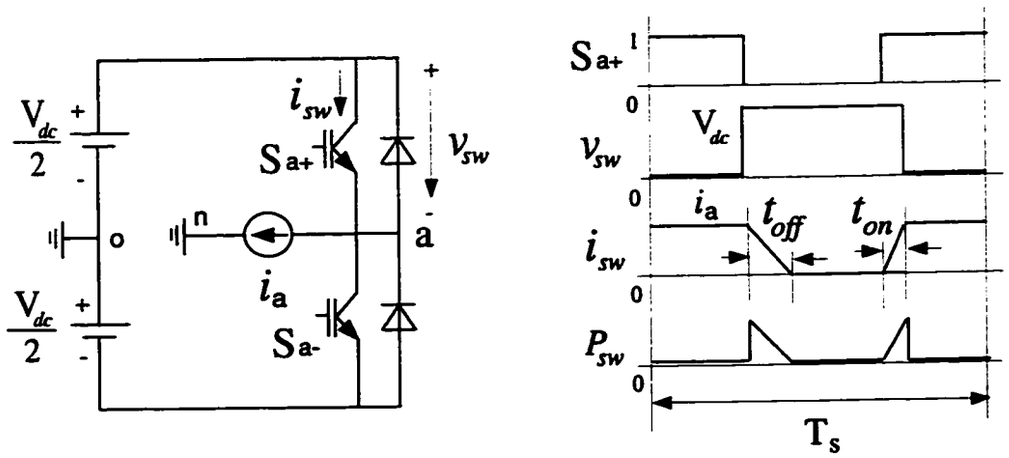

Figure 3.19: The inverter per phase model and per carrier cycle switching loss diagram under linear commutation.

a drive. Therefore, it is necessary to characterize and compare the switching losses of DPWM methods.

Assuming the inverter switching devices have linear current turn-on and turn-off characteristics with respect to time and accounting only for the fundamental component of the load current, the switching losses of a PWM-VSI drive can be analytically modeled [107]. Shown in Fig. 3.19, the single phase inverter model and the switching voltage/current diagram aid calculating the switching losses. Deriving the local (per carrier cycle) switching loss formula and calculating its average value over the fundamental cycle, the per fundamental cycle inverter per device switching loss P_{swave} can be calculated as follows.

$$P_{swave} = \frac{1}{2\pi} \frac{V_{dc}(t_{on} + t_{off})}{2T_s} \int_0^{2\pi} f_i(\theta) d\theta \tag{3.46}$$

In the above formula, t_{on} and t_{off} variables represent the turn-on and turn-off times of the switching devices, and $f_i(\theta)$ is the switching current function. The switching current function $f_i(\theta)$ equals zero in the intervals where modulation ceases and the absolute value of the corresponding phase current value elsewhere. For example, for phase "a," this function is as follows.

$$f_{ia}(\theta) = \begin{cases} 0 & |v_a^{**}| \geq \frac{V_{dc}}{2} \\ |i_a| & |v_a^{**}| < \frac{V_{dc}}{2} \end{cases} \tag{3.47}$$

The calculation assumes steady state operating conditions where the currents are practically sinusoidal functions. Therefore, $|i_a|$ is a function of the load power factor angle and the current magnitude. As a result, the phase current power factor angle φ enters the formula as the integral boundary term and φ dependent switching loss formula yields. Normalizing P_{swave} to P_o, the switching loss value under CPWM condition (which is φ independent), the Switching Loss Function (SLF) of a modulator can be found.

$$P_o = \frac{V_{dc} I_{max}}{\pi T_s} \times (t_{on} + t_{off}) \tag{3.48}$$

$$SLF = \frac{P_{swave}}{P_o} \tag{3.49}$$

In (3.48) the variable I_{max} represents the load current fundamental component maximum value. By the definition of (3.46), the SLF of CPWM methods is

unity. The SLF of DPWM methods can be easily calculated from their current switching function. Figure 3.20 shows the ψ and φ dependent switching current and switching loss function waveforms of GDPWM. Applying the procedure to GDPWM yields the following SLF.

$$SLF_{GDPWM} = \begin{cases} \frac{\sqrt{3}}{2}\cos\left(\frac{4\pi}{3} + \psi - \varphi\right) & -\frac{\pi}{2} \le \varphi \le -\frac{\pi}{2} + \psi \\ 1 - \frac{1}{2}\sin\left(\frac{\pi}{3} + \psi - \varphi\right) & -\frac{\pi}{2} + \psi \le \varphi \le \frac{\pi}{6} + \psi \\ \frac{\sqrt{3}}{2}\cos\left(\frac{\pi}{3} + \psi - \varphi\right) & \frac{\pi}{6} + \psi \le \varphi \le \frac{\pi}{2} \end{cases} \tag{3.50}$$

The SLF function of the DPWM0, DPWM1, and DPWM2 can be easily evaluated from (3.50) by substituting $\psi = 0$, $\psi = \frac{\pi}{6}$, and $\psi = \frac{\pi}{3}$. The SLF of the remaining DPWM methods are as follows.

$$SLF_{DPWMMIN} = \begin{cases} \frac{1}{2} - \frac{1}{4}\sin\varphi & -\frac{\pi}{2} \le \varphi \le -\frac{\pi}{6} \\ 1 - \frac{\sqrt{3}}{4}\cos\varphi & -\frac{\pi}{6} \le \varphi \le \frac{\pi}{6} \\ \frac{1}{2} + \frac{1}{4}\sin\varphi & \frac{\pi}{6} \le \varphi \le \frac{\pi}{2} \end{cases} \tag{3.51}$$

$$SLF_{DPWMMAX} = SLF_{DPWMMIN} \tag{3.52}$$

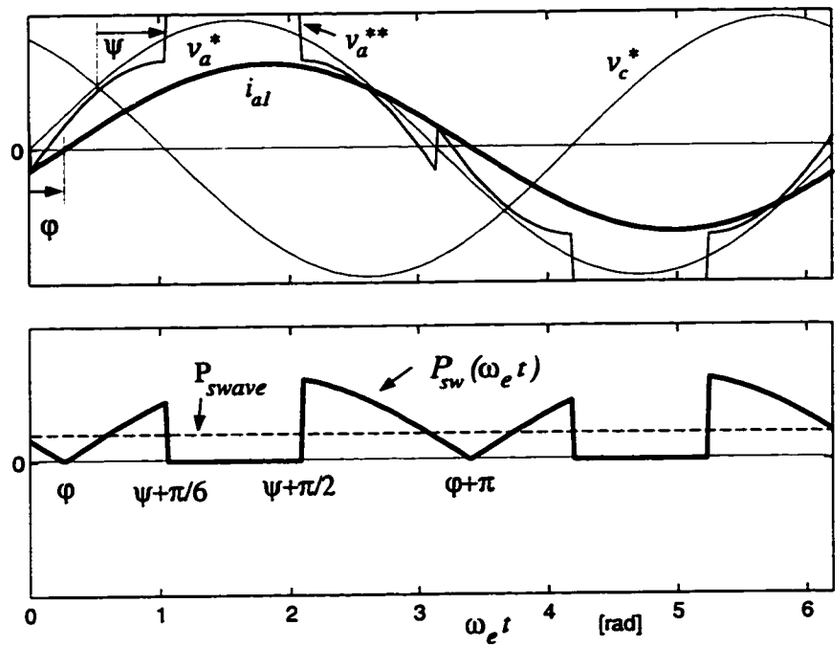

Figure 3.20: The average switching losses of GDPWM, $P_{swave} = f(\psi, \varphi)$.

$$SLF_{DPWM3} = \begin{cases} 1 + 0.5(\sqrt{3} - 1)\sin\varphi & -\frac{\pi}{2} \leq \varphi \leq -\frac{\pi}{3} \\ 0.5(\cos\varphi - \sin\varphi) & -\frac{\pi}{3} \leq \varphi \leq -\frac{\pi}{6} \\ 1 - 0.5(\sqrt{3} - 1)\cos\varphi & -\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{6} \\ 0.5(\cos\varphi + \sin\varphi) & \frac{\pi}{6} \leq \varphi \leq \frac{\pi}{3} \\ 1 - 0.5(\sqrt{3} - 1)\sin\varphi & \frac{\pi}{3} \leq \varphi \leq \frac{\pi}{2} \end{cases} \tag{3.53}$$

Shown in Fig. 3.21, SLF surface of GDPWM indicates that its switching losses are a strong function of the load power factor angle. As the three dimensional graphic indicates, the switching losses can be minimized by controlling the modulator phase angle as a function of the load power factor angle. It is apparent from the figure the SLF surface touches the $SLF = 0.5$ plane along a straight line. In the $-\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{6}$ region, selecting $\psi = \varphi + \frac{\pi}{6}$ results in

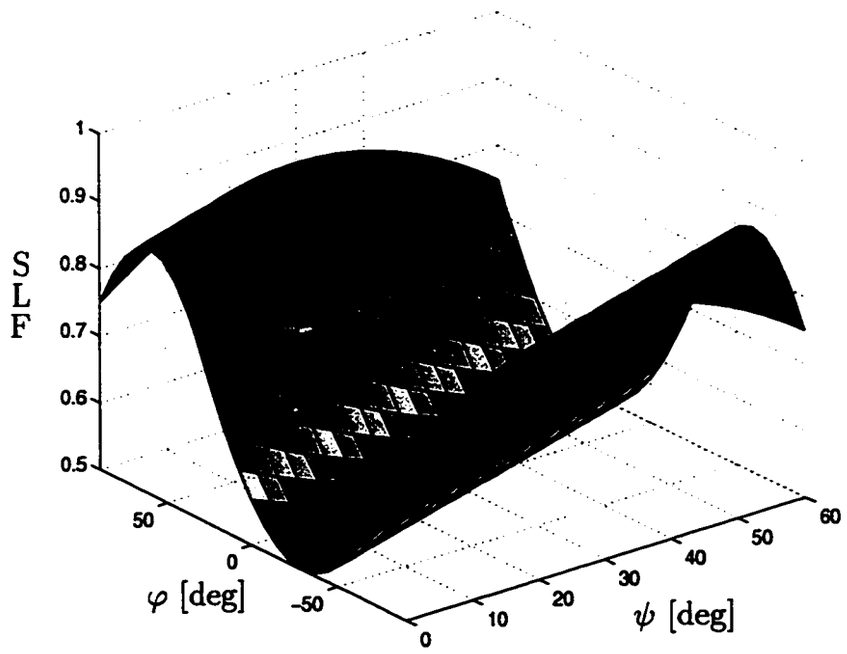

Figure 3.21: $SLF = f(\psi, \varphi)$ function of the GDPWM method.

minimum switching loss value ($SLF_{min} = 0.5$) which is equal to 50 % of the CPWM methods ($SLF_{CPWM} = 1.0$). Outside this range, the modulator phase angle must be held at the boundary value of $\psi = \frac{\pi}{3}$ (DPWM2) for positive φ and at the value of $\psi = 0$ (DPWM0) for negative φ so that the GDPWM voltage linearity is retained. As a result, in these operating regions the switching losses become more than 50 % and less than 75 % of the switching losses of CPWM methods and the exact amount can be found from the 3-D SLF surface of Fig. 3.21.

Figure 3.22 shows the SLF characteristics of the modern DPWM methods along with the optimum SLF solution of the GDPWM method. Note that outside the $-\frac{5\pi}{12} \leq \varphi \leq \frac{5\pi}{12}$ range DPWM3 yields minimum switching losses. As

Fig. 3.22 indicates, the switching losses of DPWM methods strongly depend on φ and can be reduced to 50% of the CPWM methods. The graphic suggests combining GDPWM and DPWM3 would result in optimum SLF. A control algorithm should select GDPWM within $-\frac{5\pi}{12} \leq \varphi \leq \frac{5\pi}{12}$ and optimize it with the above described ψ choice. Outside this φ range DPWM3 should be selected. With such a choice, the optimal SLF curve of Fig. 3.23 results. Note with this algorithm the switching losses become less than 65% of the CPWM methods.

The switching loss analysis with the aid of SLF has shown the modulator choice strongly influences the drive efficiency and thermal design. Since the switching losses are load power factor angle dependent, the modulator choice should involve the power factor value. Drives mostly operating near unity power factor could utilize GDPWM and optimize its phase angle for minimum losses. For example, most induction motor drives and permanent magnet motor drives operate within $-30° \leq \varphi \leq 30°$ range and therefore on-line optimized GDPWM is sufficient in such applications. In reactive power compensation applications (PWM-VSI VAr compensators) the DPWM3 method provides minimum switching losses in addition to low harmonic distortion. Applications with widely varying power factor conditions could utilize the combined algorithm and benefit from both DPWM3 and the optimal GDPWM method. Induction motor drives with frequent no-load operating conditions can utilize this algorithm to maximize the drive performance. Perhaps, the most suitable applications of the combined algorithm are the future generation intelligent drives such as universal drives. With the controller tuning the modulator on-line for the application, or

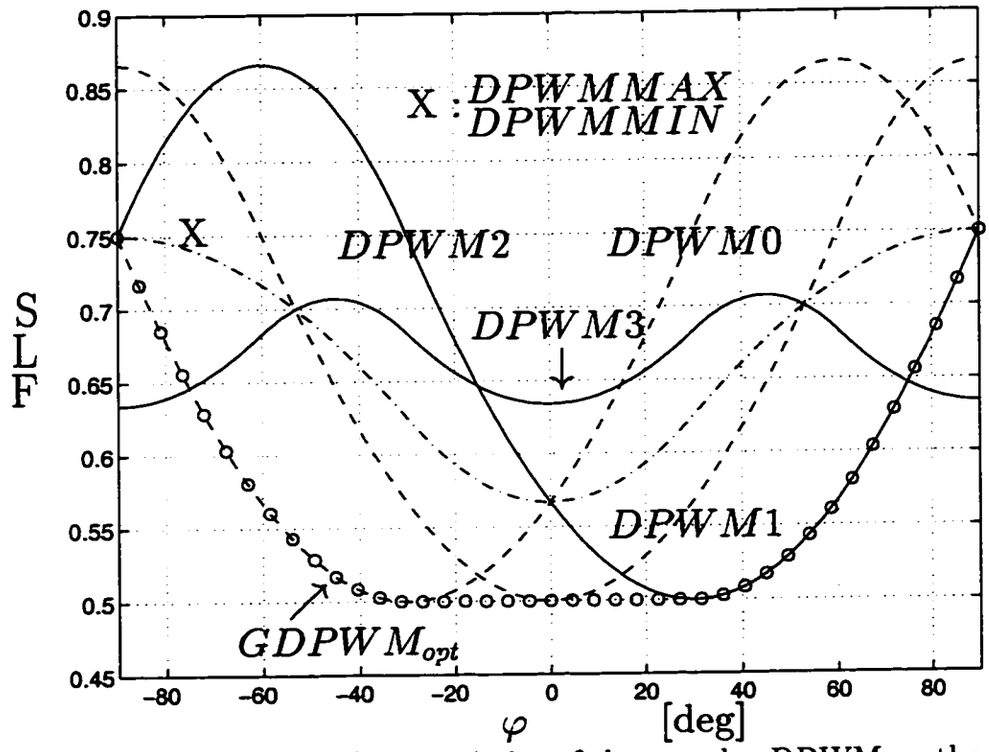

Figure 3.22: $SLF = f(\varphi)$ characteristics of the popular DPWM methods under fixed carrier frequency constraint ($SLF_{CPWM} = 1$).

by allowing the user to configure the modulator of his/her choice, an increased level of performance and satisfaction to the costumer would result. Therefore, this algorithm will be an indispensable feature of future generation drives.

Although the absolute switching loss values obtained from (3.46) may have limited accuracy due to unmodeled switching device characteristics, the relative switching losses which are represented with the SLF function are always predicted with higher accuracy. Since the SLF derivation assumes the same device characteristics both in P_{swave} and P_o, the error direction is the same in both terms and therefore the relative error is less than the absolute error. The SLF functions are effective analytical tools for evaluating and comparing

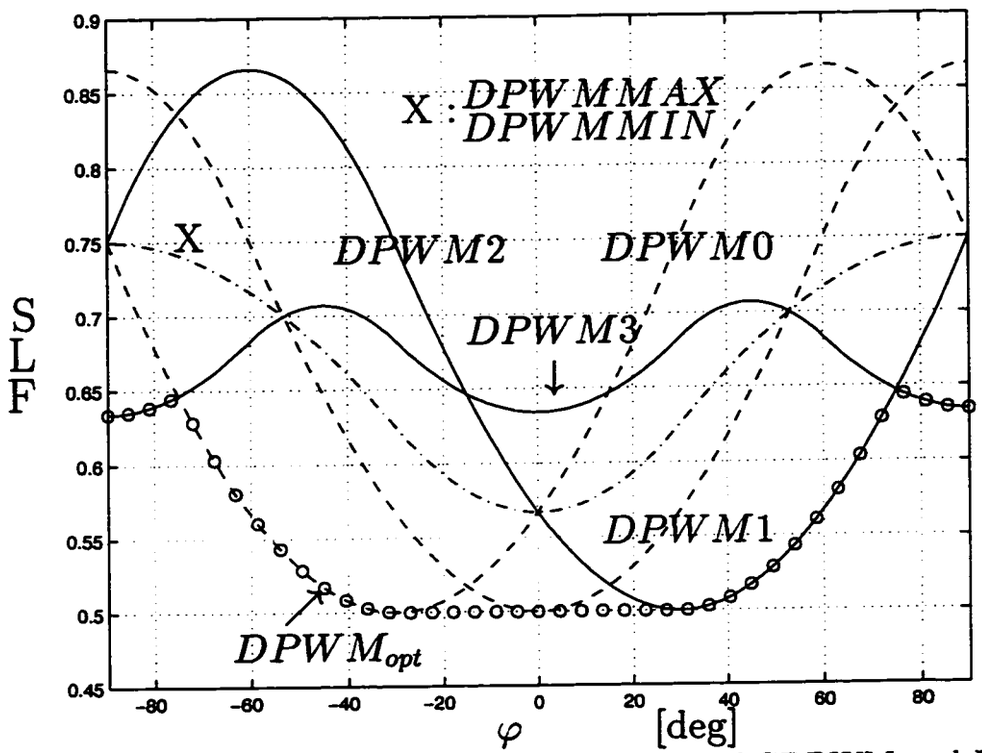

Figure 3.23: Graphic illustrates combining the SLF of GDPWM and DPWM3 minimum switching losses are attained.

the switching losses of various DPWM methods. In particular, the switching loss comparison of different PWM methods with SLF is highly accurate and meaningful. The detailed thermal modeling approach is very laborious [125] and depending on the thermal model accuracy, the calculation accuracy can be poorer than the SLF approach. Device characteristic modeling in a computer simulation is more involved than the first two methods and its accuracy is again limited to the accuracy of the device simulation model.

Unlike the switching losses, the switching device conduction losses are only slightly dependent on the modulator type. The modulator type and load power factor dependency of the conduction losses was investigated thoroughly by Kolar et al. and it was illustrated the zero sequence signal has a negligible influence on the conduction losses [107]. Therefore, switching device loss comparison of various modulators need only involve the SLF function.

When the performance criteria is only switching loss minimization, the above discussed algorithms can utilize the load power factor information and select a modulation signal which minimizes the SLF function. However, as the linear modulation range expires at high modulation index levels, the nonlinear modulation range performance characteristics increasingly dominate the drive performance. The waveform quality, voltage gain, and dynamic performance characteristics of the drive substantially degrade and in addition to SLF and

HDF, the inverter overmodulation performance characteristics must be considered. The following brief section discusses the linearity boundaries of the modern modulators. Then laboratory experiments illustrate the linear modulation region performance characteristics of the conventional and the newly developed high performance modulator/control algorithms.

3.8 Voltage Linearity

In the triangle intersection PWM technique, when the modulation wave magnitude becomes larger than the triangular carrier wave peak value, $\pm\frac{V_{dc}}{2}$, the inverter ceases to match the reference per carrier cycle volt-seconds, and a nonlinear reference-output voltage relation results within certain intervals. The linearity limit of a modulation method can be calculated by equating the peak of the modulation wave to the triangular carrier wave signal magnitude. With each modulation method, the peak of the modulation signal occurs at a different angle. SPWM's linear modulation range ends at $V_{1m}^{*} = \frac{V_{dc}}{2}$ i.e. a modulation index of $M_{LSPWM} = \frac{\pi}{4} \approx 0.785$. As previously discussed, injecting a zero sequence signal to the SPWM signal can flatten and contain the modulation wave within $\pm\frac{V_{dc}}{2}$ such that the linearity range is extended to at most $M_{Lmax} = \frac{\pi}{2\sqrt{3}} \approx 0.907$ which is the theoretical inverter linearity limit [32, 101]. With the exception of THIPWM1/4 which looses linearity at $M_{LTHIPWM1/4} = \frac{3\sqrt{3}}{7\sqrt{7}}\pi \approx 0.881$, all the discussed zero sequence injection PWM methods are linear until M_{Lmax}. Since SVPWM and all the discussed DPWM methods utilize the full inverter

hexagon, it is obvious they all have the same voltage linearity limit of M_{Lmax}. In the direct digital technique, when the reference voltage vector falls outside the modulator linearity region, (3.13) yields $t_0 + t_7 \leq 0$, indicating the reference volt-seconds can not be matched by the inverter and a volt-second error is inevitable. It is obvious that the smallest modulation index where the nonlinear (overmodulation) relation between the reference and output volt-seconds begins is defined by the largest circle inside the inverter hexagon.

Practically the theoretical voltage linearity limits are further reduced due to the inverter blanking time and Minimum Pulse Width (MPW) constraints. With a minimum allowable pulse width of t_{MPW}, a carrier cycle of T_s, and a theoretical modulator voltage linearity limit of M^t_{Lmax}, the practical modulator voltage linearity limit, M^p_{Lmax}, can be calculated by employing (3.4) in the following.

$$M^p_{Lmax} = M^t_{Lmax} \times (1 - k_m \frac{t_{MPW}}{T_s}) \tag{3.54}$$

The k_m coefficient is 1 for DPWM methods and 2 for CPWM methods. Therefore, DPWM methods have superior voltage linearity characteristics. This is due to the fact that DPWM methods utilize only one zero state in a carrier cycle while CPWM methods have two zero states. Therefore, the zero state time length of DPWM methods is always larger than the CPWM methods. Since the smallest zero state time length determines the minimum allowable pulse width, the DPWM methods can accomodate smaller minimum-on-time values. Hence,

a higher linear modulation limit.

In the DPWM methods, the low modulation index operating region also exhibits nonlinear reference-output voltage relations. Since in these methods the zero sequence signal at near zero modulation index is substantially large, the injection of this signal to the sinusoidal reference signals results in nearly saturated modulation signals. Figure 3.24 illustrates the modulation signal and the zero sequence signal at low modulation for DPWM1. Therefore, the DPWM methods have a lower limit on the voltage linearity. This limit can be calculated in a similar manner to the maximum voltage linearity limit. It can be seen in Fig. 3.24, the DPWM1 narrow pulse occurs at the $\theta = 0$ point and repeats every sixty-degrees. Again, the duty cycle calculation can be performed to determine the minimum voltage linearity limit. The calculation yields the following practical minimum voltage linearity limit equation which holds for all the discussed DPWM methods.

$$M_{Lmin}^{p} = \frac{\pi}{\sqrt{3}} \frac{t_{MPW}}{T_s} \tag{3.55}$$

The region starting from the end of the linear modulation region of a modulator until the six-step operating point ($M_i = 1$) is called the overmodulation region. All the PWM-VSI drives experience performance degradation in the overmodulation region [64, 75, 88, 169]. In the DPWM methods, as discussed in the above paragraph, from zero modulation index until M_{Lmin}^{p} an additional

nonlinear region exists. Perhaps, this nonlinear region can be termed as "undermodulation" region. In this region, similar performance problems as in the overmodulation region exist. In the overmodulation and undermodulation regions, the HDF and SLF functions are not accurate and they are not a suitable measure for performance evaluation. The following two chapters will investigate the overmodulation region behavior of different drive types and modulators. The influence of the blanking time and minimum pulse width on the modulator linearity will also be discussed in more detail. However, at this stage the linear modulation region drive performance laboratory investigations will be reported.

3.9 Experimental Results

The high performance PWM algorithm, which combines the SVPWM and GDPWM method superior performance characteristics, was tested in the laboratory on a $\frac{V}{f}$ controlled 5 HP induction motor drive. The VSI utilized a diode rectifier front end with a DC bus voltage of 620 V. The PWM-VSI drive control board was fully digital and employed a 40 MHz, 24-bit fixed point DSP. The digital PWM algorithm employed the triangular intersection technique and a simple software code generated the modulation signals. The carrier frequency was fixed at 5 kHz and modulation waves were fed to the digital PWM counters to generate the VSI gate switch signals. The drive had a $4\mu s$ blanking time, and through symmetric blanking time compensation the voltage pulses were precisely generated [117].

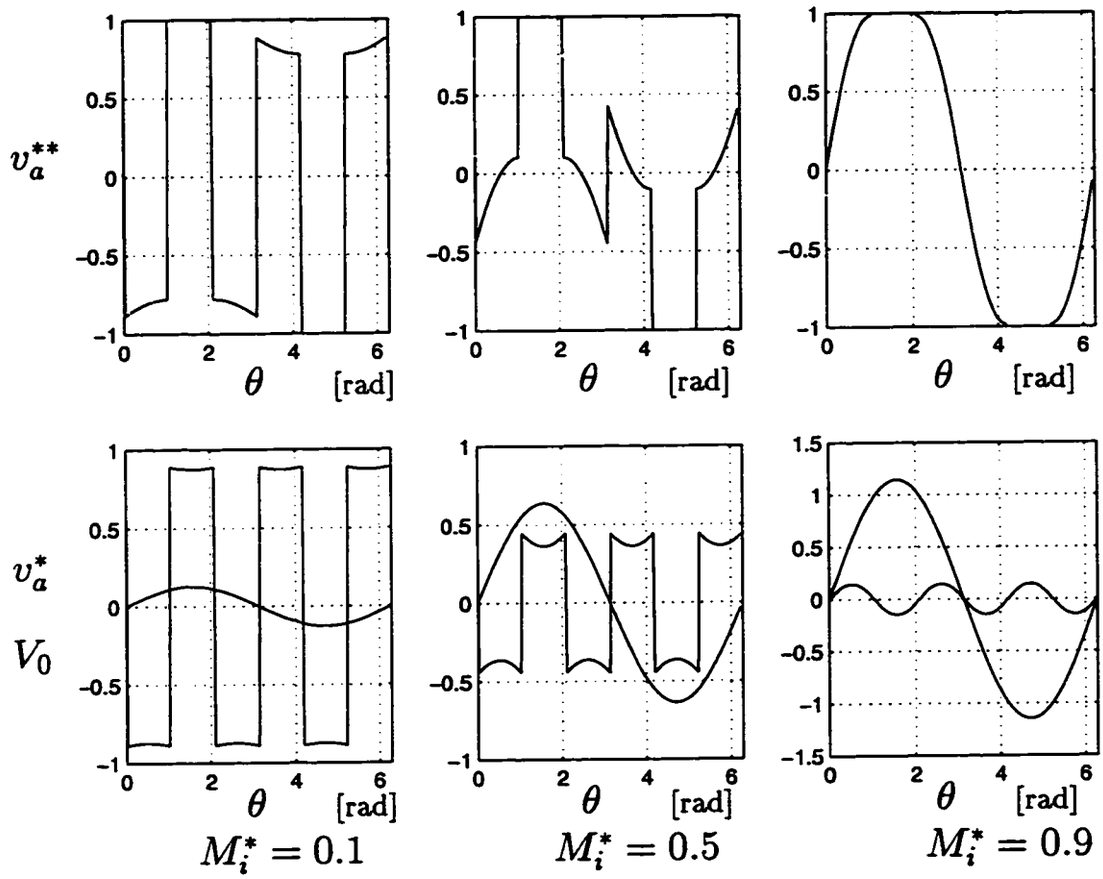

Figure 3.24: The modulation and zero sequence signals of DPWM1 for three M_i values.

The DSP generated the SVPWM and GDPWM modulation signals by employing the magnitude rules described in this chapter. Since the carrier frequency was fixed at 5 kHz, the theoretical HDF curve of SVPWM would be superior to GDPWM's curve within the linear modulation region. A transition from SVPWM to GDPWM in the linear modulation region would, therefore, imply waveform quality degradation. However, as discussed in the voltage linearity section of this chapter, the voltage linearity region of SVPWM expires before the GDPWM in the presence of minimum pulse width constraints. In the laboratory tests, a minimum pulse width control algorithm was employed and voltage pulses less than $12\mu s$ were eliminated (this approach is termed as Pulse Elimination Method (PEM)). With the given minimum pulse width constraint, the SVPWM linearity limit was calculated from (3.54) as $M_{iSVPWMmax} = 0.798$. This modulation index value could be selected as the transition modulation index from SVPWM to GDPWM. However, the experimental observation suggested that the current waveform quality with SVPWM did not immediately degrade and was slightly better than with GDPWM until approximately 0.81. Therefore, the transition modulation index value was selected as $M_{itr1} = 0.81$. Above this value, GDPWM was employed. The GDPWM method employed minimum SLF control algorithm ($\psi = \varphi + \frac{\pi}{6} \leq \frac{\pi}{3}$ for motoring) until the end of the linear region. The phase difference between a modulation wave and the corresponding phase current was measured to estimate the power factor angle.

Figure 3.25, Figure 3.26, and Figure 3.27 illustrate the modulation signal and motor phase current waveforms immediately before, during, and after transition

($M_i = 0.79, 0.81, 0.82$) at 50% of the rated motor torque (T_{eR}). Shown in the same oscillograms, the modulation waves were output from the DSP through and A/D converter and the triangular carrier signal gain is 10V/620V. The current waveform quality of all three figures, in particular the peak current ripple, is practically the same. Since the speed reference signal of the drive was fed to the DSP through an A/D converter, at the transition modulation index operating point ($M_i = M_{itr1}$) a small reference signal noise resulted in an oscillation between SVPWM and GDPWM. However, this zero sequence signal oscillation only affected the carrier frequency harmonic content of the motor current and as Fig. 3.26 shows, it would not disturb the motor current fundamental component and motion quality. This result is in correlation with the theory, which indicates the harmonic flux is zero at the beginning and the end of the carrier cycle. Due to the load equivalent resistance, the harmonic currents become slightly different from zero at the beginning and the end of the cycle. However, the residue current exponentially decays to zero with the load equivalent circuit R-L time constant. Therefore, rapid transition from SVPWM to GDPWM and back does not result in performance degradation. Therefore, it is not necessary to prohibit oscillations with any involved control algorithms.

Since the carrier frequency was constant, changing from SVPWM to GDPWM results in significant reduction in switching losses. With the power factor angle at the 50 % load operating point being larger than 30°, the SLF curve in Figure 3.22 indicates the losses are reduced by at least 45% when compared to SVPWM. As shown in Fig. 3.28 at $M_i = 0.854$ and 100% T_{eR}, the algorithm

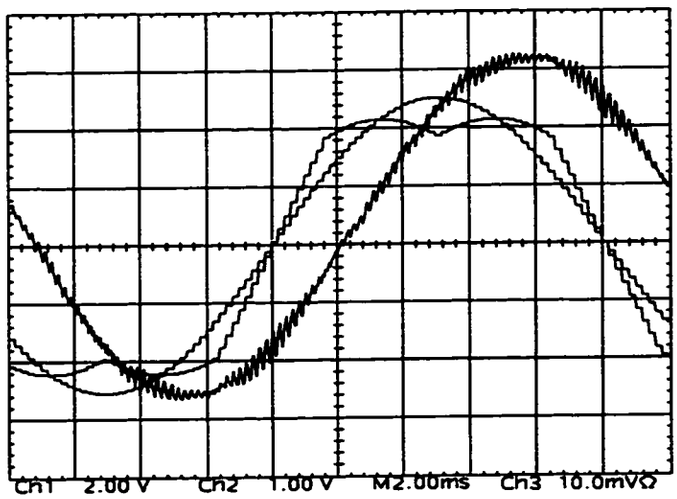

Figure 3.25: Experimental SVPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.79$, 49 Hz, $50\%T_{eR}$). Scales: 2 A /div, 2 V /div, 2ms/div.

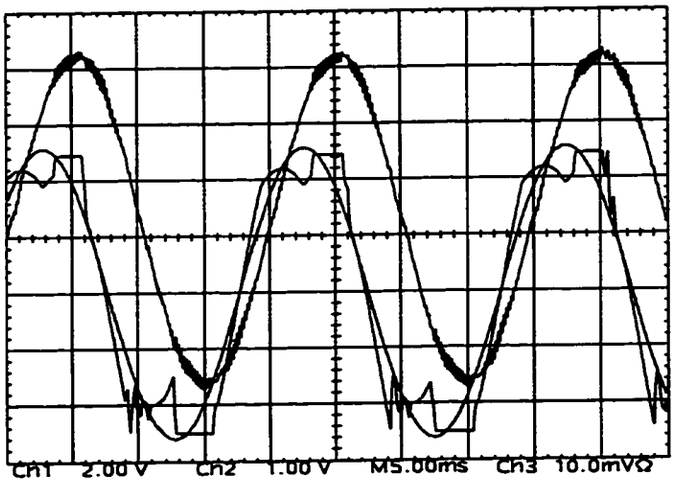

Figure 3.26: Transition from SVPWM to GDPWM ($M_i = 0.81$, 50 Hz, $50\%T_{eR}$). Scales: 2 A /div, 2 V /div, 5ms/div.

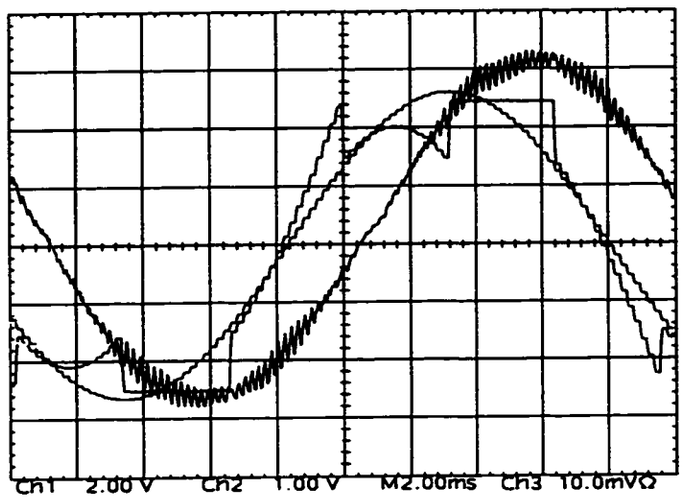

Figure 3.27: Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms (M_i = 0.82, 51 Hz, 50%T_{eR}). Scales: 2 A /div, 2 V /div, 2ms/div.

on-line optimizes ψ to minimize the switching losses. Since the power factor angle for this operating condition is less than 30°, the transistor which conducts the largest current is held on and this reduces the switching losses by approximately 50% when compared to SVPWM. Confirming the improvement in the switching losses, the laboratory measurements showed notable decrease in the heat sink temperature. The experimental data for these operating conditions is illustrated in Table 3.1 in detail. The table indicates the GDPWM full load switching losses are less than the SVPWM switching losses under 50 % load operating condition.

A PWM algorithm which is solely based on not modulating the phase current with the largest magnitude [162] does not guarantee voltage linearity (at any M_i) except for the power factor angle range of $-30° < \varphi < 30°$. If the power factor angle is outside this range, and the phase with the largest current is clamped

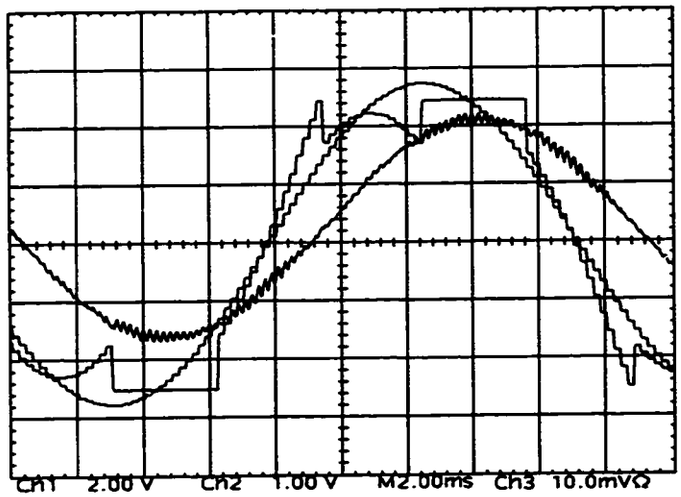

Figure 3.28: Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.854$, 53 Hz, $100\%T_{eR}$). Scaling: 5 A /div, 2 V /div, 2ms/div.

Table 3.1: SVPWM and GDPWM thermal performance data comparison

Method	M_i	T_L %	I_{max} (A)	T ($°C$)
SVPWM	0.79	50	6	31.2
$GDPWM_{opt}$	0.81	50	6	30.6
$GDPWM_{opt}$	0.854	100	10	30.8

to the positive/negative DC rail, the zero sequence signal becomes too large in magnitude. Regardless the modulation index value, the modulation signal of at least one of the two remaining phases saturate and nonlinear modulation results. Therefore, the GDPWM approach is superior.

Since the experimental system employs a PEM algorithm, the voltage linearity of GDPWM method practically ends at 0.854 modulation index (calculated from (3.54)). The modulator and drive behavior outside this region (in the overmodulation region), will be discussed in the next chapter in detail and experimental results will be provided.

3.10 Summary

In this chapter, modern carrier based PWM methods were thoroughly reviewed. Reviewing the principles and building correlation between various methods, it has become possible to group the methods, find equivalency between several methods, and furthermore establish a unified approach to study, evaluate, and program all the PWM methods. The well known waveform quality and switching loss function characteristics of the modern PWM methods have been reviewed and the algebraic functions simplified and gathered to form a user-friendly "PWM toolbox." These tools were utilized to illustrate and compare the performance characteristics of various PWM methods. The switching loss and waveform quality comparisons indicate SVPWM at low modulation and

DPWM methods at the high modulation range have superior performance. The tools and graphics aid the modulator selection and PWM inverter design process. The magnitude test is an elegant method for generating the modulation waveforms fast and accurately by digital hardware/software or analog hardware. The analytical methods are also helpful in generating graphics of the microscopic current ripple characteristics and illustrating the performance characteristics and the difference between various modulators. Therefore, they aid visual learning. As a result, the linear modulation region performance analysis provided in this chapter helps the PWM learning and design experience become simple and intuitive. Furthermore, it lays the foundations for the investigation of the overmodulation region modulator behavior.

In this chapter, also the GDPWM method with on-line performance optimization capability has been developed and its characteristics have been analytically and experimentally studied. An algorithm that combines the superior high modulation range performance characteristics of GDPWM and the superior low modulation range performance characteristics of SVPWM method has been developed and implemented. The self-optimization procedure of the algorithm which minimizes the harmonic distortion and reduces the switching losses has been described. The algorithm has a simple structure and it is suitable for DSP or microprocessor based digital implementation. The phase angle ψ of the modulator is on-line controlled in order to optimize the drive performance and reduce the switching losses. The operating characteristics of the GDPWM method and the high performance PWM algorithm have been verified in the

laboratory tests. The losses, harmonic distortion and other characteristics have been both experimentally and theoretically investigated and reported. The transition modulation index value from SVPWM to GDPWM was investigated and an approach to estimate this value has been proposed.

With the linear modulation region performance of all the modulators well defined and illustrated in this chapter, the overmodulation region performance of these modulators remain unknown. Should the PWM method with the highest overmodulation region performance be known, the only remaining task would be to integrate its modulation algorithm to the high performance PWM algorithms discussed in this chapter. However, with the HDF and SLF functions not being valid in the overmodulation region, the overmodulation region performance of the modern PWM methods is difficult to predict. The following chapters investigate the overmodulation region performance of voltage feedforward controlled drives and closed loop current controlled drives.

Throughout this study it has been found the performance of voltage feedforward controlled and closed loop current controlled drives involve different modulator overmodulation performance characteristics. Therefore, in this work voltage feedforward drives and closed loop current controlled drives have been separately investigated and reported. With the voltage feedforward drive performance issues being simpler than the closed loop current controlled drives, the voltage feedforward controlled drive overmodulation issues are investigated first.

Chapter 4

Overmodulation in Voltage Feedforward Controlled Drives

4.1 Introduction

In the previous section the linear modulation range behavior of the modern carrier based PWM methods was studied in detail. Their performance characteristics were analytically derived and graphically illustrated. It was shown several modern PWM methods exhibit superior performance characteristics and their application areas were identified. However, all the carrier based PWM methods provide a linear relationship between the reference and the output voltages within a limited range.

The linear voltage range of a PWM-VSI drive is mainly determined by the modulator characteristics. Using the modulation index definition of the previous chapter, full voltage utilization (six-step operating mode) occurs at $M_i = 1$. Normalizing the triangular wave peak-to-peak signal magnitude to V_{dc}, it follows that SPWM's linear modulation range ends at $V_{1m} = \frac{V_{dc}}{2}$, a modulation index

of $M_{imax[SPWM]} = \frac{\pi}{4} \approx 0.785$. Inverter blanking time and minimum-pulse-width constraints can further reduce the range of linearity by a considerable amount. As a result, the voltage linearity of a drive, for example, in the SPWM case, can be lost at as low a value as 70% of the six-step voltage, i.e. 0.7 modulation index. Figure 4.1 illustrates the typical linear and nonlinear range modulation waveforms of the SPWM method, and switching device gate logic signals. The portion of the modulation wave having a larger magnitude than the triangular wave peak value remains unmodulated, and the gate signals remain on or off for a full carrier cycle leading to a nonlinear reference-output voltage relationship.

The voltage linearity of a modulator can be significantly increased by injecting a zero sequence signal. For example, in the SVPWM case, the theoretical limit can be easily calculated by evaluating the modulation signal at the 30° point (see Fig. 3.7 SVPWM modulation waveform), where the zero sequence signal becomes zero and this calculation yields $M_{imax[PWM]} = \frac{\pi}{2\sqrt{3}} \approx 0.907$. With the exception of THIPWM1/4, the theoretical linearity limit of all the discussed zero sequence injection PWM methods is equal to this inverter theoretical limit. In the THIPWM1/4 method, the linearity is limited to 0.885 modulation index. However, in all these methods the inverter blanking time and minimum-pulse-width constraints imply a narrower voltage linearity range than the theoretical. Therefore, in all the discussed modulation methods, a wide overmodulation range with poor performance characteristics results.

Operating in the nonlinear modulation range, or in more common terms

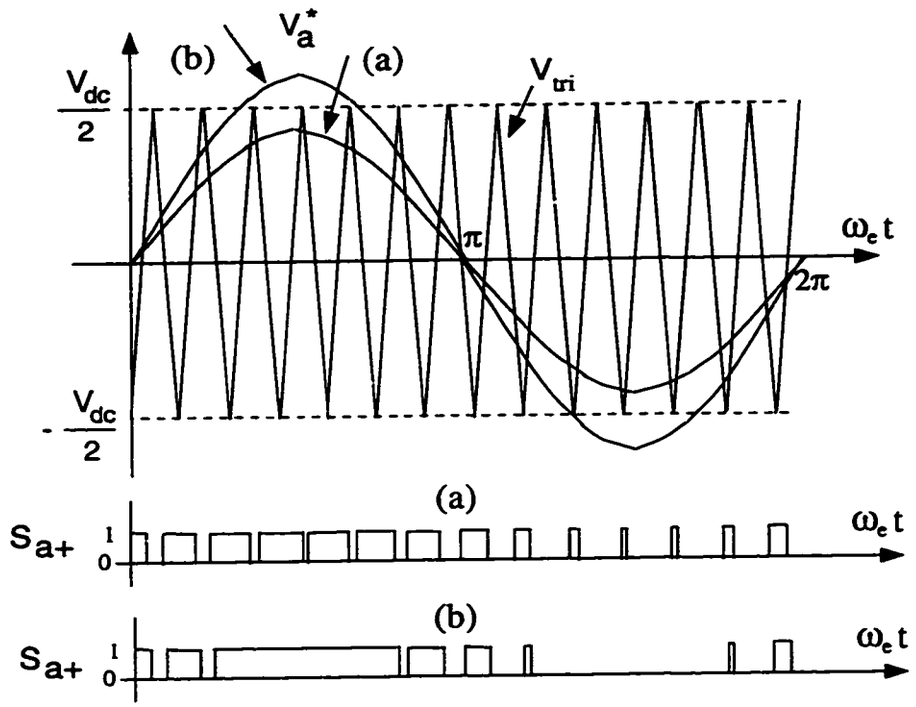

Figure 4.1: SPWM modulation waveforms and switching device gate logic signals. (a): linear modulation range, (b): overmodulation range.

the overmodulation range is problematic: large amount of subcarrier frequency harmonic voltages/currents are generated, the fundamental component voltage gain significantly decreases, and the switching device gate pulses are abruptly dropped. In $\frac{V}{f}$ controlled PWM-VSI AC motor drives, operation in this range results in poor performance. The current ripple, and therefore, the torque ripple substantially increases. Near the six-step operating point, the harmonic current magnitude can become significantly large and frequent overcurrent fault conditions may occur. Abruptly eliminating narrow voltage pulses can induce significant transients and the poor overmodulation performance condition can be further exacerbated.

On the other hand, full inverter voltage utilization is important from cost and power density improvement perspectives. Also a drive with high overmodulation performance is less sensitive to inverter DC link voltage disturbances. In certain applications, operation in the overmodulation region may not be necessary under normal operating conditions. However, a DC link voltage sag may result an unintentional entrance to the overmodulation region. In particular, in diode rectifier front end type drives (the widemost utilized rectifier type), AC utility line voltage sag or fault conditions frequently occur and a drive operating near its rated voltage may frequently enter the overmodulation region. Under such conditions, a high performance overmodulation method could maintain the drive performance as much as possible. Hence, increased drive reliability. Therefore, the overmodulation region performance of a drive and its modulator are important and will be investigated in this chapter in detail.

With the focus being on the voltage feedforward controlled $\frac{V}{f}$ drives, in this chapter the steady state overmodulation behavior of the modern modulators and voltage feedforward drives will be investigated. Therefore, the fundamental component voltage gain and steady state voltage/current waveform quality of the modern modulators will be analyzed in detail and performance comparison will follow. The influence of the blanking time on the modulator overmodulation range performance will be discussed. The detailed analytical and numerical investigations of modulator performance characteristics and the performance comparison will aid the overmodulation region modulator selection and design procedure. Following the establishment of high performance overmodulation algorithms, the laboratory experiments will illustrate the effectiveness of the proposed method.

4.2 Overmodulation Range Voltage Gain Characteristics

In the triangle intersection technique, when the modulation wave magnitude becomes larger than the peak of the triangular wave, switching during that carrier cycle ceases, and the corresponding switch remains locked to the inverter pole within the carrier cycle. This condition is defined as the "saturation" of the particular phase. Though not commonly utilized, the terms "unmodulated phase" will be frequently utilized in this thesis to indicate the modulation signal

of the corresponding phase becomes larger than the triangular carrier wave and modulation ceases. In the beginning of the overmodulation region, depending on the modulator type, one or two of the three modulation waves are simultaneously saturated. As the modulation index increases, the saturated segments of each modulation wave and the number of simultaneously saturated phases increase according to the waveform characteristic of each modulator until the six-step operating mode is reached.

When saturation occurs, the reference per carrier cycle average voltage can not be matched by the inverter, and a voltage gain reduction results. This nonlinear voltage gain relation can be analytically modeled by Fourier analysis of the saturated modulation wave independently of the carrier frequency. Utilizing the modulation index definition, general formulas can be derived independent of the inverter voltage. However, except for the SPWM method, the voltage gain formulas of the carrier based PWM methods have not been reported, nor has a detailed gain characteristic study been conducted [52, 147, 169]. The SPWM method gain, and the gain of several other functions frequently encountered in the servomechanism systems were established many decades ago and instead of gain, the term "describing function" was utilized [52, 147]. However, the zero sequence signal injection technique, which yields functions unique to three phase systems, has not been common in control system applications. Therefore, the gain functions of zero sequence signal injection PWM methods have not been investigated until now. In the following, the gain formulas of the modern modulators are derived and a comparative evaluation follows.

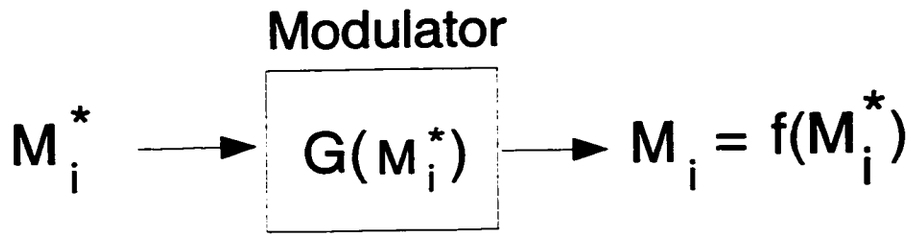

Figure 4.2: Modulation index gain block diagram of a PWM-VSI

The fundamental component voltage gain of a modulator is the ratio of the output voltage fundamental component peak value V_{1m} to the reference modulation wave fundamental component peak value V_m^*. Utilizing the modulation index and reference modulation index definitions, it can also be expressed in terms of the modulation indices as:

$$G = \frac{V_{1m}}{V_m^*} = \frac{M_i}{M_i^*} \tag{4.1}$$

The fundamental component gain formulas can be utilized in the drive overmodulation range behavior analysis, simulation, and control. With their analysis and graphic illustration, the overmodulation region behavior of the modern modulators can be studied and compared. The overmodulation region behavior of the drive can be modeled with the gain functions in computer simulations. With no PWM signals involved, the simulation can be rapid and accurate. The gain functions can also be utilized in developing a gain linearizing block for a drive controller such that proper voltage control is maintained. The the following the voltage gain functions of the modern modulators are calculated.

4.2.1 SPWM

As shown in Fig. 4.3, the SPWM modulation signal has quarter-wave symmetry in the overmodulation region. Utilizing this quarterwave symmetry, we calculate the fundamental component by means of Fourier analysis in the following equation.

$$V_{1m} = \frac{4}{\pi}\left(\int_0^{\alpha_s} V_m^* \sin\theta \sin\theta d\theta + \int_{\alpha_s}^{\frac{\pi}{2}} \frac{V_{dc}}{2} \sin\theta d\theta\right) \tag{4.2}$$

Writing the output voltage fundamental component in terms of the modulation index value, the following relation between the reference voltage modulation index M_i^*, and output voltage fundamental component modulation index M_i yields [169, 147, 52].

$$M_i = \left(\frac{2}{\pi}\right) M_i^* \arcsin\left(\frac{\pi}{4M_i^*}\right) + \left(\frac{1}{2}\right)\sqrt{1 - \left(\frac{\pi}{4M_i^*}\right)^2} \tag{4.3}$$

Since the output voltage fundamental component is different from the reference voltage, the output modulation index M_i has a different value from the reference modulation index M_i^*. Utilizing the definition of (4.1), the fundamental component voltage relation can be expressed by the following gain function.

$$G = \left(\frac{2}{\pi}\right) \arcsin\left(\frac{\pi}{4M_i^*}\right) + \left(\frac{1}{2M_i^*}\right)\sqrt{1 - \left(\frac{\pi}{4M_i^*}\right)^2} \tag{4.4}$$

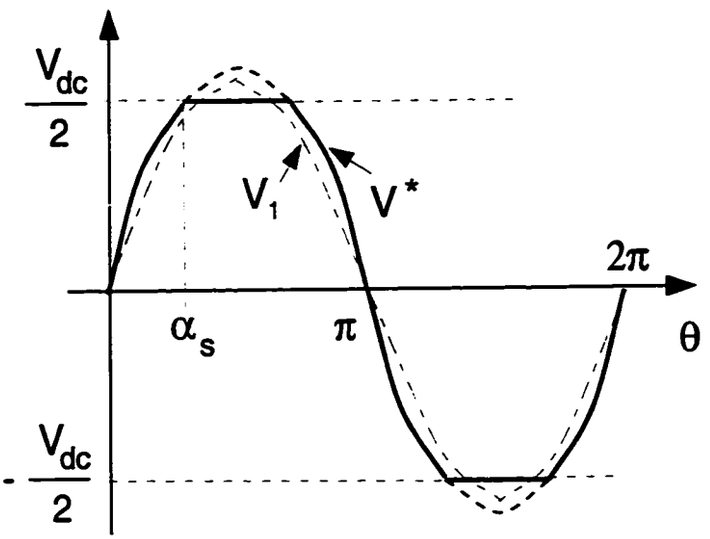

Figure 4.3: The sinusoidal PWM modulator saturation waveforms.

4.2.2 SVPWM

The overmodulation range characteristics of the triangle intersection implementation of the SVPWM can be closed form modeled in the same manner as SPWM. As illustrated in Fig. 4.4, the overmodulation region consists of two sub-regions. Region I has two intersections between the saturation line and the modulation waveform per quarter wave while region II has only one intersection. Employing Fourier analysis, the fundamental component modulation index and voltage gain relations of overmodulation region I are found as follows.

$$M_i = -\frac{1}{2}M_i^* + \frac{3}{\pi}M_i^* \arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\right) + \frac{\sqrt{3}}{2}\sqrt{1-\left(\frac{\pi}{2\sqrt{3}M_i^*}\right)^2} \qquad (4.5)$$

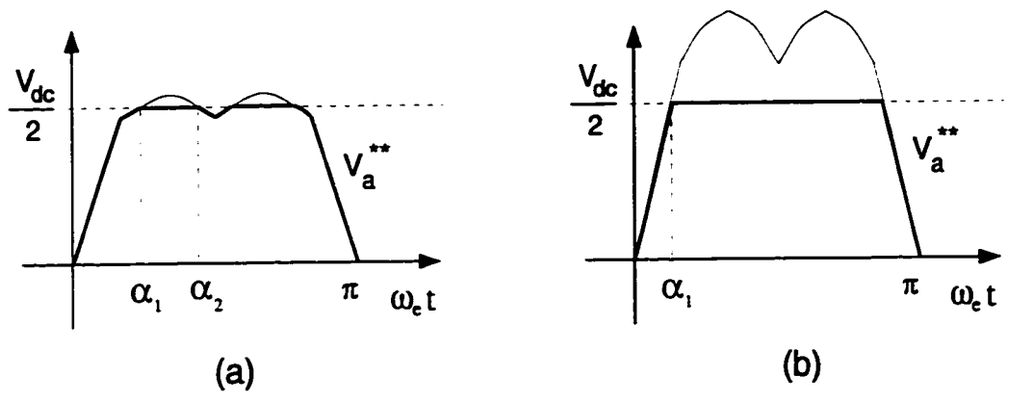

Figure 4.4: SVPWM triangle intersection method modulation waveforms in the overmodulation region. (a): Region I, (b): Region II.

$$G = -\frac{1}{2} + \frac{3}{\pi}\arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\right) + \frac{\sqrt{3}}{2M_i^*}\sqrt{1-\left(\frac{\pi}{2\sqrt{3}M_i^*}\right)^2} \tag{4.6}$$

Region II begins at $M_i^* = \frac{\pi}{3} \approx 1.047$ ($M_i \approx 0.957$), and the modulation index and gain relations in this region are calculated as follows.

$$M_i = \frac{3}{\pi}M_i^*\arcsin\left(\frac{\pi}{6M_i^*}\right) + \frac{1}{2}\sqrt{1-\left(\frac{\pi}{6M_i^*}\right)^2} \tag{4.7}$$

$$G = \frac{3}{\pi}\arcsin\left(\frac{\pi}{6M_i^*}\right) + \frac{1}{2M_i^*}\sqrt{1-\left(\frac{\pi}{6M_i^*}\right)^2} \tag{4.8}$$

4.2.3 THIPWM1/6

The zero sequence signal of THIPWM1/6 can be algebraically defined as $v_0 = \frac{1}{6}V_{1m}\sin(3w_e t)$ [32]. This definition is based on the assumption that the associated modulation function prior to zero sequence signal injection is a sine

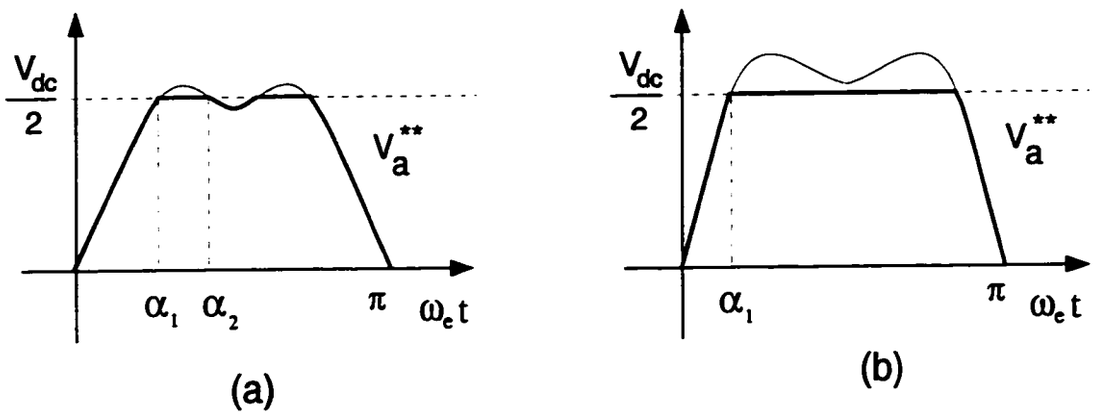

Figure 4.5: THIPWM1/6 waveforms in the overmodulation region. (a): Region I, (b): Region II.

function. The overmodulation voltage gain relations of this method are quite similar to the SVPWM methods.

As shown in Fig. 4.5 (a), in region I, the modulator waveform intersects with the saturation line twice per quarter-fundamental cycle. The intersection angles are calculated from the following transcendental equation.

$$\sin\alpha_{1,2} + \frac{1}{6}\sin 3\alpha_{1,2} = \frac{\pi}{4M_i^*} \tag{4.9}$$

The above equation can be easily solved by iterative methods. Utilizing the intersection angle values, the reference-output voltage relationship can be computed by the following formula established by the Fourier analysis of the modulation wave:

$$M_i = (\frac{2}{\pi})M_i^*(\frac{\pi}{2} + \alpha_1 - \alpha_2 + \frac{5}{12}(\sin 2\alpha_2 - \sin 2\alpha_1) +$$

$$\frac{1}{24}(\sin 4\alpha_2 - \sin 4\alpha_1)) + \cos\alpha_1 - \cos\alpha_2 \tag{4.10}$$

The above formula is valid until the reference modulation index value of $M_i^* = \frac{3\pi}{10} \approx 0.943$ and then region II begins. While in region II, only one intersection point exists and can be calculated from (4.9). Finally, the modulation index can be calculated from the Fourier analysis derived formula as follows.

$$M_i = (\frac{2}{\pi})M_i^*(\alpha_1 - \frac{5}{12}\sin 2\alpha_1 - \frac{1}{24}\sin 4\alpha_1) + \cos\alpha_1 \tag{4.11}$$

Although the above formulas are dependent on the intersection angles and difficult to completely write in full closed form, they can be easily evaluated by simple numerical software packages. Once the modulation index values are calculated, the gain can be easily computed from (4.1).

4.2.4 THIPWM1/4

The zero sequence signal of THIPWM1/4 can be algebraically defined as $v_0 = \frac{1}{4}V_{1m}\sin(3w_e t)$ [32]. THIPWM1/4 looses linearity at $M_i^* = \frac{3\sqrt{3}}{7\sqrt{7}}\pi \approx 0.885$ and its overmodulation gain characteristic can be evaluated following the same algebraic steps described in the THIPWM1/6 case.

Similar to the THIPWM1/6 case, in region I, the modulator waveform intersects with the saturation line twice per quarter-fundamental cycle. The intersection angles are calculated from the following transcendental equation.

$$\sin\alpha_{1,2} + \frac{1}{4}\sin 3\alpha_{1,2} = \frac{\pi}{4M_i^*} \tag{4.12}$$

Similar to the THIPWM1/6 case, the above equation can be easily solved by iterative methods. Utilizing the intersection angle values, the reference-output voltage relationship can be computed by the following formula established by the Fourier analysis of the modulation wave:

$$\begin{aligned} M_i = (\frac{2}{\pi})M_i^*(\frac{\pi}{2} + \alpha_1 - \alpha_2 + \frac{3}{8}(\sin 2\alpha_2 - \sin 2\alpha_1) + \\ \frac{1}{8}(\sin 4\alpha_2 - \sin 4\alpha_1)) + \cos\alpha_1 - \cos\alpha_2 \end{aligned} \tag{4.13}$$

The above formula is valid until the reference modulation index value of $M_i^* = \frac{\pi}{3} \approx 1.0472$ and then region II begins. While in region II, only one intersection point exists and can be calculated from (4.12). Finally, the modulation index can be calculated from the Fourier analysis derived formula as follows.

$$M_i = (\frac{2}{\pi})M_i^*(\alpha_1 - \frac{3}{8}\sin 2\alpha_1 - \frac{1}{8}\sin 4\alpha_1) + \cos\alpha_1 \tag{4.14}$$

The above formulas can be computed with numerical software in a similar manner to the THIPWM1/6 case. Once the modulation index values are calculated, the gain can be easily computed from (4.1).

4.2.5 DPWM1

As shown in Fig. 4.6, once in the overmodulation range, the saturated segments of DPWM1 increase beyond the 60° span of the linear modulation range, and the modulation wave is upward shifted by an amount dependent on the modulation index value. As shown in Fig. 4.6, the quarterwave consists of the sinusoidal portion, and beyond the point of saturation, which is indicated as α_s, the reference voltage waveform consists of the constant voltage portion with the value of $\frac{V_{dc}}{2}$. The fundamental component voltage formula is therefore in the following.

$$V_{1m} = \frac{4}{\pi}\left(\int_0^{\alpha_s}\left(V_m^*(\sin\theta - \sin(\theta - \frac{2\pi}{3})) - \frac{V_{dc}}{2}\right)\sin\theta d\theta + \int_{\alpha_s}^{\frac{\pi}{2}} \frac{V_{dc}}{2}\sin\theta d\theta\right) \quad (4.15)$$

Fourier analysis of the saturated wave yields the following modulation index and voltage gain relations.

$$M_i = -1 + (\frac{\sqrt{3}}{\pi} - \frac{1}{2})M_i^* + (\frac{\pi}{4\sqrt{3}})\frac{1}{M_i^*} + (\frac{3}{\pi})M_i^* \arcsin(\frac{\pi}{2\sqrt{3}M_i^*}) + (\frac{\sqrt{3}}{2})\sqrt{1 - (\frac{\pi}{2\sqrt{3}M_i^*})^2} \quad (4.16)$$

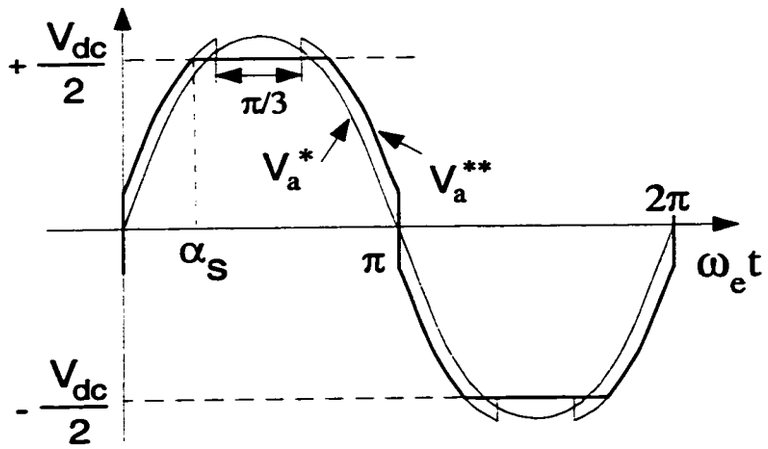

Figure 4.6: DPWM1 method overmodulation waveforms.

$$G = \frac{-1}{M_i^*} + (\frac{\sqrt{3}}{\pi} - \frac{1}{2}) + (\frac{\pi}{4\sqrt{3}})\frac{1}{M_i^{*2}} + (\frac{3}{\pi})\arcsin(\frac{\pi}{2\sqrt{3}M_i^*}) + (\frac{\sqrt{3}}{2M_i^*})\sqrt{1-(\frac{\pi}{2\sqrt{3}M_i^*})^2} \qquad (4.17)$$

4.2.6 DPWM2 and DPWM0

The DPWM2 modulation wave is not quarter-wave symmetric, hence the overmodulation voltage gain equations are complex compared to the previous cases.

As shown in Fig. 4.7, the overmodulation region is divided into two subregions. In the first subregion, as shown in Fig. 4.7 (a), the modulation wave has four saturated segments per fundamental cycle. Employing Fourier analysis and utilizing the intermediate variables ψ, a_1, and b_1, the voltage relations in the first region can be calculated from the following equations.

$$\psi = -\frac{\pi}{3} + \arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\right) \tag{4.18}$$

$$a_1 = \frac{M_i^*}{4} - \frac{\sqrt{3}}{2}\sin\left(\psi - \frac{\pi}{6}\right) + \frac{3\psi}{2\pi}M_i^* - \frac{3}{4\pi}M_i^*\cos\left(2\psi + \frac{\pi}{6}\right) \tag{4.19}$$

$$b_1 = -\frac{1}{2}\cos\left(\psi + \frac{\pi}{3}\right) + \frac{\sqrt{3}}{4\pi}M_i^*\left(\frac{\pi}{3} - 2\psi - \sin\left(2\psi - \frac{\pi}{3}\right)\right) \tag{4.20}$$

$$M_i = \sqrt{a_1^2 + b_1^2} \tag{4.21}$$

The second subregion begins at $M_i^* = \frac{\pi}{3}$. Shown in Fig. 4.7 (b) the modulation wave heavily saturates and on each side two saturated segments merge, leading to only two saturated segments per cycle. Introducing the variable α, the coefficients a_1, and b_1 can be calculated as follows.

$$\alpha = \frac{2\pi}{3} - \arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\right) \tag{4.22}$$

$$a_1 = \frac{\sin\alpha}{2} + \left(\frac{1}{2} - \frac{\sqrt{3}}{8\pi} - \frac{3}{4\pi}\alpha\right)M_i^* - \frac{\sqrt{3}}{4\pi}M_i^*\cos\left(2\alpha - \frac{2\pi}{3}\right) \tag{4.23}$$

$$b_1 = -\frac{\cos\alpha}{2} + \frac{\sqrt{3}}{2\pi}M_i^*\left(\frac{\sqrt{3}}{4} - \frac{1}{2}\sin\left(2\alpha - \frac{2\pi}{3}\right) + \frac{\pi}{3} - \frac{\alpha}{2}\right) \tag{4.24}$$

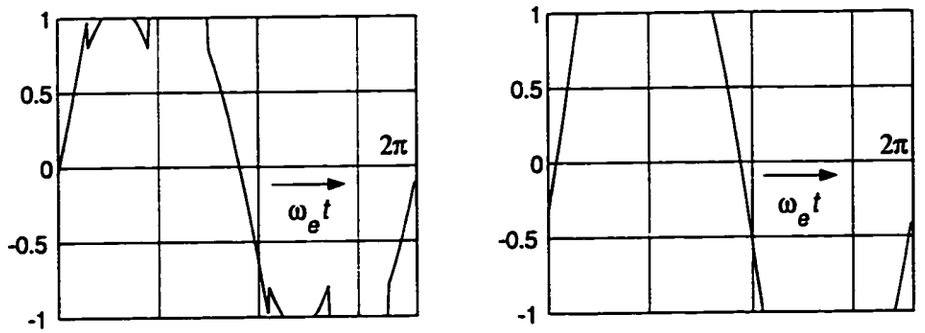

Figure 4.7: DPWM2 overmodulation waveforms. (a): Region I, (b): Region II.

Once the above coefficients are known, the reference-output voltage relations can be calculated from (4.21) and the voltage gain can be calculated in both subregions from the definition of (4.1).

The modulation waves of DPWM2 and DPWM0 are only different by the position of the unmodulated segment. Therefore, Fourier analysis of both yield the same fundamental component gain results. For this reason the derivation for DPWM0 will not be pursued and the above results can be readily utilized when necessary.

4.2.7 DPWM3

As shown in Fig. 4.8, the overmodulation region of DPWM3 is divided into three subregions. The first subregion covers the reference modulation index range of $\frac{\pi}{2\sqrt{3}} \leq M_i^* \leq \frac{\pi}{3}$. In this region the modulation index relations are calculated in the following.

$$M_i = 1 + (1 - \frac{\sqrt{3}}{\pi})M_i^* - \frac{\pi}{4\sqrt{3}M_i^*} - \frac{3}{\pi}M_i^* \arccos(\frac{\pi}{2\sqrt{3}M_i^*}) + \frac{\sqrt{3}}{2}\sqrt{1 - (\frac{\pi}{2\sqrt{3}M_i^*})^2} \quad (4.25)$$

The second subregion covers the range of $\frac{\pi}{3} \leq M_i^* \leq \frac{\pi}{\sqrt{3}}$ and the modulation index formula of this region is as follows.

$$M_i = 1 + (\frac{1}{2} - \frac{\sqrt{3}}{\pi})M_i^* \quad (4.26)$$

The third and last region covers the range of $\frac{\pi}{\sqrt{3}} \leq M_i^* \leq \infty$ and in this region the following modulation index relations are valid.

$$M_i = -1 + 2\cos\beta + (\frac{1}{2} - \frac{3\beta}{\pi} - \frac{\sqrt{3}}{2\pi})M_i^* + \frac{\sqrt{3}}{\pi}M_i^* \sin(2\beta - \frac{\pi}{6}) \quad (4.27)$$

$$\beta = \frac{\pi}{6} - \arcsin(\frac{\pi}{2\sqrt{3}M_i^*}) \quad (4.28)$$

Evaluating the above formula for $M_i^* \to \infty$ the modulation index of $M_i = \sqrt{3} - 1 \approx 0.732$ is found. This result indicates DPWM3 has an unusual over-modulation behavior. In the third region, as the reference modulation index increases, the fundamental component signal magnitude decreases. Unlike all the other modulators, which experience saturation, this modulator generates a reduced output voltage and exacerbates the drive performance.

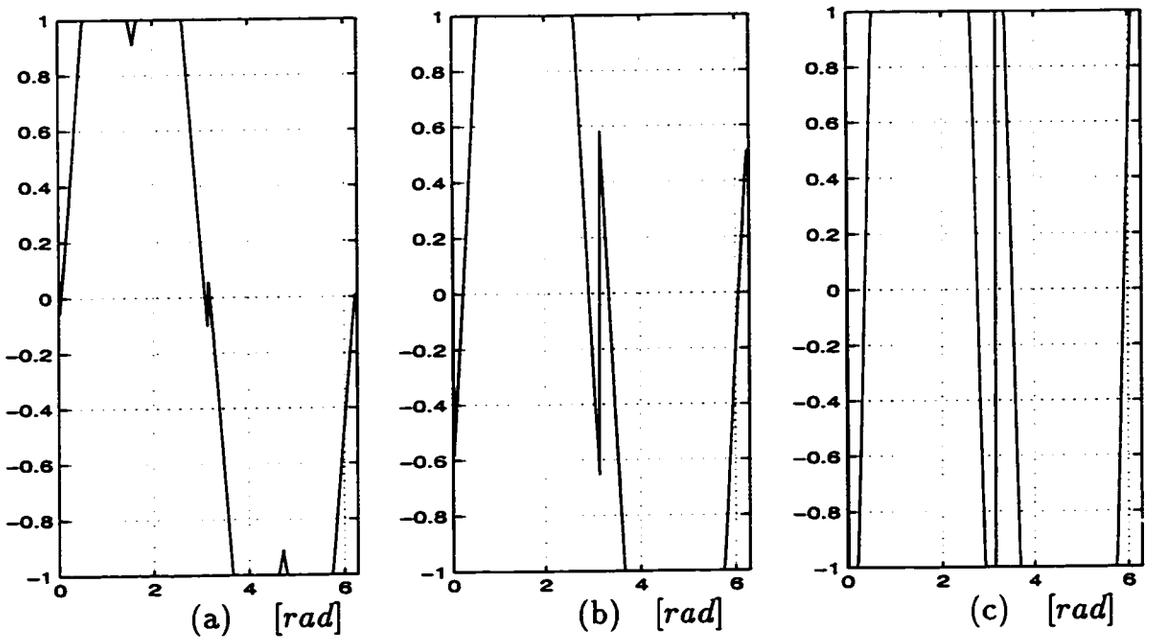

Figure 4.8: DPWM3 method overmodulation waveforms for three M_i^* values. (a): Region I ($M_i^* = 1.0$), (b): Region II ($M_i^* = 1.5$), (c): Region III ($M_i^* = 3.0$).

As illustrated in Fig. 4.8(c), in the third overmodulation region, this modulator generates voltage pulses with opposite polarity to the fundamental component, therefore the output voltage becomes smaller. As the reference signal becomes large, the opposite polarity pulses become rectangles with 30° width.

4.2.8 GDPWM

Since GDPWM covers the DPWM0, DPWM1 and DPWM2 modulators, its fundamental component overmodulation gain model has been developed in the previous subsections at least for these operating points. The following sections will illustrate except for these operating points, the remaining ψ range

of GDPWM does not have practical importance from the overmodulation perspective. Since a generalized fundamental component gain formula of GDPWM would be substantially complex and it has no practical value, its derivation will not be pursued in this work.

4.2.9 DPWMMAX and DPWMMIN

Since these modulators have a zero sequence signal with DC bias, in the overmodulation region, the output voltage contains a DC average voltage output. Therefore, the overmodulation region operation of these modulators is prohibitive and their waveform analysis will not be pursued in this work.

4.3 On The Gain Formula Accuracy

Obvious from the above analyses, the gain function calculation involves continuous or piece-wise continuous modulation signals, as opposed to the actual PWM inverter output voltages consisting of high frequency rectangular pulses. Theoretically, a modulator could match the reference volt-seconds within every carrier cycle and as a result the per-carrier-cycle-average-voltage could approach the theoretical modulation signals. Therefore, high fundamental component voltage gain accuracy is expected. However, at least in the regularly sampled asynchronous PWM, the discretized modulation signal may yield a slightly different volt-seconds than the original signal due to finite sampling

rate. Therefore, the theoretical gain formula can yield a slightly different fundamental component than the actual.

To test the accuracy of the Fourier analysis based fundamental component gain calculation method, the SVPWM method (the choice of SVPWM modulator was arbitrary) gain calculation was compared with simulation data. Employing the regularly sampled SVPWM modulator, an ideal PWM-VSI simulation was utilized to generate the pulsating inverter output voltage data. Evaluating the simulation data with a Fast Fourier Transformation (FFT) program, the fundamental component signal could be computed with high accuracy ($2^{13} = 8192$ data points). The fundamental frequency was selected as 50 Hz and the carrier frequency was varied from 1 to 5 kHz to investigate the influence of the sampling rate. The results are illustrated in Table 4.1 in terms of modulation indices. Based on the table data, the relative error was calculated for all the data and it was found to be less than 0.5 % and higher carrier frequencies implied significantly better accuracy.

The above results indicate for $\frac{f_s}{f_c} > 20$, the relative gain error is less than 0.5 % and the error significantly decreases with increasing $\frac{f_s}{f_c}$. Since the widely utilized PWM-VSI drives employing Insulated Gate Bipolar Transistor (IGBT) devices typically have high $\frac{f_s}{f_c}$ values, the model successfully represents most inverter drives.

Table 4.1: SVPWM theoretical and simulation based $M_i = f(M_i^*)$ data

M_i^*	M_i^t	$M_i(5kHz)$	$M_i(2kHz)$	$M_i(1kHz)$
0.907	0.907	0.907	0.907	0.907
0.950	0.934	0.934	0.933	0.933
1.0	0.949	0.949	0.948	0.946
2.0	0.989	0.988	0.987	0.984
4.0	0.997	0.997	0.996	0.993

4.4 Voltage Gain Comparisons

In this section the voltage gain characteristics of all the discussed modulators are comparatively evaluated. The comparisons are provided in terms of the voltage gain ($G = f(M_i)$) and modulation index ($M_i = f(M_i^*)$) relations. Utilizing the gain functions derived in the previous section, the gain characteristics of the modern modulators are computed and illustrated in Fig. 4.9. The improvement in the linearity range of all the zero sequence injection methods compared to SPWM is obvious from the figure. More importantly, the graph reveals the superior gain characteristic of Depenbrock's DPWM1 method; the gain of this modulator drops at a significantly smaller rate than all the other modulators, and the minimum value, which occurs at the six-step operating point is $\frac{\sqrt{3}}{\pi} \approx$ 0.551. All the other modulators have a rapid drop in gain and eventually the gain becomes practically zero at the six-step operating point. With the exception of DPWM3, the similarity of their gain characteristics with respect to each other is also obvious from the figure.

With its most unusual and poorest gain characteristic, the DPWM3 method would perhaps be mainly of academic interest. Unlike all the other modulators, which experience saturation, this modulator generates a substantially reduced output voltage and exacerbates the drive performance. Since in the overmodulation region the voltage pulse pattern of this modulator does contradict the pulse polarity consistency principle, its performance is unacceptable. In particular, its application to closed loop speed regulated voltage feedforward drives is prohibitive. Therefore, no further investigation on this modulator has been attempted.

Shown in Fig. 4.10 and illustrated in terms of the modulation indices, the input-output voltage relations of the important modulators provide more specific information. Except for DPWM1, all the modulators require large reference signals in order to penetrate the overmodulation region. In particular, DPWM1 requires a reference signal with a magnitude of $M_i^* = \frac{\pi}{\sqrt{3}} \approx 1.81$, while the other modulators require signals with very large magnitudes ($M_i^* \approx 5...20$). This result is extremely important from an implementation perspective: the smaller the gain range, the better the accuracy of the modulation signal and the smaller word length requirement of a signal processor(or the signal range in an analog implementation). Therefore, DPWM1 utilizes the signal range of a processor with high resolution and abrupt pulse dropping and the consequent overcurrent fault condition is avoided.

The unusual gain characteristic of DPWM1 is not difficult to explain. In the

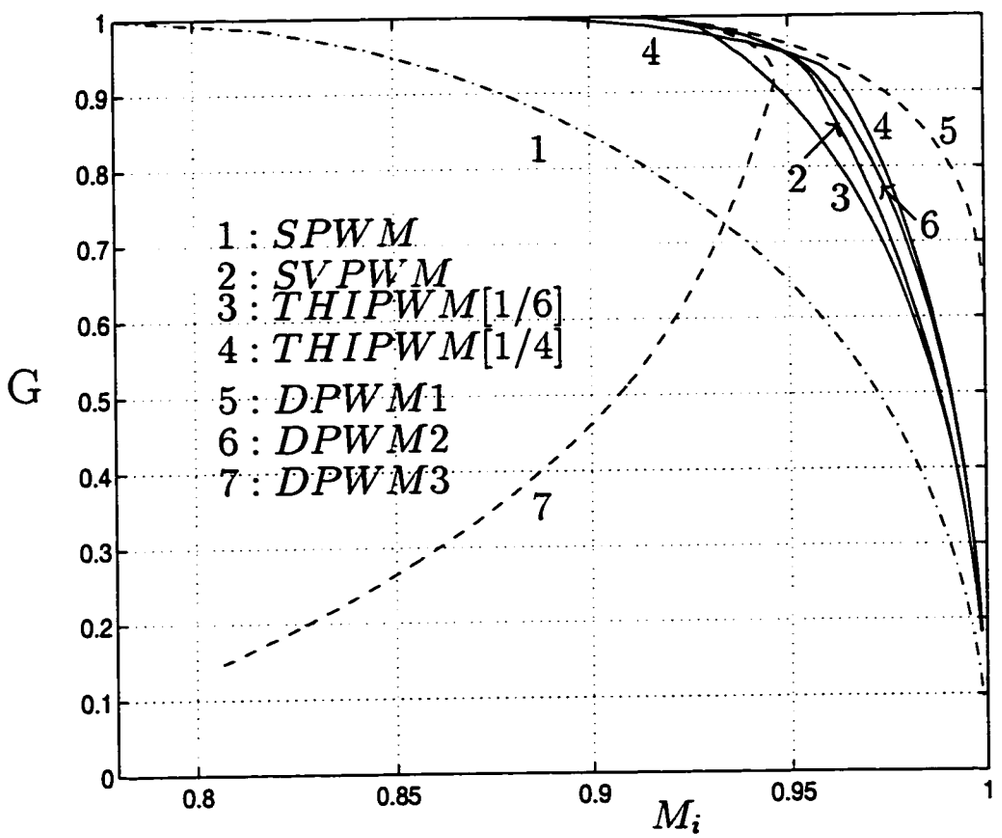

Figure 4.9: $G = f(M_i)$ voltage gain characteristics of the popular modulators.

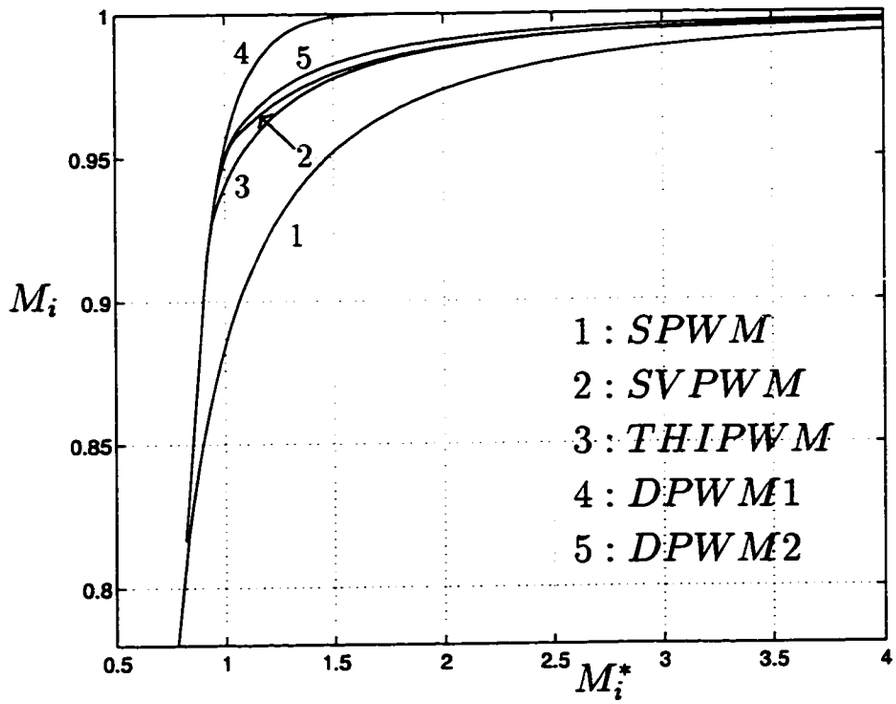

Figure 4.10: Overmodulation region $M_i = f(M_i^*)$ characteristics.

overmodulation range, the zero sequence signal of this modulator is effectively a square-wave function with an increasing magnitude as the six-step operating point is approached. Therefore, in this method, the modulation wave is vertically and horizontally forced to approach the six-step mode, while the other zero sequence injection methods force the modulation wave to expand mainly horizontally until the six-step mode is generated. This characteristic of DPWM1 can be clearly observed in Fig. 4.11 where DPWM1 and SVPWM modulation waveforms are compared for a set of reference modulation index values. It is apparent that as the reference modulation index increases, the SVPWM modulation wave saturates heavily, while the DPWM1 modulation wave easily approaches the square-wave.

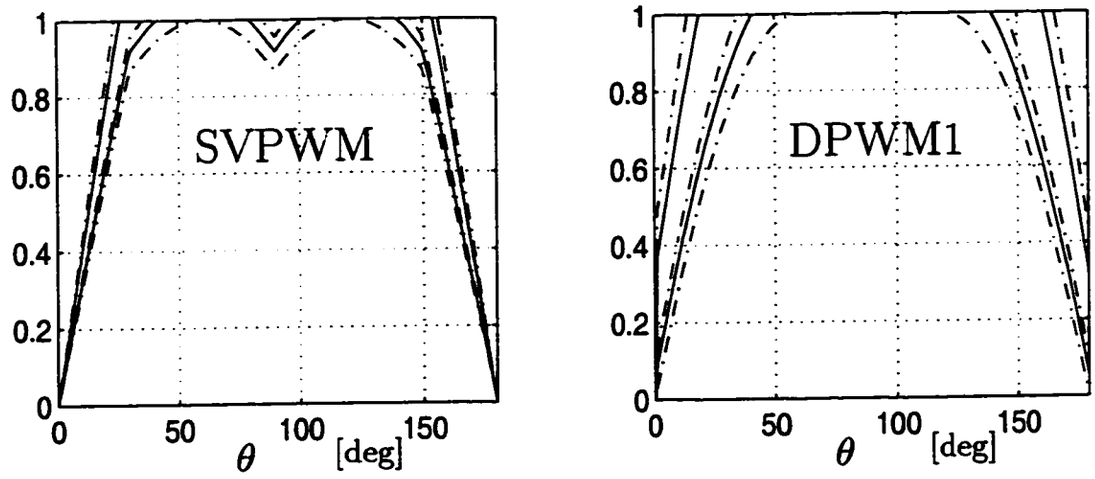

Figure 4.11: Overmodulation region modulation wave profiles of SVPWM and DPWM1 for five different M_i^* values.

4.5 Influence Of Blanking Time And Minimum Pulse Width On Modulator Gain

The inverter voltage linearity section of the previous chapter provided a short introduction to the influence of the inverter non-ideal characteristics (such as the minimum pulse width and the inverter blanking time) on the modulator voltage gain behavior. This section provides a more detailed investigation of these characteristics.

Inverter blanking time is the time interval that both switches of an inverter leg are open following a change in the gate logic reference signal value. It is provided for protection against DC bus short circuit. As shown in Fig. 4.12(b), the blanking time controller delays the reference gate signals by the blanking time t_d, and results in loss of gate signal symmetry (increases the uncharacteristic

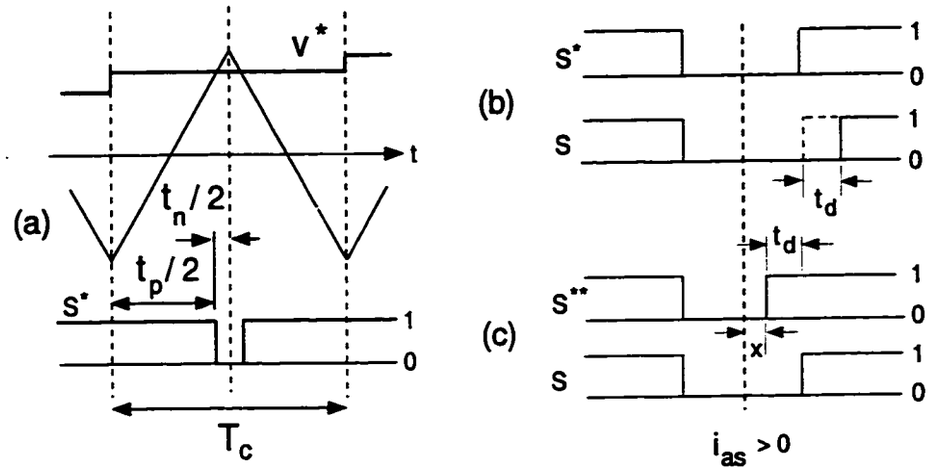

Figure 4.12: Regular sampling PWM reference and gate signals. (a): The reference gate signal at high modulation level, (b): No compensation results in asymmetric gate signal (for $i_{as} > 0$), (c): Signal after exact compensation.

harmonics), and also a reduction in the output voltage value. Typically, a gate pulse correction (compensation) algorithm is employed in order to restore the symmetry and volt-second balance [117]. As shown in Fig. 4.12 (c), in the exact compensation method, if the polarity of the phase current of the corresponding inverter leg is positive (negative), the reference gate signal on the triangle side with negative(positive) slope is advanced (delayed) by the blanking time leading to the correct output voltage pulse.

When a modulator operates near its theoretical linearity limits, as shown in Fig. 4.12 (a), narrow gate pulses are generated. When the width of such pulses becomes smaller than $2t_d$ (t_d is the blanking time), the compensation algorithm fails to correct the pulses properly. In Fig. 4.12 (c), this condition corresponds to $x \leq 0$ and correct compensation requires interference with the

modulation signal in the previous half carrier cycle. Since in the conventional digital PWM methods the reference modulation signal is generated only at the positive and/or negative peak points of the triangular carrier wave (regular sampling), correct compensation of such a narrow pulse is not possible. Hence, voltage gain reduction occurs before the theoretical linearity limit. The lowest modulation level at which this problem occurs can be easily calculated. When the modulation signal v^* is positive, the narrow pulse occurs when in the upper inverter leg switch is the off state with a duration t_n^* calculated as follows.

$$t_n^* = (\frac{T_s}{2})(1 - \frac{v^*}{\frac{V_{dc}}{2}}) \tag{4.29}$$

Substituting the modulation wave peak value of the modulator under investigation in the above formula and selecting the minimum pulse width equal to $2t_d$, the practical maximum linear modulation index M_{Lmax}^p can be found as follows.

$$M_{Lmax}^p = (1 - k_m \frac{2t_d}{T_s}) * M_{Lmax}^t \tag{4.30}$$

In the above formula, M_{Lmax}^t is the theoretical linearity limit of the modulator. The k_m coefficient distinguishes the discontinuous PWM methods from the continuous wave modulation methods. Its value is $k_m = 1$ for the DPWM methods and $k_m = 2$ for the modulators with continuous modulation wave. Note the above equation and (3.54) are derived with the same approach and replacing

$2t_d$ with t_{MPW} yields equal results. As discussed in the previous chapter, the small k_m coefficient of the DPWM methods indicates that DPWM methods have wider voltage linearity range than SPWM, SVPWM, and other CPWM methods. This result is a consequence of the different distribution of the inverter zero states in the two different modulation groups. The discontinuous PWM methods generate only one inverter zero state per carrier cycle (t_0: all the lower inverter switches are in the on-state or t_7: all the upper switches are in the on-state), while the continuous PWM methods generate two zero states (for SVPWM $t_0 = t_7$). Since the total zero state time is not a function of the zero sequence signal but the line-line reference voltage, for the same line-line output voltage and carrier frequency value, the gate pulses of the DPWM methods are wider than the gate pulses of the CPWM methods. Therefore, the narrow pulse problem occurs at a higher modulation index with DPWM methods than CPWM methods.

Notice that in both continuous and discontinuous PWM cases, the linearity boundaries depend on the ratio of the blanking time to the carrier cycle. Since the increasing carrier cycle practically implies increasing inverter power and increasing blanking time, the ratio is at least a few percent in most PWM-VSI drives. As a result, in most applications the linearity range of a modulator is reduced by a substantial amount. In either modulation method, once beyond the boundary of linear modulation range, the output voltage is reduced by an amount which depends on the overlap time "x" shown in Fig. 4.12 (c). As a result, the gain begins to decrease at a lower modulation index than the

theoretical linearity limit and decreases more rapidly than the theoretical gain characteristic. Compared to the modulator theoretical gain reduction, the gain reduction of the DPWM methods due to the blanking time is fairly small, and can be ignored for inverters with a few kHz switching frequency and blanking time less than a few microseconds. In the Gate Turn Off (GTO) switching device based PWM-VSI applications, the effect is more emphasized due to the long blanking time.

In certain applications, the narrow voltage pulses which occur at high modulation levels may damage the drive or load. In such cases the blanking time correction algorithm yields to a Minimum Pulse Width (MPW) control algorithm. For example, the turn-on and/or turn-off speed capabilities of a GTO may not be sufficient to generate such narrow pulses. In order to avoid commutation failure of GTO based drives, such narrow pulses are either eliminated or fixed at an acceptable level.

Narrow voltage pulses can also cause overvoltage related motor insulation failure. State of the art PWM-VSI drives utilize the modern third generation IGBT devices with very small turn-on and turn-off times. Feeding motors with long cables from such PWM-VSI drives, significant overvoltages are generated across the motor terminals due to voltage reflection. As a result, the motor terminals experience excessive overvoltages contributing to insulation failure. When such PWM-VSI drives operate at high modulation levels and narrow

pulses are generated, the voltage reflection problem is exacerbated: overvoltages in excess of twice the DC bus value can appear across the terminals of a motor connected to a drive through as short a cable as 30 m [92]. Therefore, narrow voltage pulses are problematic in many drives. These problems can be eliminated by either employing passive solutions such as inserting reactors between the drive and the motor, or active solutions such as MPW control which only requires modification to the PWM algorithm of a drive. The active solution is more economic, compact and maintenance free.

When employed, MPW control algorithms affect the modulator voltage gain and reduce the linear modulation range noticeably. The Pulse Elimination Method (PEM) omits pulses narrower than a desirable limit and increases the modulator gain. The Pulse Limiting Method (PLM) limits the width of the pulses to the minimum allowable pulse width limit and reduces the gain. However, as the modulation index increases, the modulator theoretical gain characteristics dominate and in both cases the gain decreases rapidly, therefore the gain curves follow the gain curves of Fig. 4.9 closely. In either method, the linearity limit of a modulator becomes smaller than the theoretical limits. In a proper design, the MPW pulses are wider than $2t_d$; therefore, the blanking time controller has no influence on the modulator linearity in this case. When MPW is applied, the practical voltage linearity limit of an inverter can be found from (3.54). Since in this algorithm both sides of the triangle are affected while in the blanking time compensation case only one side of the triangle has incorrect

gate signal, the effect of MPW control has more influence on the gain characteristic of a PWM-VSI. In particular, in GTO based high power PWM-VSIs which employ GTO's with large MPW values ($t_{MPW} \approx 200\mu$s), MPW control starts at very low modulation depths, and the nonlinear gain characteristics dominate the drive behavior at a low modulation depth. Although less significant, the effect can not be underemphasized in the modern IGBT device based PWM-VSI drives. In order to avoid the above mentioned overvoltage problem, MPW times as large as 8-16 μs are required [92]. Since the carrier frequency is at least a few kilohertz, the influence of MPW control on the gain characteristics of such drives is significant.

The MPW controlled modulator gain formulas can be closed form calculated by modifying the theoretical modulator gain formulas. In a PEM controlled inverter, the output modulation index is different from the modulation index output by an amount the additional volt-seconds determine. Calculating the additional components by the Fourier analysis, the modified modulation index relations can be easily obtained. In the following the modified modulation index formulas of SPWM, SVPWM, and DPWM1 are summarized.

4.5.1 SPWM

When employing PEM, the modulation index relations of the SPWM method become as follows.

$$M'_{iSPWM} = M_i + \cos\alpha_{0s} - \cos\alpha_{1s} -$$
$$\frac{2M_i^*}{\pi}[\alpha_{1s} - \alpha_{0s} - \frac{1}{2}(\sin(2\alpha_{1s}) - \sin(2\alpha_{0s}))] \tag{4.31}$$

The α_{0s} and α_{1s} angles correspond to points PEM begins and ends. These angles are calculated as follows.

$$\alpha_{0s} = \arcsin(\frac{\pi}{4M_i^*}(1 - \frac{2t_{MPW}}{T_s})) \tag{4.32}$$

$$\alpha_{1s} = \arcsin(\frac{\pi}{4M_i^*}) \tag{4.33}$$

4.5.2 SVPWM

The SVPWM modulation index relations with PEM control are calculated in the following for three operating regions. In the first region, for $\frac{\pi}{2\sqrt{3}}(1 - 2\frac{t_{MPW}}{T_s}) \leq M_i^* \leq \frac{\pi}{2\sqrt{3}}$ the following relations yield.

$$M'_{iSVPWM} = M_i^* + \cos\alpha_{1sv1} - \cos(\frac{2\pi}{3} - \alpha_{1sv1}) -$$
$$\frac{\sqrt{3}M_i^*}{2\pi}[\sqrt{3}(\frac{2\pi}{3} - 2\alpha_{1sv1}) + \sin(2\alpha_{1sv1} + \frac{\pi}{6}) + \cos(2\alpha_{1sv1})] \tag{4.34}$$

$$\alpha_{1sv1} = -\frac{\pi}{6} + \arcsin(\frac{\pi}{2\sqrt{3}M_i^*}(1 - \frac{2t_{MPW}}{T_s})) \tag{4.35}$$

The second region involves a reference modulation index range of $\frac{\pi}{2\sqrt{3}} \leq M_i^* \leq \frac{\pi}{3}$ and in this region the modulation index relations are as follows.

$$M'_{iSVPWM} = M_i + \cos\alpha_{1sv2} + \cos\alpha_{3sv2} - \cos\alpha_{2sv2} - \cos\alpha_{4sv2} + \frac{3M_i^*}{2\pi}(\alpha_{1sv2} + \alpha_{3sv2} - \cos\alpha_{2sv2} - \cos\alpha_{4sv2}) + \frac{\sqrt{3}M_i^*}{2\pi}[\sin(2\alpha_{2sv2} + \frac{\pi}{6}) + \sin(2\alpha_{4sv2} + \frac{\pi}{6}) - \sin(2\alpha_{1sv2} + \frac{\pi}{6}) - \sin(2\alpha_{m3sv2} + \frac{\pi}{6})] \quad (4.36)$$

$$\alpha_{1sv2} = -\frac{\pi}{6} + \arcsin(\frac{\pi}{2\sqrt{3}M_i^*}(1 - \frac{2t_{MPW}}{T_s})) \quad (4.37)$$

$$\alpha_{2sv2} = -\frac{\pi}{6} + \arcsin(\frac{\pi}{2\sqrt{3}M_i^*}) \quad (4.38)$$

$$\alpha_{3sv2} = \frac{2\pi}{3} - \alpha_{2sv2} \quad (4.39)$$

$$\alpha_{4sv2} = \frac{2\pi}{3} - \alpha_{1sv2} \quad (4.40)$$

The third region involves the remainder of the reference modulation index range ($M_i^* \geq \frac{\pi}{3}$) and in this region the modulation index relations are as follows.

$$M'_{iSVPWM1} = M_i + \cos\alpha_{0sv3} - \cos\alpha_{1sv3} - \frac{3M_i^*}{\pi}[\alpha_{1sv3} - \alpha_{0sv3} - \frac{1}{2}(\sin(2\alpha_{1sv3}) - \sin(2\alpha_{0sv3}))] \quad (4.41)$$

$$\alpha_{0sv3} = \arcsin\left(\frac{\pi}{6M_i^*}\left(1 - \frac{2t_{MPW}}{T_s}\right)\right) \tag{4.42}$$

$$\alpha_{1sv3} = \arcsin\left(\frac{\pi}{6M_i^*}\right) \tag{4.43}$$

4.5.3 DPWM1

When employing PEM, the modulation index relations of the DPWM1 method become as follows.

$$M'_{iDPWM1} = M_i + 2(\cos\alpha_{d0} - \cos\alpha_{d1}-) - M_i^*\frac{3}{\pi}(\alpha_{d1} - \alpha_{d0}) + M_i^*\frac{\sqrt{3}}{\pi}(\sin(2\alpha_{d1} + \frac{\pi}{6}) - \sin(2\alpha_{d0} + \frac{\pi}{6})) \tag{4.44}$$

In the above equation, M'_i is the output voltage modulation index and M_i is the theoretical modulation index value without MPW control which is given by (4.16). The intermediate variables α_{d0} and α_{d1} are calculated as follows.

$$\alpha_{d0} = -\frac{\pi}{6} + \arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\left(1 - \frac{t_{MPW}}{T_s}\right)\right) \tag{4.45}$$

$$\alpha_{d1} = -\frac{\pi}{6} + \arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\right) \tag{4.46}$$

4.5.4 Evaluation and Comparison

Figure 4.13 shows the closed form calculated gain characteristics of PEM controlled PWM-VSI for both SVPWM and DPWM1. Both modulators employ $f_s = 5kHz$ and $t_{MPW} = 12\mu s$. As the figure illustrates, the influence of the MPW algorithm has a non-negligible effect on the voltage gain of SVPWM. The nonlinearity is noticeably smaller in the DPWM1 case. On the same figure, the blanking time dependent gain characteristic of DPWM1 is shown for $t_d = 4\mu$s. Notice the blanking time has very little influence on the linearity compared to MPW. The gain curves of the PEM controlled drive clearly indicate the linearity range of DPWM methods is significantly wider than SVPWM and in the overmodulation region DPWM1 is the only modulator that maintains a high gain. Therefore, DPWM1 can be most beneficial to high power PWM-VSI drives and all the PWM-VSI drives with large $\frac{t_{MPW}}{T_s}$ ratio while operating in the high modulation range.

4.6 Voltage Gain Linearization

As illustrated in Fig. 4.14 (a) in block diagram form, in the overmodulation region the VSI output voltage is different from the reference voltage due to gain nonlinearity. PWM-VSI drives which employ PLM and drives which do not employ any MPW control algorithm always experience gain reduction, while those employing PEM experience gain increase in the entrance of the overmodulation

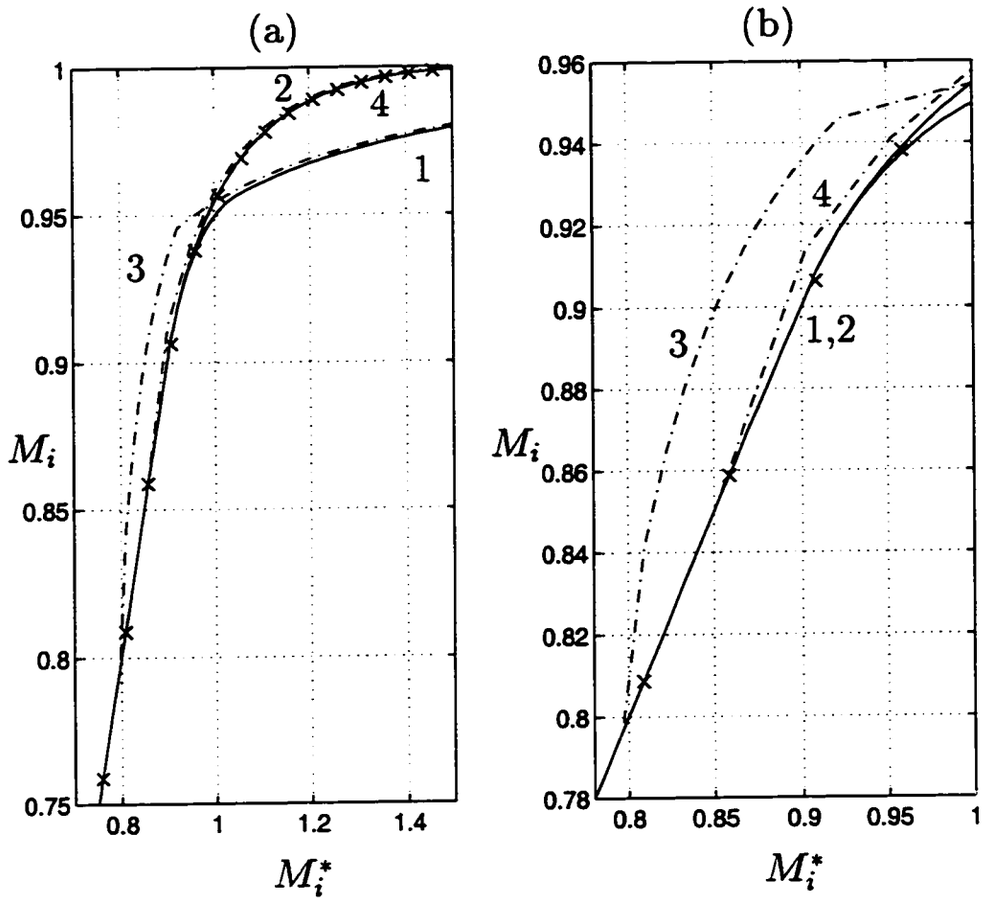

Figure 4.13: SVPWM and DPWM1 theoretical $M_i = f(M_i^*)$ characteristics (a), and the magnified view in the low end of the overmodulation region (b). 1: SVPWM, 2: DPWM1, 3: SVPWM with MPW, and 4: DPWM1 with MPW. The blanking time dependent nonlinearity of DPWM1 is shown with the "×" symbol.

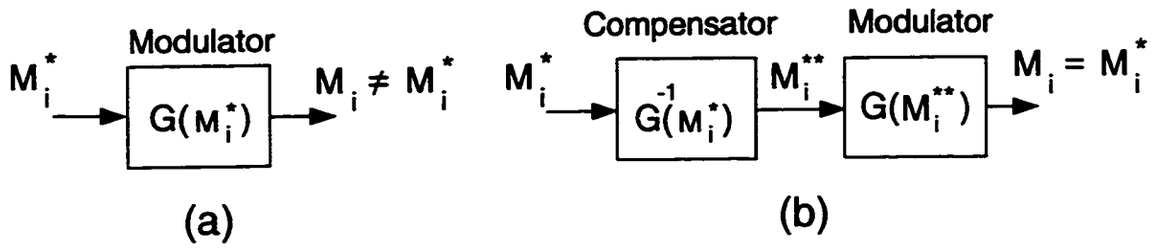

Figure 4.14: Overmodulation range voltage gain block diagrams. (a): Modulator nonlinear gain characteristic. (b): The compensator cancels the nonlinearity by inverse gain multiplication.

region and gain reduction as the overmodulation region is further penetrated. On the other hand, it is important to program the reference fundamental component voltage value correctly so that the drive performance does not degrade. For example, in AC motor drive applications the stator flux value (or equivalently the $\frac{V}{f}$ value) must be maintained at a proper level to obtain high efficiency. Therefore, fundamental component voltage linearity must be retained in the overmodulation range also. Since the discussed modulation methods have nonlinear gain characteristics, to retain voltage linearity a gain compensation technique must be employed. Gain compensation techniques are based on either adding extra signals such as square-waves to the reference modulation waves, or by increasing or decreasing the fundamental component magnitude of the reference modulation waves [93]. As shown in Fig. 4.14 (b), in the latter approach the reference modulation wave fundamental component signal is pre-multiplied with the inverse gain function such that the nonlinearity is canceled. The former approach may alter the modulator harmonic characteristics while the latter does not. In this work, the inverse gain method will be investigated.

In both gain linearization methods, calculating the gain compensation function is very difficult. The difficulty of describing the gain functions in closed form equations has been overcome in the early stages of this paper. However, closed form calculation of the inverse gain function is very difficult. Furthermore, on-line computation of such complex gain compensation signals with the state of the art DSP or μP devices is prohibitive. Instead, the gain function and its inverse can be numerically computed off-line and the data can be utilized to approximate the gain compensation function by a look-up table and/or a simple curve fitting method.

Inverse gain compensation based gain linearization of the SPWM method which employs a table look-up approach was previously reported, and the requirement for a large table size and an efficient table search algorithm were indicated [93]. The zero sequence injection PWM methods which are discussed in this paper have smaller gain range than SPWM, therefore the memory requirements are less demanding. However, of all the discussed methods, DPWM1 provides an exceptional implementation advantage due to its significantly small gain reduction. The gain compensation signal (inverse gain function magnitude) of DPWM1 is less than 2 units while the other modulators require large signals ranging from 5 to 20 units. Therefore, when employing DPWM1 in a fixed-point digital platform, the word length of the μP or DSP can be more efficiently utilized. The other methods require a significant amount of data shifting to process the large inverse gain values such that overflow does not

occur and this results in poor modulation signal resolution and increased computation time. The inverse gain function data of DPWM1 can be easily fit into several first order polynomials leading to a smaller memory size requirement and improved accuracy. Near the six-step operating point ($M_i \geq 0.99$) the gain inverse coefficients increase due to the rapid gain reduction and the inverse gain function can be better modeled by several data entries.

Employing the analytical gain function of DPWM1 and accounting for PEM based nonlinearity, the inverse gain function data can be accurately and easily computed from (4.44). Utilizing this data to obtain a simple hybrid model consisting of several piece-wise first order polynomial functions and several data entries is a straightforward task.

Compared to the direct digital PWM implementation, the triangle intersection technique requires simpler overmodulation algorithms. In the direct digital method, the overmodulation condition is detected only after computing a zero state time length with negative sign. Therefore, a back step for correcting the sign is inevitable, and additional algorithms (often complex) must be employed to compensate for the gain loss [75]. Therefore, DPWM1 triangle intersection method requires the simplest overmodulation algorithm and has superior performance when compared to all the other PWM methods reported.

4.7 Waveform Quality

As discussed in the previous chapter in detail, the linear modulation range harmonics of carrier based PWM methods (characteristic harmonics) are concentrated at the carrier frequency, its multiples and their sidebands. These harmonics could be successfully modeled with the HDF function. The analysis and comparison aided understanding the characteristics of all the modern modulators. It was illustrated that CPWM methods have superior waveform quality in the lower linear modulation index region while the DPWM methods would perform better in the higher linear modulation index region. Therefore, it was concluded a modulation algorithm that selects SPWM or SVPWM in the lower linear modulation region and a suitable DPWM method in the remainder of the linear modulation region would yield an optimal drive performance. However, the overmodulation region waveform quality was not considered. In this section the overmodulation region waveform quality will be investigated.

In the overmodulation region, as the unmodulated portions of the modulation waves increase the characteristic harmonics decrease. Therefore, the high frequency harmonic content becomes less significant with increasing modulation index and eventually becomes zero at the six-step operating point. However, large amount of sub-carrier frequency harmonics (5th, 7th, etc.) are generated and as the six-step mode is approached these harmonics become increasingly dominant in determining the waveform quality. Since the overmodulation region implies loss of volt-second balance, in the carrier cycles that saturation occurs

the HDF formula is not applicable. Therefore, it is difficult to analytically model the overmodulation region waveform characteristics of a modulator and a numerical approach is more suitable. Defined in the following, the inverter output line to line voltage Weighted Total Harmonic Distortion (WTHD) factor is an appropriate measure in determining the modulator waveform quality both in the linear and overmodulation range.

$$WTHD = 100 \times \frac{\sqrt{\sum_{i=2}^{n}(\frac{V_{LLi}}{i})^2}}{V_{LL1}} \tag{4.47}$$

In most AC motor drive and utility interface applications, the WTHD function is more meaningful than the conventional voltage THD definition in which the $\frac{1}{i}$ weight factor is absent in the formula because the WTHD function accounts for the low pass filter characteristic of the load inductance automatically. Thus, a better measure for the current harmonic distortion. The WTHD function is carrier frequency dependent and the V_{LLi} terms are typically calculated by evaluating the PWM-VSI line to line output voltage data for one fundamental cycle (obtained by simulation) through FFT analysis.

In this study, line to line voltage WTHD curves for SVPWM and DPWM1 are calculated and compared. The inverter line to line voltage data of a PWM-VSI drive which employs the once per carrier regular sampling technique is generated by means of computer simulations. The simulation assumes a fundamental frequency of $f_e = 60$ Hz. The carrier frequency f_s is 5 kHz in the DPWM1 case and 3.33 kHz in the SVPWM case. This implies equal inverter

average switching frequency in both methods. In order to illustrate the carrier frequency dependency of the WTHD function, the SVPWM case is evaluated for 5 kHz also. The harmonic voltages, accounting for all the dominant harmonics (up to $3f_s$), were calculated by evaluating the 8192 data points by means of an FFT algorithm of the MATLAB [1] numerical computation software package.

The WTHD curves in Fig. 4.15 (a) illustrate the advantageous waveform characteristics of the DPWM1 method at high modulation including the over-modulation range. Under the equal inverter average switching frequency criteria, the harmonic distortion of DPWM1 is less than the SVPWM methods from $M_i \approx 0.6$ to $M_i \approx 0.95$ where both curves merge. Under an equal carrier frequency criteria, which implies a 50 % increase in the average switching frequency in the SVPWM case, the waveform quality advantage of SVPWM over DPWM1 is lost near $M_i \approx 0.90$.

Although they have different shapes and definitions, the HDF and WTHD performance indices yield similar conclusions in the linear modulation region. Since in the lower modulation index region the line to line voltage pulses become narrow, the 8192 data FFT analysis yields a result with limited accuracy while the HDF approach is exact and yields a higher accuracy waveform quality calculation. Also it should be kept in mind these approaches are difficult to mathematically relate and they should be independently utilized as required by the application.

The blanking time and minimum-pulse-width control algorithm dependent

inverter nonlinearities can cause significant harmonic distortion increase which is modulator dependent. Figure 4.15 (b) illustrates the increase in the harmonic distortion when a $12\mu s$ MPW control algorithm (PEM) is employed in the above system. Although the harmonic distortion increases in all the cases, the relative increase in the DPWM1 case is significantly smaller than the SVPWMs. The data clearly indicates that the harmonic distortion of the SVPWM method significantly increases and the increase in the switching frequency worsens the harmonic distortion. Therefore, accounting for the MPW nonlinearity, the superiority of DPWM1 over SVPWM begins at a significantly smaller modulation index value than the ideal case. Figure 4.15 (b) clearly indicates that if the carrier frequency is kept constant and the modulation method is switched from SVPWM to DPWM1 beyond $M_i \approx 0.8$, no degradation of waveform quality will be obtained relative to the SVPWM case. Furthermore, in the DPWM1 case the switching losses are greatly reduced.

Figure 4.15 also indicates the overmodulation region waveform characteristics of DPWM1 are superior to SVPWM until the point where the 5th, 7th, etc. sub-carrier frequency harmonics totally dominate and both WTHD curves merge ($M_i \approx 0.95$). Although in the low end of the overmodulation range the WTHD factor is strongly dependent on the carrier frequency, inverter nonlinearities and the modulation method, in the high end it is dominated by the sub-carrier frequency harmonics and it is weakly dependent on the carrier frequency and the modulation method. Therefore, a detailed investigation of the sub-carrier frequency harmonic characteristics is required.

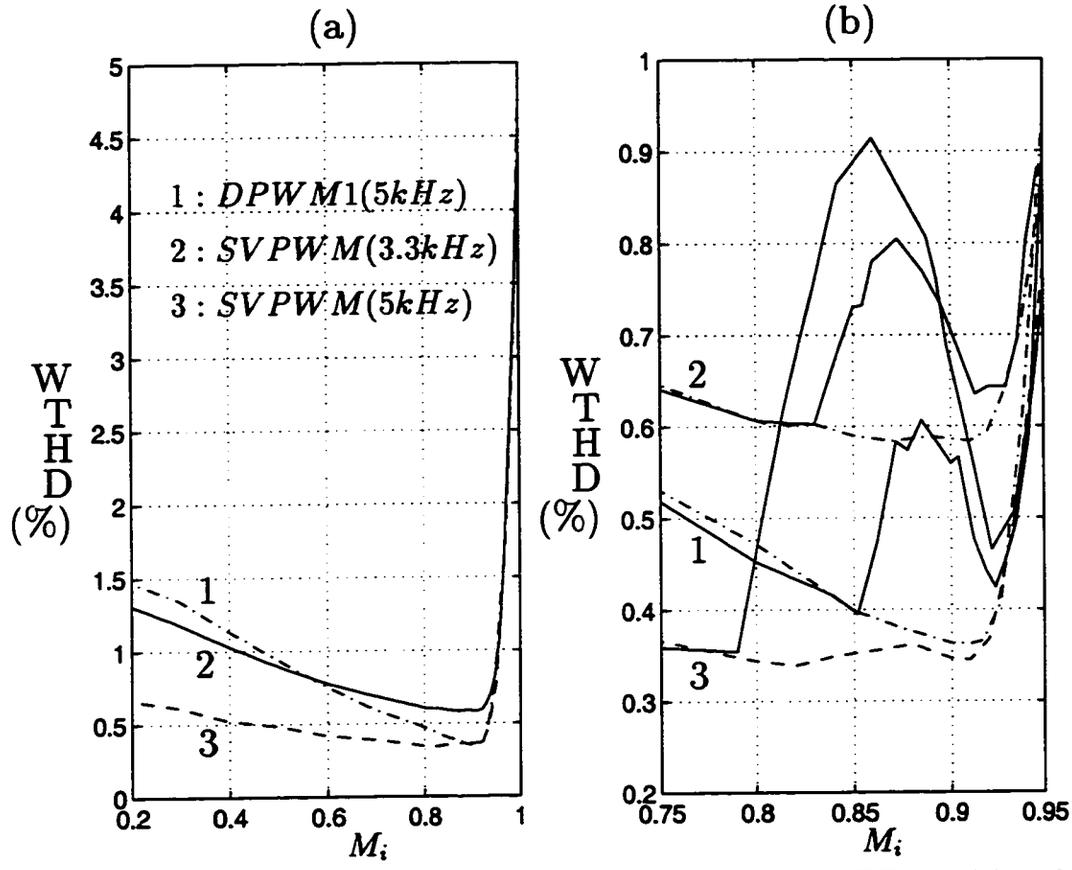

Figure 4.15: WTHD characteristics of SVPWM and DPWM1. (a): Ideal inverter model case. (b): Magnified view with MPW (solid) and without MPW (dashed) control algorithm.

4.7.1 Subcarrier Frequency Harmonic Content

Since each modulator has a unique modulation wave and in the overmodulation region unique modulation signals are generated, the sub-carrier frequency harmonic content of each modulator is unique. Since the modulation wave shape is independent of the carrier frequency, these harmonics are also independent of the carrier frequency. Although it is theoretically possible to closed form calculate these harmonics for each modulator, the process would be substantially difficult, laborious, and perhaps the detail unnecessary. Therefore, a numerical approach is more suitable to obtain the subharmonic data which is mainly required for the purpose of comparison between modulators.

For isolated neutral loads, the inverter output voltage subcarrier frequency harmonics which affect the drive performance are the non-triplen odd harmonics, i.e. 5th, 7th, etc. Since electric machines and utility interfaces with inductive interface filters have low pass filter characteristics, the high frequency inverter output voltage harmonics do not generate large currents, while small magnitudes of low frequence harmonics can generate large harmonic currents. As a result, the low frequency harmonics influence the drive characteristics at high modulation index values. They cause torque ripple and copper losses. Therefore, only the dominant low frequency harmonics need be considered.

In this study the overmodulation region inverter output voltage subcarrier frequency dominant harmonics are computed through FFT analysis of the modulation waves for various modulation index values. The 5th, 7th, 11th, 13th,

17th, 19th, 23th, and 25th harmonics are accounted for in this analysis. For each modulator and modulation index value, a full modulation wave fundamental cycle has been computed employing 2048 data points. Through FFT analysis of this data the harmonic components were calculated. Evaluating the individual harmonics, and excluding the triplen harmonics, the Total Harmonic Distortion (THD) (in (4.47), by replacing the $\frac{1}{i}$ term with unity, the THD formula yields) was computed and stored for each modulation index and each modulator. For each modulator, the overmodulation range data has been evaluated for 20 different modulation index values. The results provide accurate estimates of the subcarrier frequency harmonic content for systems with carrier frequency to fundamental frequency ratios of approximately 20 or higher. For low ratios, the results are rough approximates. As illustrated in the voltage gain accuracy study, this limitation is due to the fact the actual discretized modulation wave may be slightly different than the ideal modulation signal. Since the carrier waves and switchings are not modeled, the data does not contain information regarding the carrier frequency harmonics. In the higher end of the overmodulation range, the influence of the high frequency harmonics on the total THD is significantly smaller than the low frequency harmonics, hence these terms can be neglected.

The voltage sub-carrier frequency THD characteristics of SVPWM, SPWM, THIPWM1/6, and DPWM1 have been calculated and shown in Fig. 4.16 in detail. The figure indicates that there is no significant difference between the THD of the zero sequence signal injection PWM methods considered. However, it is

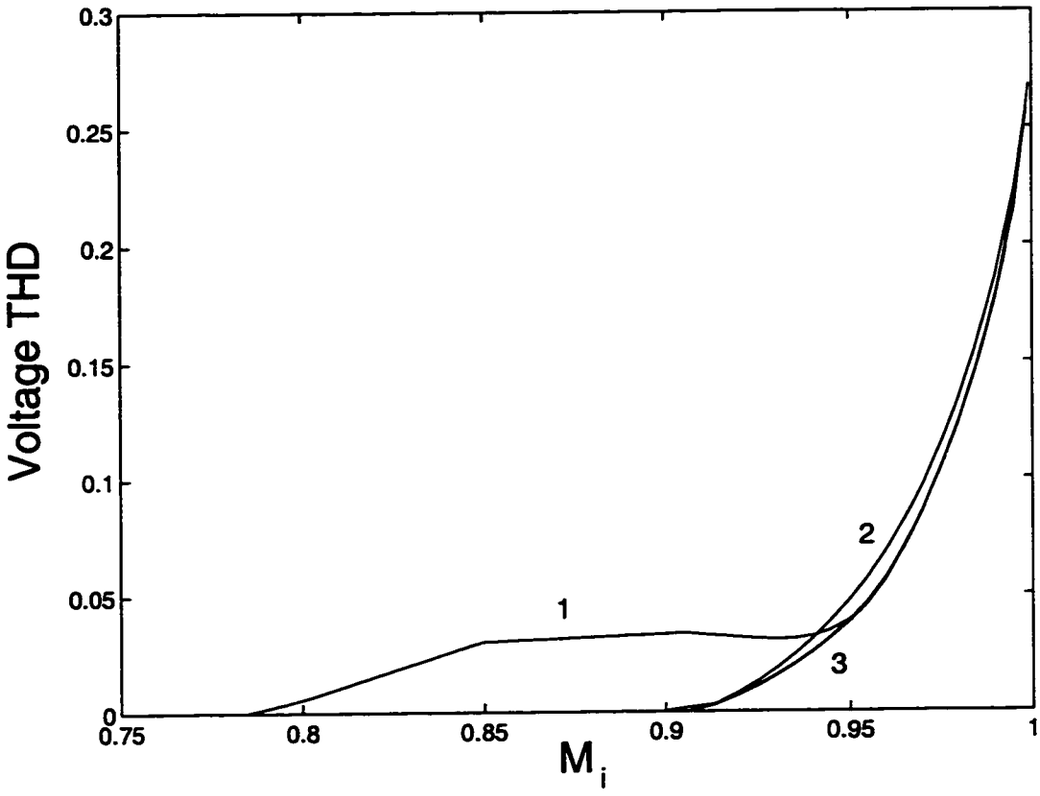

Figure 4.16: Ideal subcarrier frequency voltage THD of various modulators in the overmodulation range. 1: SPWM, 2:DPWM1, 3: SVPWM and THIPWM1/4.

visible from the curves that the SVPWM has slightly better THD characteristic. The SPWM method harmonic content has an interesting THD characteristic. As the modulator enters the overmodulation region the THD almost linearly increases, and at about 0.91 modulation index it saturates and furthermore it slightly decreases. As the modulation index further increases, the SPWM THD curve joins the other curves inclining towards the six step value.

Assuming that the AC load harmonic model can be represented by the load transient inductance, the current THD can be easily calculated from the voltage

harmonic data ($I_n = \frac{V_n}{nw_e L_\sigma}$). If harmonic currents are a cause of concern from the efficiency or torque ripple perspective, the allowed overmodulation range of a drive may be limited to a modulation range in which the performance is acceptable. The harmonic characteristics extracted in this section can be utilized for such purposes.

Although the total voltage THD is very close in all the modulators discussed, the individual harmonics of various modulators may differ more noticeably. Figure 4.17, Figure 4.18, and Figure 4.19 show the modulation index dependency of sub-carrier frequency voltage dominant harmonics of the SPWM, DPWM1, and SVPWM. The data was calculated in terms of harmonic modulation index variables for the sake of generality. The figures indicate that the most dominant harmonic is the fifth harmonic, and as the order increases the harmonic magnitudes decrease. The dominant harmonics do not have linear gain relations with the modulation index value, and as the modulation index increases, their magnitudes increase very steeply, in particular near six step modulation. This characteristic is common to all the modulators discussed. The six-step operating mode harmonic content is well defined and these harmonics are the non-triplen odd harmonics. Utilizing the Fourier analysis approach, the harmonic content of the six-step voltage waveforms can be calculated as follows.

$$V_n = \frac{2}{n\pi} V_{dc} \tag{4.48}$$

where

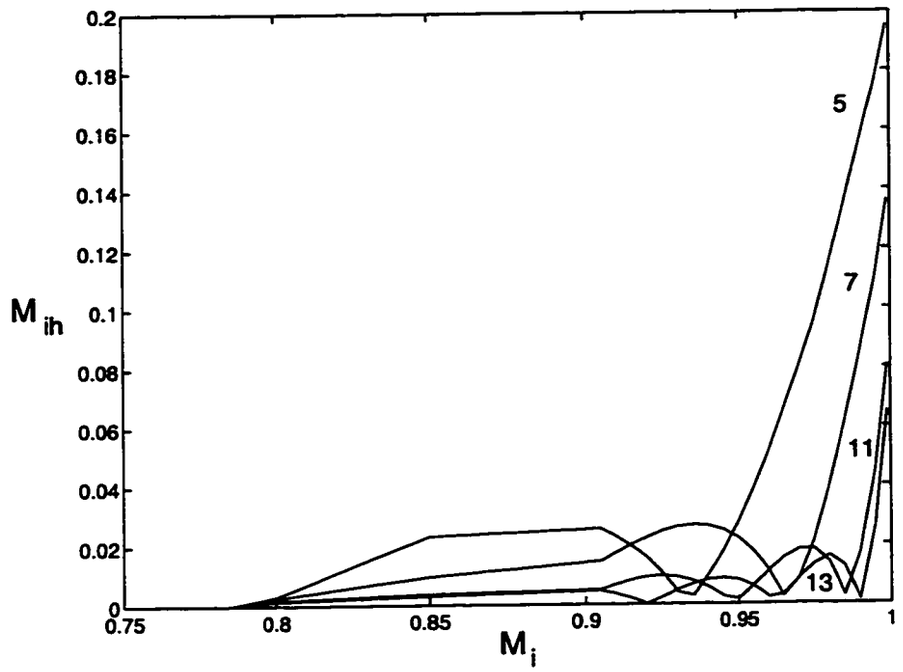

Figure 4.17: Individual voltage harmonic content of SPWM in the overmodulation range. The values are given in terms of the modulation index.

$$n = 6h \pm 1, h = 1, 2, 3, etc. \tag{4.49}$$

4.7.2 Evaluation and Comparison

Inverter output voltage waveform quality in the lower end of the overmodulation region is mainly determined by the carrier frequency harmonics, and a modulator with less distortion would provide the best results. Therefore, selecting a suitable DPWM method would yield a superior performance. In the higher end of the overmodulation region, the sub-carrier frequency harmonics dominate the performance. Although the sub-carrier frequency harmonic content of different modulators is different, practically the voltage THD is not modulator type

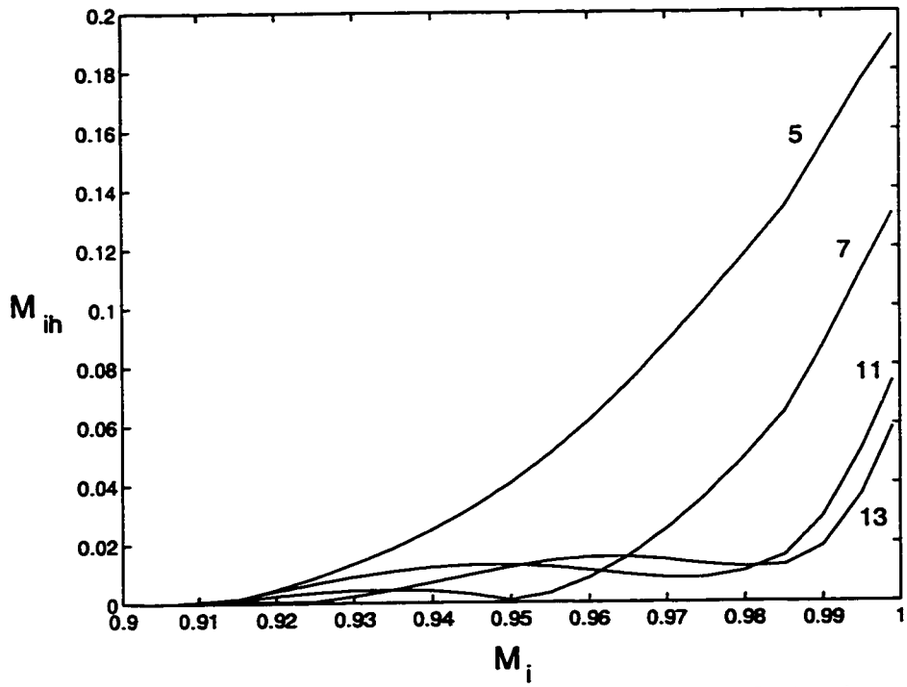

Figure 4.18: Individual voltage harmonic content of DPWM1 in the overmodulation range. The values are given in terms of the modulation index.

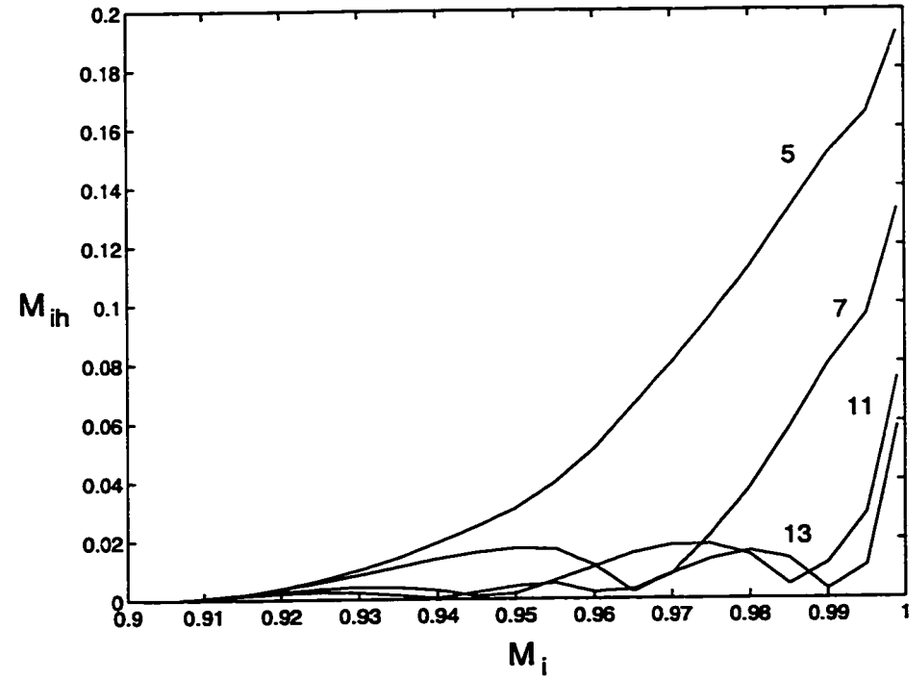

Figure 4.19: Individual voltage harmonic content of SVPWM in the overmodulation range. The values are given in terms of the modulation index.

dependent (except in comparison with SPWM which is considered a poor overmodulation method). Therefore, the choice of modulator in this region could be determined by other performance criteria such as voltage gain and switching losses. The modulation index value that the dominance of the carrier frequency harmonics ends and the sub-carrier frequency harmonics become dominant is approximately 0.95.

Since the harmonic current is approximately proportional to the inverse of the load transient impedance (at high frequencies mainly inductance), a load with large transient inductance experience less current ripple in the high overmodulation range than the low inductance loads. Therefore, it may be acceptable for some applications to allow the drive to operate in the overmodulation range, perhaps until 0.95 modulation index and even higher. Loads with large transient inductance can easily suppress the harmonics generated in the low end of the overmodulation range. In current ripple sensitive low inductance loads, the operating region perhaps could be limited to this value or less such that the overmodulation region drive performance does not significantly degrade. Since all modulators have essentially the same waveform quality beyond 0.95 modulation index, in this region the modulator choice could involve optimization of other performance indices such as the gain and switching losses.

In the previous chapter it was shown all DPWM methods have approximately equal HDF in the higher end of the linear modulation region. This argument is also valid for the switching frequency harmonics of the modulation

wave in the overmodulation region. Therefore, in the overmodulation region the waveform quality of all the discussed DPWM methods is practically the same as DPWM1 which has been investigated in this chapter. Since these results are also applicable to GDPWM at any modulator phase angle, an alternative to DPWM1 could be considered for switching loss reduction. However, transition from one operating point to another in the overmodulation region may result in substantial transients due to the differences in the voltage gain characteristics. Therefore, due to its superior voltage gain characteristic, the choice of DPWM1 from the beginning of the overmodulation region until the six-step operating mode is favorable. This result clearly indicates that for voltage feedforward drives, DPWM1 provides optimal performance in the overmodulation region from the global perspective of waveform distortion minimization, maximum voltage gain, and switching losses, and minimum transients. The overmodulation region experimental results of a voltage feedforward controlled drive are provided next.

4.8 Experimental Results

In this section the experimental voltage gain characteristics of SPWM, SVPWM, and DPWM1 are extracted and their waveform characteristics are illustrated. For this purpose, an experimental system which consists of a PWM-VSI drive and a 10 HP induction machine has been utilized. The inverter drive employs triangle intersection technique based PWM and the carrier frequency is 5 kHz.

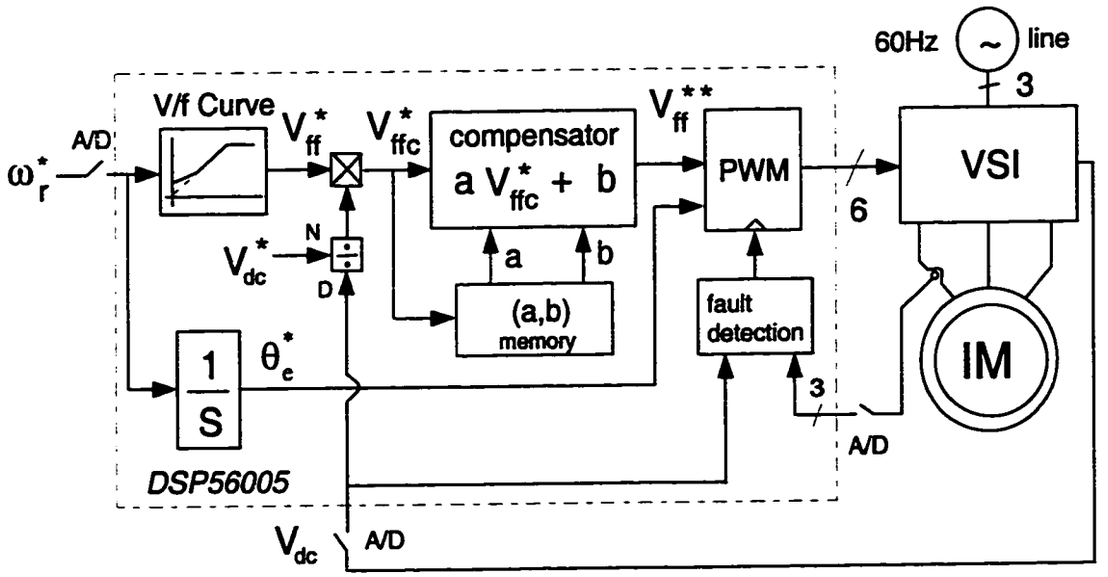

Figure 4.20: The experimental setup and the gain linearized DPWM1 based $\frac{V}{f}$ controlled motor drive block diagram.

The blanking time of the inverter is $4\mu s$. The controller is fully digital and it employs a 24 bit fixed point DSP (Motorola 56005) with 40 MHz clock frequency [80]. The experimental system diagram is shown in Fig. 4.20 in detail.

For the purpose of voltage gain measurement, operating the drive in the constant V/f mode is adequate and the motor can be operated at no-load. The V/f algorithm and the modulation waves are generated by the DSP. In particular, generation of all the discussed modulation waves, exact blanking time compensation, and when required MPW control are all simple tasks requiring only a few lines of software code when employing a DSP. The digitally implemented triangle comparison hardware (PWM block) is also inside the DSP chip providing a compact integrated solution.

First, the SPWM and SVPWM method voltage gain characteristics were

extracted by measuring the reference and output line-line voltages from zero voltage until the six-step mode could be reached. The inverter output voltage fundamental component value was measured by a dynamic signal analyzer (HP35670A). The inverter DC bus voltage was also measured in order to account for the utility line and load dependent DC bus voltage variations. The test was conducted with and without PEM based MPW control algorithm. When employed, PEM eliminates (drops) the pulses which are narrower than $12\mu s$. Experimental results are shown in Fig. 4.21 along with the analytical results. As the figure clearly indicates, the theoretical and experimental results match with good accuracy. The SVPWM method has wider linearity range than the SPWM method, and both methods require very large reference signals in order to reach the six-step mode. As the experimental data indicates, PEM narrows the linearity range of both modulators quite significantly.

In the second stage, the gain characteristics of DPWM1 were measured, first without PEM control, and second with $12\mu s$ PEM control. In the following, an inverse gain algorithm was implemented for the PEM controlled case and gain data extracted. Selecting the MPW length as $12\mu s$, the inverse gain function data was computed from (4.44) and this data was utilized to extract the following numerical approximation for the inverse gain compensated modulation index function.

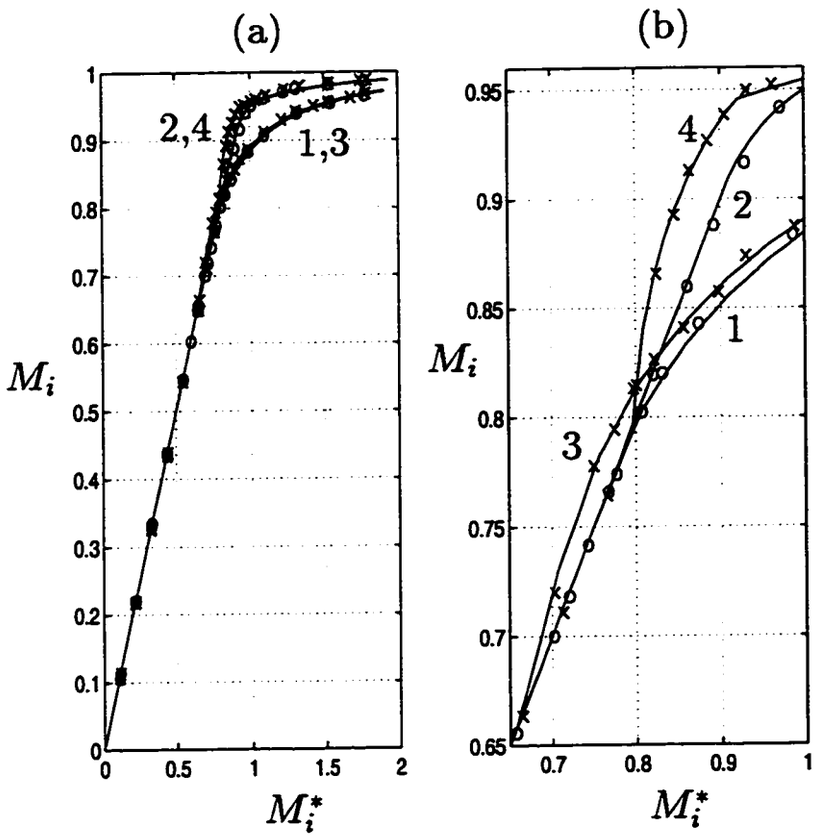

Figure 4.21: Experimental and theoretical $M_i = f(M_i^*)$ characteristics of SPWM and SVPWM. (a): Full modulation range, (b): Magnified view of the nonlinear modulation region. 1: SPWM, 2: SVPWM , 3: SPWM with MPW, 4: SVPWM with MPW. The experimental data is shown with "o", and "×" symbols, while the continuous curves correspond to the theoretical formulas.

$$M_i^{**}(M_i^*) = \begin{cases} M_i^* & 0 < M_i^* < 0.852, \\ 0.5252M_i^* + 0.4026 & 0.852 < M_i^* < 0.88 \\ 1.0823M_i^* - 0.0887 & 0.88 < M_i^* < 0.91 \\ 1.6659M_i^* - 0.6191 & 0.91 < M_i^* < 0.94 \\ 3.4396M_i^* - 2.2903 & 0.94 < M_i^* < 0.97 \\ 7.9754M_i^* - 6.6882 & 0.97 < M_i^* < 0.99 \\ 1.247 & 0.99 < M_i^* < 0.992 \\ 1.285 & 0.992 < M_i^* < 0.994 \\ 1.335 & 0.994 < M_i^* < 0.996 \\ 1.422 & 0.996 < M_i^* < 0.998 \\ 1.49 & 0.998 < M_i^* < 0.999 \\ 1.547 & 0.999 < M_i^* < 0.9993 \\ 1.65 & 0.999 < M_i^* < 0.9995 \\ 1.81 & 0.9995 < M_i^* < 1.0 \end{cases} \tag{4.50}$$

The above numerical representation provides a straightforward and highly accurate approximation with little computation and memory requirements, suitable for microprocessor or DSP implementations. In the gain linearized case, a DC bus voltage disturbance decoupling algorithm which scales the reference modulation index by $\frac{V_{dc}^*}{V_{dc}}$ was also implemented in order to account for the DC bus voltage variations. The $\frac{V_{dc}^*}{V_{dc}}$ value was computed by a simple Taylor series approximation ($\frac{1}{1+x} \approx 1 - x + x^2$) instead of straightforward division which consumes significant amount of computations. The complete block diagram of

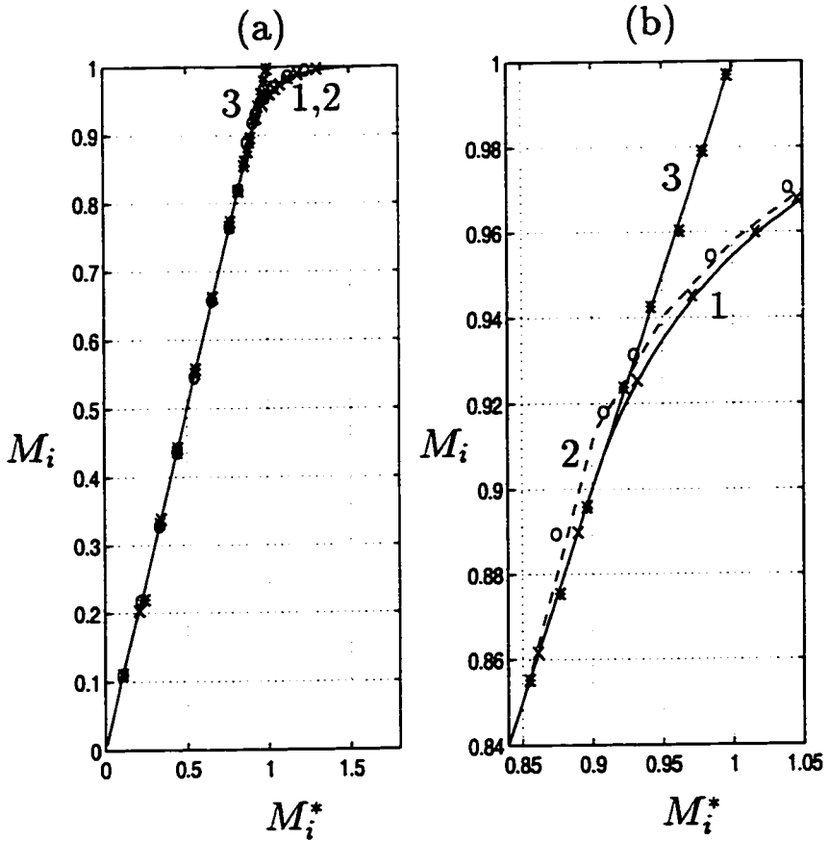

Figure 4.22: Experimental and theoretical $M_i = f(M_i^*)$ characteristics of DPWM1 with and without linearization (a) and the magnified view of the overmodulation region (b). 1: The theoretical $M_i = f(M_i^*)$ curve, 2: The theoretical $M_i = f(M_i^*)$ curve with MPW, 3: Ideal linear modulator line. The experimental results are shown with "o", "×", and "*" symbols.

the system for this case is shown in Fig. 4.20.

Figure 4.22 shows the theoretical and experimental gain characteristics of the DPWM1 method. The linearity range of the DPWM1 method as the data indicates is wider than the SVPWM case, and the influence of the MPW algorithm is significantly smaller. The gain compensator, as shown in the figure extends the modulator linearity until near the six-step operating mode with high accuracy.

For the purpose of comparing the waveform quality of DPWM1 and SVPWM, the motor currents for several modulation index values are demonstrated along with the modulation waveforms. The modulation signals were output from the DSP through a D/A converter and the triangular wave gain is $\frac{20V}{V_{dc}^*}$ ($\pm 10V$ represent the positive/negative DC rail clamp conditions). Figure 4.23 and Figure 4.24 illustrate the motor current and modulation waveforms of SVPWM and DPWM1 for $M_i^* \approx 0.75$. As the figures indicate, both modulators have good waveform quality within the linear modulation range and the ripple of SVPWM is slightly less. However, as the modulation index is increased and MPW control is applied the SVPWM performance degrades significantly. Figure 4.25 shows when a $12\mu s$ PEM is employed, the SVPWM method performance degrades at $M_i^* \approx 0.82$, a value significantly smaller than the theoretical linearity limit of 0.907. The modulator linearity is lost at $M_i^* \approx 0.82$ and the current waveform contains significant low frequency harmonic distortion leading to poor motor performance. As illustrated by the $M_i^* \approx 0.855$ operating point in Fig. 4.26, DPWM1 maintains linearity and low harmonic distortion in a significantly wider modulation range. As illustrated in Fig. 4.27 by the $M_i^* \approx 0.876$ operating point, beyond $M_i^* \approx 0.855$, modulator linearity is lost and the waveform quality significantly degrades. Further increase in the modulation index results in significant increase of the low frequency subcarrier harmonic content. Figure 4.28 illustrates the near six-step mode behavior of the inverter.

Notice in all the figures which belong to the high modulation region, the PWM ripple current magnitude appears to be practically the same. Since the

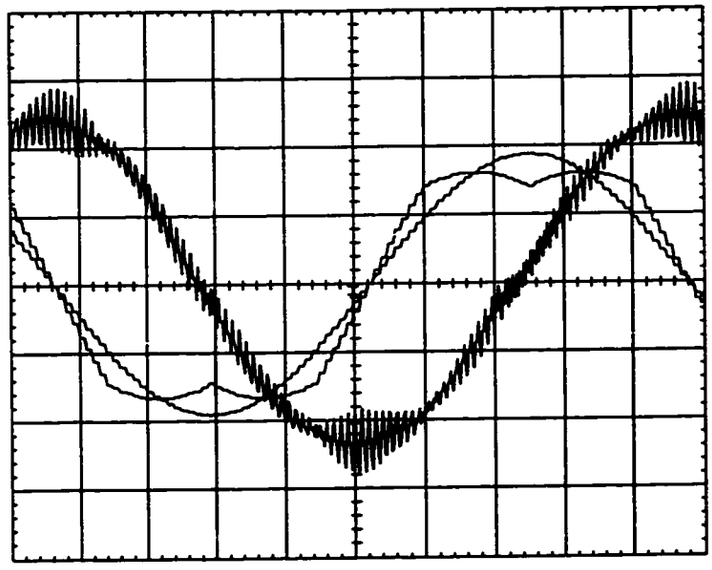

Figure 4.23: Experimental SVPWM modulation wave, its fundamental component and the motor current waveforms for $M_i^* = 0.75$. Scales: 2ms/div, 2A/div, 5V/div.

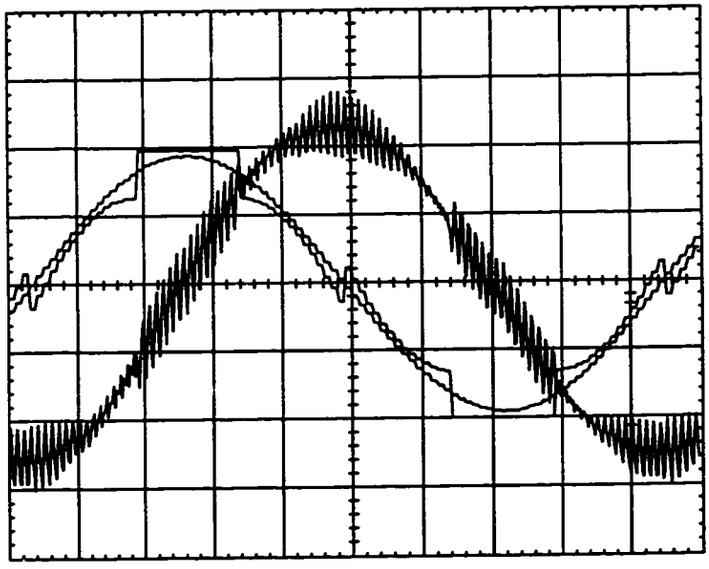

Figure 4.24: Experimental DPWM1 modulation wave, its fundamental component and the motor current waveforms for $M_i^* = 0.75$ value. Scales: 2ms/div, 2A/div, 5V/div.

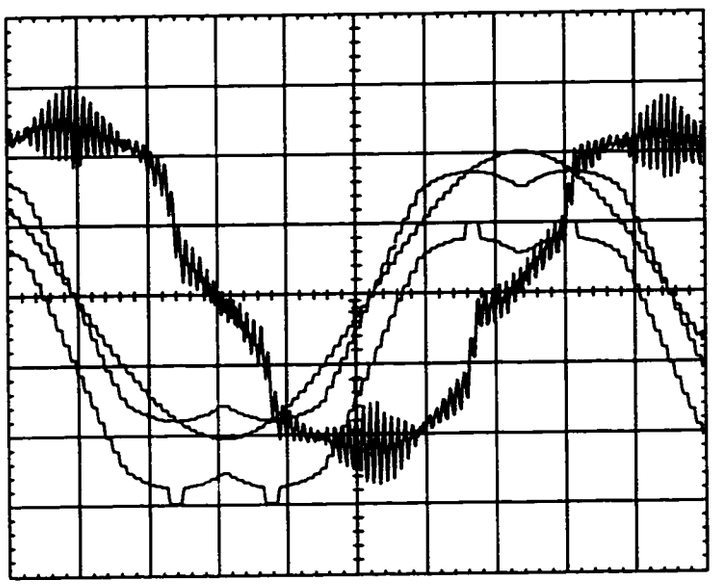

Figure 4.25: Experimental SVPWM modulation wave, modulation signal previous to MPW block, its fundamental component and the motor current waveforms for $M_i^* = 0.82$. Note the low frequency current harmonic distortion. Scales: 2ms/div, 2A/div, 5V/div.

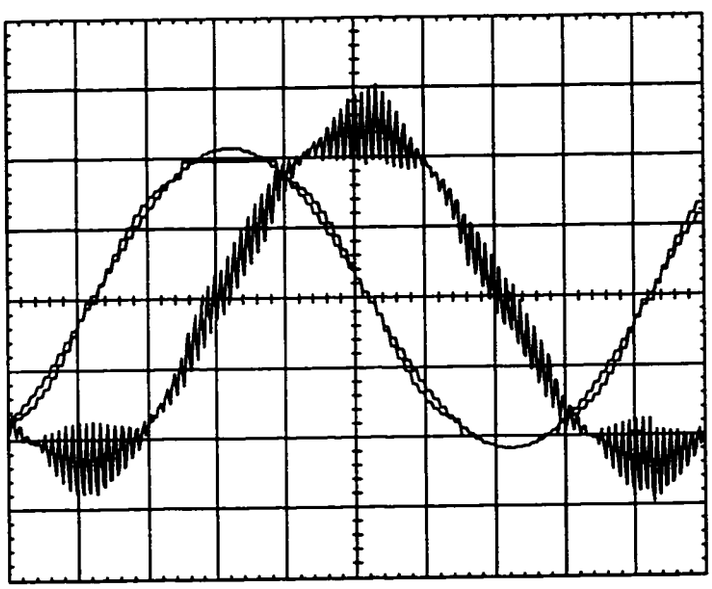

Figure 4.26: Experimental DPWM1 modulation wave, its fundamental component and the motor current waveforms for $M_i^* = 0.855$ value. Scales: 2ms/div, 2A/div, 5V/div.

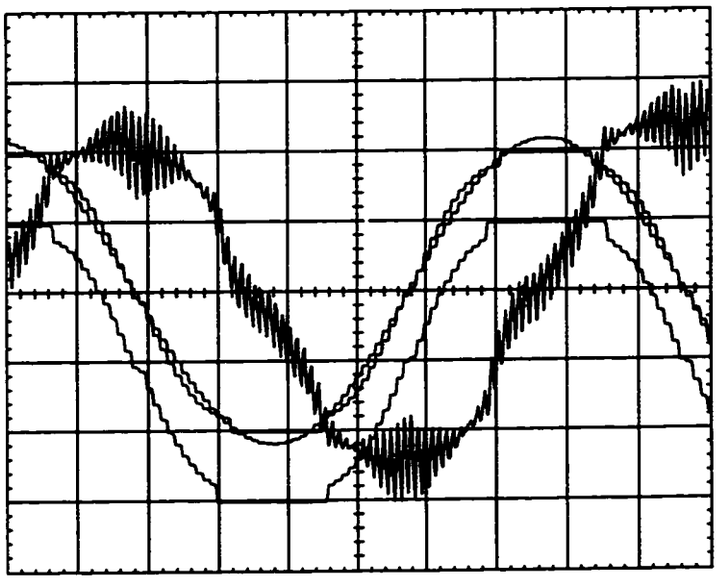

Figure 4.27: Experimental DPWM1 modulation wave, modulation signal previous to MPW block, its fundamental component and the motor current waveforms for $M_i^* = 0.876$. Scales: 2ms/div, 2A/div, 5V/div.

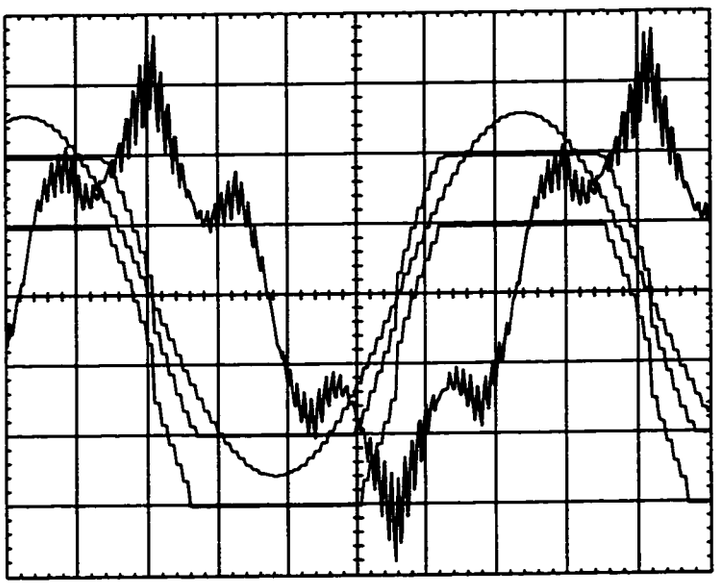

Figure 4.28: Experimental DPWM1 modulation wave, modulation signal previous to MPW block, and the motor current waveforms for $M_i^* = 0.964$. Note near the six-step mode the low frequency subcarrier harmonics are dominant. Scales: 2ms/div, 2A/div, 5V/div.

carrier frequency is fixed at 5 kHz for both SVPWM and DPWM1, the average switching frequency of DPWM1 is 33 % less than SVPWM. Therefore, DPWM1 has significantly reduced switching losses compared to SVPWM. Considering the reduction in the switching losses and increase in the linear modulation range, the DPWM1 method, clearly becomes the choice for operating in the high modulation range.

Finally, the sensitivity of the *V/f* controlled drive to DC bus voltage variations is illustrated with and without the inverse gain compensation and DC bus disturbance decoupling algorithms. The *V/f* controlled induction machine was operated at constant inverter output voltage reference value V_{lm}^{*} = 337 V (M_i^{*} = 0.855 at $V_{dc}^{*} = 620V$). Obtained from a diode rectifier, the DC bus voltage of the drive was slowly varied by adjusting the AC input voltage via an autotransformer and the motor terminal voltage was measured. Figure 4.29 illustrates the experimental inverter output voltage-DC bus voltage characteristics with and without inverse gain compensation and DC bus voltage disturbance decoupling. As the figure indicates, the compensated case output voltage is maintained at the commanded value until the DC bus voltage is significantly reduced and the inverter operates in the six-step mode. The uncompensated case output voltage significantly changes with the DC bus voltage variation. The motor speed and torque deviate from the normal operating points and poor drive performance results. Therefore, the compensated drive performance is insensitive to the DC bus voltage variations for a wide range of DC bus voltage variations (utility line voltage sag or surge conditions), while

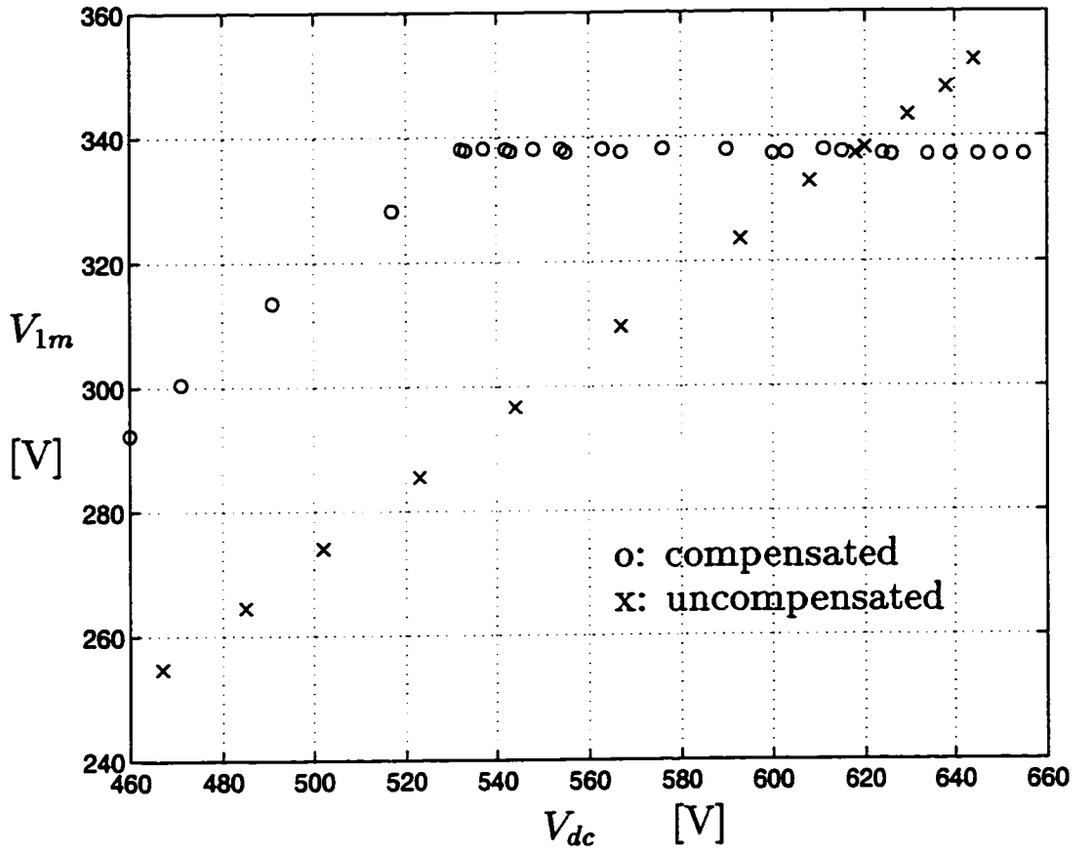

Figure 4.29: Experimental drive terminal voltage-DC bus voltage characteristics for $V_{1m}^{*} = 337$ V.

the uncompensated drive experiences disturbances.

4.9 Voltage Feedforward PWM-VSI Drive High Performance Modulator Design

In the previous chapter the linear modulation region performance analysis of modern modulators indicated SPWM or SVPWM could provide superior performance in the lower linear modulation region and GDPWM and DPWM3

have superior attributes in the remainder of the linear modulation region. As this chapter illustrated the superior overmodulation region performance characteristics of DPWM1 (as a unique operating point of GDPWM), the conceptual stage of a high performance modulation algorithm design has been completed for voltage feedforward drives. The remaining task in the high performance modulation algorithm design procedure is to select appropriate modulation methods, determine the modulation method transition points and establish the control algorithm.

To maximize the drive performance, the transition point from SPWM/SVPWM to GDPWM and the ψ value of GDPWM must be properly selected. As the previous chapter indicated, the transition point from SPWM/SVPWM to GDPWM is determined by the waveform quality characteristics while the GDPWM modulator phase angle ψ is determined from the switching loss and voltage gain characteristics. Figure 4.30 shows the on-line modulator selector flow diagram of the proposed algorithm. Simple in structure and computational procedure, the algorithm requires only two transition modulation indices and φ as optimization parameters. With φ on-line estimated, the algorithm on-line calculates the optimal ψ to maximize the drive performance.

The transition value M_{itr2} is determined by the GDPWM linearity limit from (3.54) for $k_m = 1$. However, the optimal value of M_{itr1} depends on the carrier frequency value as well as the SLF and HDF characteristics. To assist in selecting this transition value, the HDF curves of SVPWM and GDPWM for

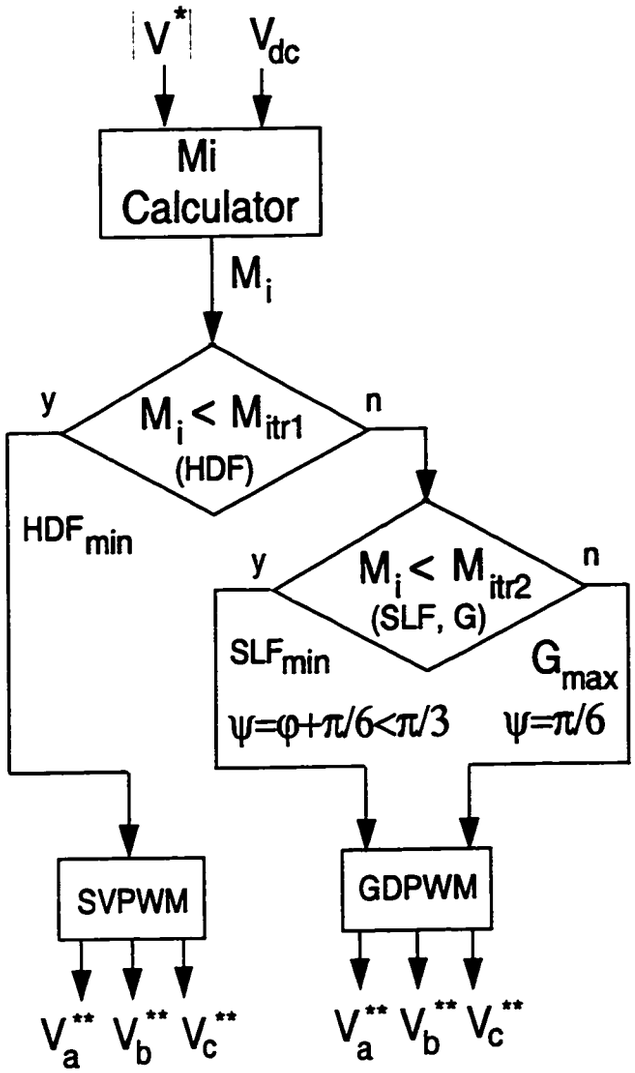

Figure 4.30: The combined high performance PWM algorithm flow diagram.

various carrier frequency values are compared in Fig. 4.31 for $\psi = \frac{\pi}{4}$ (approximate average value over $0 \leq \psi \leq \frac{\pi}{3}$). As the figure indicates, depending on the carrier frequency value, three practical cases can be distinguished.

1) Constant carrier frequency ($f_c = const.$): As Fig. 4.31 indicates the theoretical HDF curves of SVPWM and GDPWM do not intersect and SVPWM is superior to GDPWM until M_{itr1} (calculated from (3.54) for $k_m = 2$). As a result, transition from SVPWM to GDPWM at a point before M_{itr1} implies an increase in the current waveform distortion. However, according to Fig. 3.21 with early entrance to GDPWM, the switching losses can be reduced by as much as 50%. If the waveform quality requirements are not stringent, the M_{itr1} value should be selected as small as possible. Given a HDF limit, the M_{itr1} transition point can be easily determined from Fig. 4.31. More precise calculations to determine its value could involve (3.42) and (3.54).

2) Constant inverter average switching frequency ($f_{swave} = const.$): In this case, the carrier frequency for SVPWM case is selected as f_c, and for GDPWM as $1.5f_c$, such that the inverter average switching frequency, f_{swave} remains constant. The HDF curves of Fig. 4.31 indicate the intersection point of SVPWM and GDPWM is at $M_{itr1} \approx 0.65$. Therefore, this M_{itr1} value minimizes the HDF of the drive, and under this condition the switching losses in the GDPWM mode are reduced by at most 25% when compared to SVPWM.

3) Constant switching losses ($P_{swave} = const.$): In this case, the carrier frequency for SVPWM case is selected as f_c, and for GDPWM as $2f_c$, such that

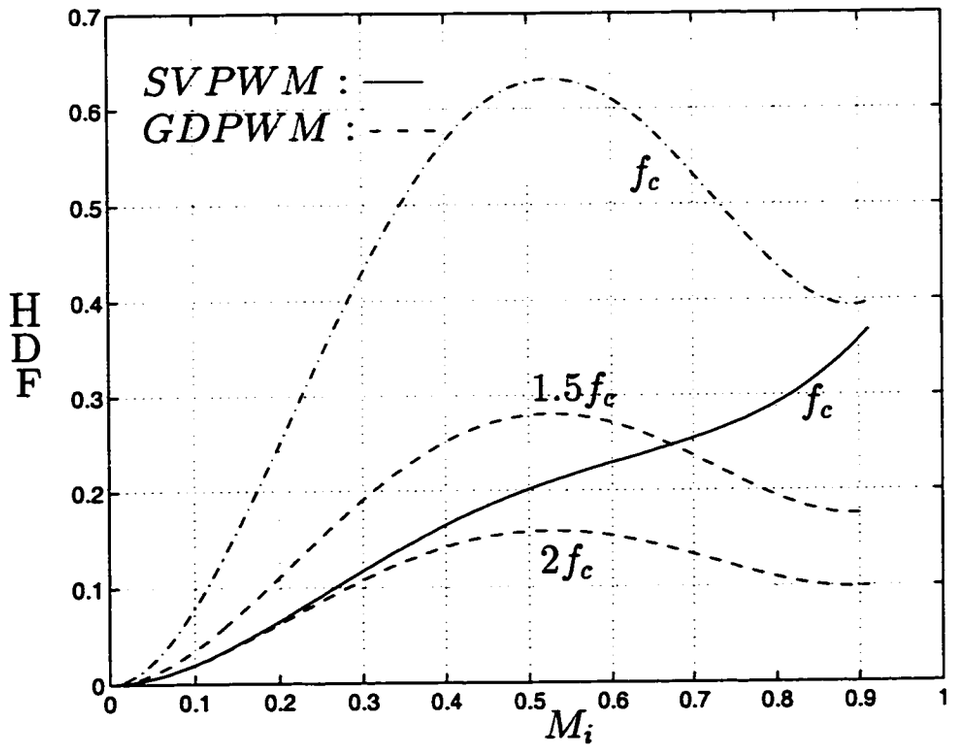

Figure 4.31: $HDF = f(M_i)$ curves of SVPWM and GDPWM for various carrier frequency values illustrate the optimal transition points/regions.

the inverter switching losses P_{swave} remain constant (this is true for $-30° \leq \varphi \leq 30°$ where the optimal SLF of GDPWM is 0.5). Figure 4.31 indicates that the SVPWM and GDPWM method curves are close together until near a modulation index of 0.3, then GDPWM method becomes superior. With this approach, smallest possible M_{itr1} becomes equal to the undermodulation limit of GDPWM defined in (3.55). Figure 4.31 indicates, in applications with small current ripple requirement, $M_{itr1} \approx 0.3$ would yield superior performance. Note in this case SPWM can be utilized instead of SVPWM. Since at such low modulation levels SPWM and SVPWM have practically the same performance, SPWM can be chosen for its implementation simplicity.

The full PWM algorithm can be easily and efficiently programmed in a microprocessor or a DSP leading to a low cost high performance drive. Since the transition from SVPWM to GDPWM only involves a zero sequence signal, oscillatory transitions do not affect the load current fundamental component and motion control. Only the switching frequency harmonic content changes. The computational requirements of the algorithm (including the modulation signal generation) are only slightly higher than the conventional modulation methods. Thus, the algorithm is suitable over a wide range of applications where low cost, high performance, and high energy efficiency are in demand. Perhaps, the most suitable applications of the combined algorithm are the future generation multi-purpose intelligent drives. With the controller tuning the modulator on-line for the application, or by allowing the user to configure the modulator of his/her choice, an increased level of performance and satisfaction to the costumer would result. Therefore, it is believed this algorithm will be an indispensable feature of future generation drives.

Linear modulation region performance of the above described high performance modulation algorithm was illustrated in the previous chapter by laboratory experiments. The present chapter experimentally illustrated the DPWM1 overmodulation region performance with a different motor from the motor utilized in the experiments of the previous chapter. The overmodulation region performance of the above described modulation algorithm with the previously utilized motor will next be presented for the sake of completeness.

4.10 Experimental Results of GDPWM in the Overmodulation Region

The high performance modulation algorithm combining SVPWM in the low modulation region, and GDPWM from the transition modulation index until the six-step operating point was tested in the laboratory and the linear modulation region performance was illustrated in the previous chapter. The overmodulation region performance of the drive with the same motor will be illustrated in this section. As described in the experimental results section of the previous chapter, with $12\mu s$ minimum pulse width control (PEM) the GDPWM voltage linearity ends at 0.854 modulation index (calculated from (3.54)). However, the experimental study indicated transition at 0.86 modulation index value did not cause noticeable waveform quality degradation. Therefore, $M_{itr2} = 0.86$ was selected. As a result, within $0.81 < M_i < 0.86$ the GDPWM method reduces the switching losses significantly and maintains high waveform quality. Above M_{itr2} the GDPWM algorithm on-line selects $\psi = \frac{\pi}{6}$ for maximum voltage gain, and the inverse gain compensated and DC bus voltage disturbance rejected modulator operates in the overmodulation range.

Figure 4.32 and Figure 4.33 show the modulator and motor phase current waveforms during and after transition to the nonlinear modulation range ($M_i = 0.86, 0.903$). As the figures indicate the zero sequence signal oscillation (sudden variation of ψ) does not distort the fundamental component current, and motion

quality is not affected. As the HDF curves of Figure 3.17 suggest, in the upper linear modulation range the phase current ripple of GDPWM decreases as the modulation index increases. In the overmodulation range the switching losses are reduced by at least 40% when compared to SVPWM. As the modulation index is further increased large amount of non-triplen odd subcarrier frequency voltage/current harmonics are generated and the waveform quality degrades due to inverter saturation. However, as Figure 4.34, and Figure 4.35 indicate, the modulated segments of the current waveform still retain the low harmonic distortion characteristic of the GDPWM method.

Figure 4.36 and Figure 4.37 illustrate and compare the effect of the PEM algorithm on the SVPWM and GDPWM method performance. As the experimental waveforms indicate, with 12 μs PEM, the SVPWM method looses linearity at a lower modulation index than GDPWM method and the phase current waveform distorts significantly. As all the experimental waveforms indicate, the SVPWM method in the lower modulation range combined with the GDPWM method in the remainder of the range is a superior approach.

4.11 Summary

Closed form fundamental component voltage gain formulas of the conventional carrier based PWM methods, which are useful tools in the analysis and design

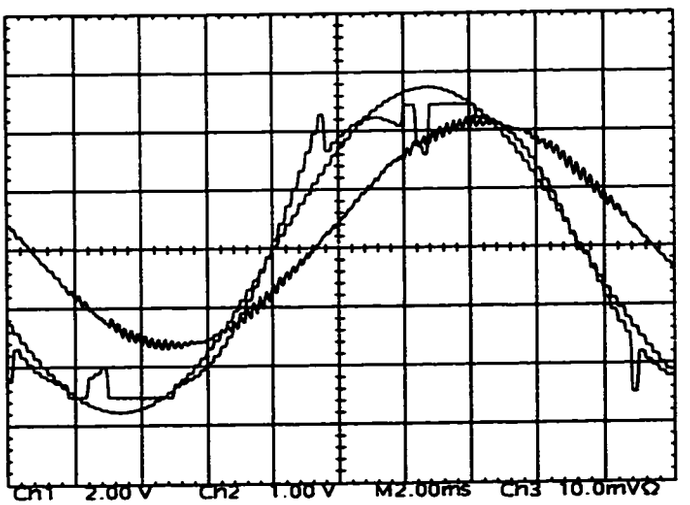

Figure 4.32: Transition of GDPWM from $\psi = \varphi$ to $\psi = 0$ ($M_i = 0.86$, 54 Hz, $100\%T_{eR}$). Scaling: 5 A /div, 2 V /div, 2ms/div.

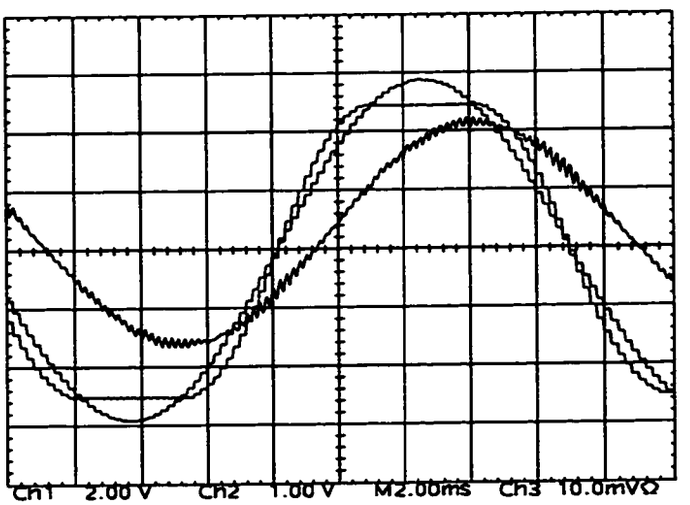

Figure 4.33: Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.903$, 56 Hz, $100\%T_{eR}$). Scaling: 5 A /div, 2 V /div, 2ms/div.

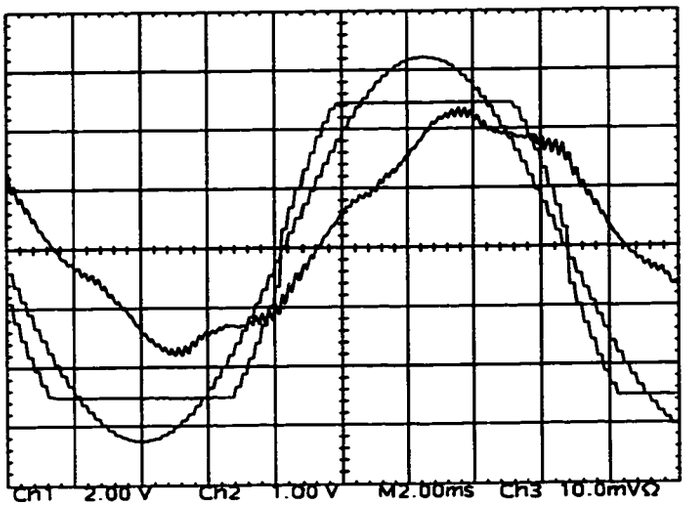

Figure 4.34: Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms in the overmodulation range ($M_i = 0.96$, 59 Hz, $100\%T_{eR}$). Scaling: 5 A /div, 2 V /div, 2ms/div.

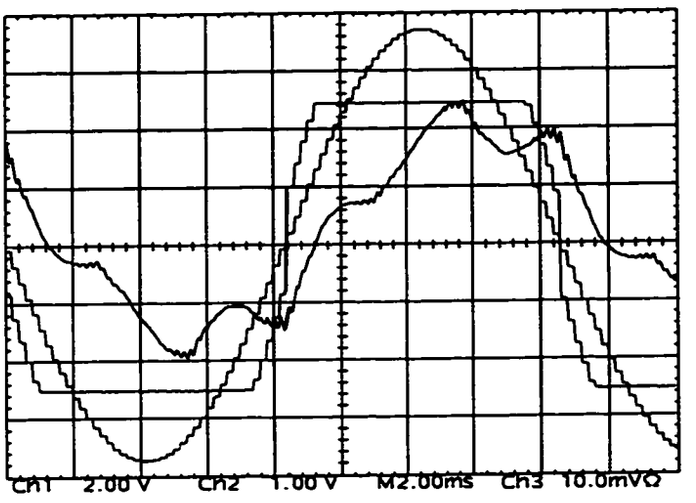

Figure 4.35: GDPWM modulation wave and motor current waveforms in the overmodulation range ($M_i = 0.986$, 60 Hz, $100\%T_{eR}$). Scaling: 5 A /div, 2 V /div, 2ms/div.

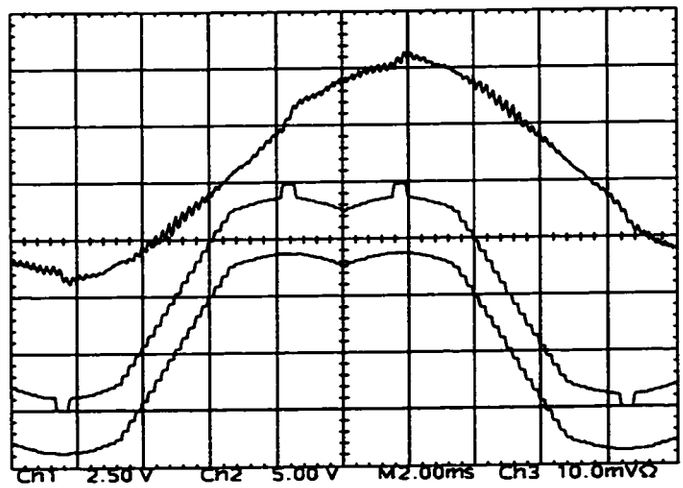

Figure 4.36: SVPWM modulation wave, PEM controlled modulation wave and the motor current waveforms for $M_i = 0.815$, 49 Hz. Scaling: 5 A /div, 2 V /div, 2ms/div.

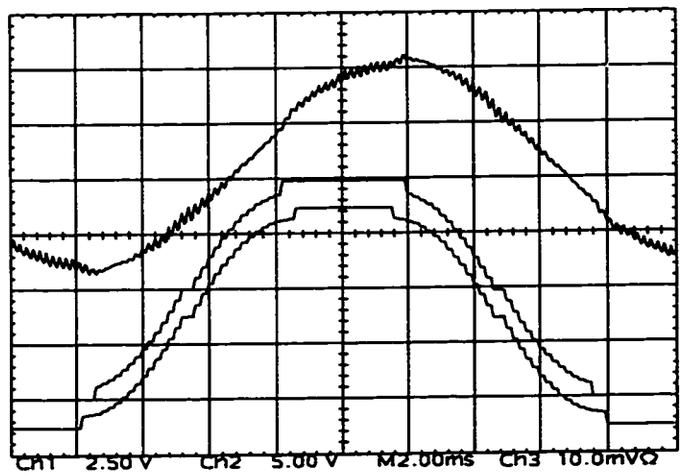

Figure 4.37: GDPWM modulation wave, PEM controlled modulation wave and the motor current waveforms for $M_i = 0.867$, 53 Hz. Scaling: 5 A /div, 2 V /div, 2ms/div.

of PWM-VSI drives were derived. High modulation index operating range voltage gain characteristics of various conventional carrier based PWM methods were analyzed and comparative results provided. Overmodulation region waveform characteristics of various PWM methods were numerically investigated and compared. The study indicates the DPWM methods have wider linearity range than the CPWM methods. The overmodulation range performance characteristics of DPWM1 are shown to be superior to the remainder of the known modulators. The voltage gain of DPWM1 is exceptionally high and its harmonic distortion is low.

It is shown that the inverter blanking time and minimum pulse width control based nonlinearities can significantly influence voltage gain and harmonic distortion characteristics of a modulator. MPW control significantly reduces the linearity range and increases the harmonic distortion. The effect is less significant in DPWM methods compared to CPWM methods.

The study indicates that for best overall performance a combination of various modulators must be employed: In the low modulation index range SVPWM has lower harmonic distortion. In the high modulation index range DPWM methods have wider linearity and less harmonic distortion. In the high linear modulation region the superiority of GDPWM was illustrated in the previous chapter. Therefore, in the overmodulation region, selecting the DPWM1 operating point of GDPWM results in optimal performance.

Voltage gain linearization is a simple task with DPWM1, and a polynomial

curve fit based inverse gain function in most of the region, and a small table entry near six step was found to be adequate to provide good linearity in the overmodulation range. The simplified inverse gain compensation and DC bus disturbance decoupling algorithms linearize the modulator with high accuracy and result in high drive performance.

Experimental voltage gain and waveform characteristics are in good agreement with the theoretical predictions, and illustrate the performance superiority of GDPWM over SVPWM in the high modulation and overmodulation range (in particular of DPWM1).

Finally, the high performance modulator design rules for voltage feedforward controlled drives were established and a high performance modulation algorithm which combines SVPWM and GDPWM was developed. Simple design formulas and graphics, which overly simplify the voltage feedforward drive modulator design procedure were established.

The next chapter addresses the overmodulation issues of closed loop current controlled PWM-VSI drives. With the dynamic performance requirements of current controlled drives being substantially higher than voltage feedforward drives, these drives differ in design and performance than the voltage feedforward drives. Therefore, the subject is of significant importance and will be thoroughly investigated in the remainder of this thesis.

Chapter 5

Overmodulation in Current Controlled Drives

5.1 Introduction

The performance of voltage feedforward controlled constant $\frac{V}{f}$ PWM-VSI drives is insufficient for most industrial processes with stringent position, speed, and torque regulation and high dynamic response requirements. Its AC power line and motor load disturbance rejection capability is also poor. Therefore, many applications require higher performance control methods. Electric traction, elevators, textile machines, paper and plastic machines, steel mills, conveyors, cranes, machine tools, etc. belong to the industrial drives category with stringent speed/torque regulation and disturbance rejection requirements. Assembly robots, semiconductor manufacturing, disk drives, cutting machines, etc. belong to the servo drives category and these drives additionally require precise position control, and more stringent regulation. When operated as a regenerative converter, the PWM-VSC interfaces a three phase AC voltage source with a

DC link voltage source. In such applications power flow must be tightly regulated for high performance and safe operation. Therefore, high bandwidth and good disturbance rejection characteristics are required. Three phase UPS applications have similar requirements. In all these applications, PWM-VSI drives employ inner current or flux loops to improve the regulation, dynamic response, and disturbance rejection. With the exception of the DTC methods which employ flux and torque regulators, modern high performance PWM-VSI drives generally utilize current controllers.

In current controlled drives, the current references are generated by the outer control loops (the speed loop of an AC machine or the DC link voltage loop of a PWM-VSC etc.). In tension control applications, the torque producing current reference may be directly obtained by scaling the torque reference (in case of nonlinear torque-current relations, by reading the current reference value from a table etc.) and the flux producing current reference is directly commanded (constant or a function of the motor speed/voltage). Depending on the controller structure involved, the reference currents may be three phase (abc) variables or two phase (d-q) variables. In the latter case, they may be defined in the stationary frame or a rotating frame (typically synchronous frame). Once the reference currents are generated the task of a current controller is to generate a switching pattern for the inverter that will force the load currents follow the reference currents as accurately as possible. However, with the DC link voltage being lmited and variable (due to the finite DC bus capacitor size of most drives) and the switching frequency being finite, the current controller

performance is constrained.

In the carrier based PWM methods, the modulator voltage linearity boundaries may significantly constrain the performance of a current controller. Due to the interaction between the outer loops (speed/position/DC voltage regulation loop etc.), current loop and the modulator, in the overmodulation region the drive performance may degrade significantly. Therefore, the steady state operation of most high performance current regulated PWM-VSI drives is confined to the linear modulation range. However, operation in the overmodulation region may be allowed during transients and in the so called "dynamic overmodulation" region the full voltage capability of the modulator may be utilized to improve the dynamic response. For example, in an induction motor drive, the speed response and robustness to load torque variations and disturbances can be greatly improved. Therefore, the overmodulation region performance issues of current controlled drives deserve a detailed study and thorough understanding.

Since the duration of the dynamic overmodulation transients can be smaller than the minimum fundamental cycle (at the maximum fundamental frequency), the per fundamental cycle modulator characteristics are not appropriate for the investigation of the dynamic overmodulation behavior of a modulator, and the per carrier cycle voltage linearity is important. The dynamic overmodulation characteristics of various direct digital PWM methods were investigated in [88, 131, 58] and various solutions with performance and implementation

complexity trade-offs have been developed. The dynamic overmodulation characteristics of the triangle intersection PWM methods of Fig. 3.7, however, have not been reported and their behavior is not well understood. In this chapter, the influence of the triangle intersection PWM method voltage linearity on the current controller and drive performance will be thoroughly investigated.

Although the focus of this chapter mainly involves the overmodulation region behavior of current loops, a clear understanding of the linear modulation region behavior is necessary for a thorough understanding of the issues. Therefore, the chapter will start with a review of the current regulator operating principles, design, and implementation methods. In particular the fully digital Synchronous Frame Current Regulator (SFCR), which is the wide most recognized current regulation technique (it has zero steady state error and superior dynamic performance) will be reviewed in detail. Following, the current regulator behavior in the overmodulation region will be thoroughly investigated. The direct digital PWM dynamic overmodulation methods will be reviewed. The dynamic overmodulation characteristics of the popular triangle intersection PWM methods will be analyzed in detail. Following the discussion on the influence of these characteristics on the drive performance in various applications, the induction motor drive dynamic overmodulation behavior will be investigated in detail and the correlation between theory, simulations, and laboratory experiments will be illustrated. Finally, the steady state operating performance and voltage limit will be discussed.

5.2 The Synchronous Frame Current Regulator

Shown in Fig. 5.1 in detail, SFCR is the industry standard high performance current control method. In this method, the reference and measured three phase currents are transformed to the d-q coordinates which rotate synchronously with the electrical frequency of the system (the angular speed of the stator flux of a motor, the AC line frequency of a VSC etc.). The transformed currents are compared with their reference values, and the errors are input to PI controllers to generate the synchronous frame feedback voltage references. Voltage feed-forward signals and inductive cross-coupling decoupling voltage references are added to the feedback references to form the total d and q axis voltage references. These synchronous frame reference voltages are transformed to the stationary d-q frame and at this stage a modulator is involved in generating the switching device gate signals. In the direct digital modulation technique, the stationary frame d-q voltage references are directly utilized to calculate the switch duty cycles. In the triangle intersection technique, transformation from d-q frame variables to abc variables is required, and then generation of the modulation signals follows. The modulation techniques described in the previous chapters are utilized to generate the switching signals.

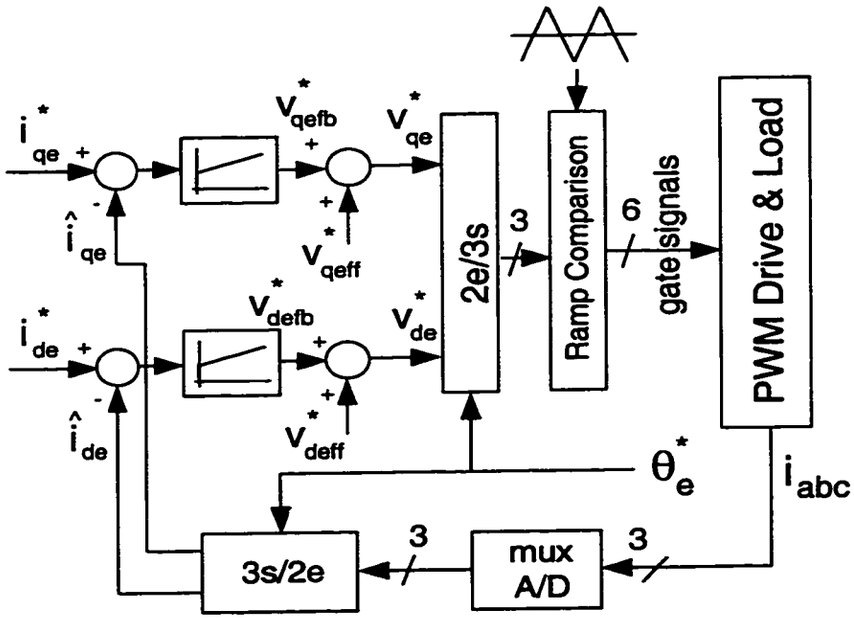

Figure 5.1: High performance drive employing the SFCR algorithm.

At sinusoidal steady state the synchronous frame d and q axis currents become DC variables. Therefore, SFCR yields zero steady state error. The cross-coupling decoupling terms eliminate the coupling between the d and q axis controllers and yield two independent current controllers. The voltage feedforward terms form a direct signal path for the EMF decoupling purpose and therefore enhance the drive dynamic performance. Algorithms and calculations involving the voltage feedforward terms have been discussed in detail in [50]. With the voltage feedforward terms forming the most significant portion of the reference voltage magnitudes, the PI controller output signal range can be retained wide. With a wider PI controller gain choice and wider number range for the integrators, a higher performance drive can be realized.

The SFCR performance is strongly dependent on the implementation method involved. The regulator can be implemented with analog hardware or digital hardware/software. Mostly suitable for analog implementation, its stationary frame equivalent implementation (illustrated in Figure 2.2.b) eliminates the stationary to synchronous frame and backwards coordinate transformations [167]. In the conventional SFCR digital software implementation, however, the coordinate transformations are easily computed. In all the implementations, one important detail is the feedback current measurement technique involved. The feedback current measurement, conditioning and processing methods strongly influence the current regulator steady state and dynamic performance.

In the analog current regulator implementation, the feedback current signals are continuously monitored by the controller. Therefore, the output signals of the PI controllers and the modulation signals continuously vary. However, in order to avoid multiple switchings (more than one switching per device over a half carrier cycle may occur due to noise or system dynamics), a lockout circuit is involved. Following a switching action, the gate signal of each switch retains its position for at least the remaining time interval of the corresponding half carrier cycle. Required for safe thermal and electrical performance, this constraint limits the current controller dynamic response. This limitation on the dynamic performance of the drive can be modeled as a modulator delay and is termed as "PWM delay." As shown in Fig. 5.2(a), in this case the PWM delay is $\frac{T_s}{4}$ (T_s is the carrier wave cycle), the weight center of the half carrier wave. Since the modulation wave is allowed to change once within every

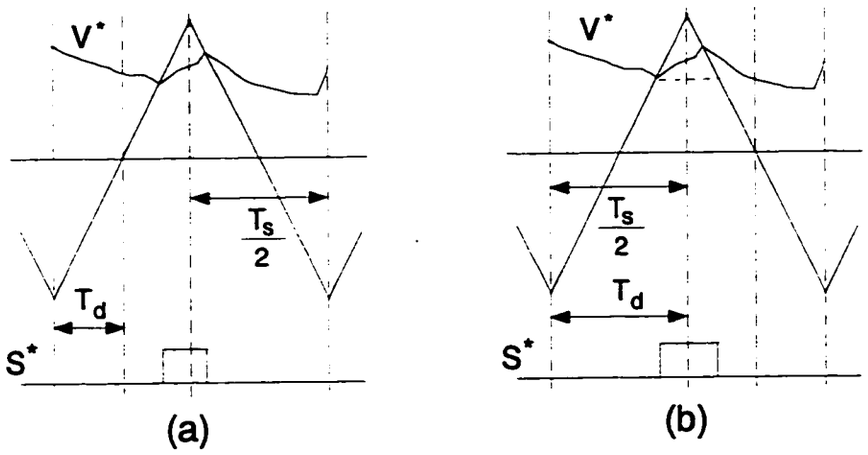

Figure 5.2: Analog current regulator reference, carrier, and gate signal waveforms, and the PWM delay: (a): Asymmetric PWM, (b): Symmetric PWM.

half carrier cycle, typically asymmetric pulse pattern occurs, and this leads to increased steady state voltage and current harmonic content. As shown in Fig. 5.2(b), in order to reduce the harmonic content, symmetric switching can be employed (the first time a switching occurs in a carrier cycle the modulation wave is sampled and held constant until the end of the cycle) at the expense of increasing the PWM delay to $\frac{T_s}{2}$. Although the modulator signal is sampled and held constant, the current regulator proportional and integral components continuously operate on the current errors such that the current controller prime characteristics are not strongly affected. In either case, while in the modulator linearity range, the feedback PWM harmonic currents only slightly influence the drive performance, and the switching frequency harmonic content may slightly increase. Therefore, the analog implementation of SFCR has high steady state and dynamic performance.

In the digital software implementation, the feedback currents can not be continuously monitored. Instead, the feedback currents or their integral value (charge) over a specific time interval is sampled with an analog to digital (A/D) converter. With the integral value of the switching frequency components (harmonics) of the feedback currents over a carrier cycle (or half carrier cycle) being equal to zero, following a scaling operation on the sampled value (dividing the integral value by the time interval) the computed value corresponds to low frequency components (lower than the carrier frequency). During steady state it equals the fundamental component value. This technique is also called the average sampling technique. The method yields high signal to noise ratio. However, in addition to an A/D converter, the integral value sampling technique requires a high accuracy analog integrator and a reset circuit. Therefore, the integral value sampling technique is expensive and most applications employ the simpler and more economical synchronous sampling technique.

In the synchronous sampling technique, the feedback currents are sampled at the positive and/or negative peaks of the triangular carrier signals. With the switching frequency harmonic currents at these instants being negligible, the measurement values correspond to the feedback current low frequency components (at sinusoidal steady state they correspond to the fundamental component). The microscopic harmonic voltage and current waveform sketches of Figure 5.3 aid illustrating this characteristic of inductive loads. How accurately the synchronous sampling method represents the low frequency component depends on the load transient impedance time constant to carrier cycle ratio; the

larger the ratio, the better the approximation. A ratio of 10 or higher (typical) yields satisfactory results. For systems with very small time constant, the synchronous sampling method may not provide sufficiently accurate fundamental component estimation. In such cases, as shown in Figure 5.3 by dashed curves, the harmonic currents are significantly phase advanced with respect to the triangle peak points due to the exponential decay the resistive component of the transient impedance provides. In such applications, the per half carrier or per carrier cycle average value obtained by the integral sampling technique can give a better fundamental component estimate [12, 126]. As previously described, such integral value methods are involved and require dedicated hardware.

Since in the synchronous sampling technique, the feedback current signal is sampled only at specific instants, noise in the system can affect the measurement accuracy to a greater extent than the integral measurement. A/D sampling delays and bit resolution issues can also be other significant limiting factors. However, in most drives the measurement accuracy of the synchronous sampling technique is satisfactory. Therefore this method is widely employed [206]. With proper signal conditioning and low cost and high accuracy A/D converters (10-12 bit) the measurement accuracy meets the demand for most applications.

As shown in Fig. 5.4, when utilizing the synchronous sampling method, the signal is available at the following rates: $\frac{T_s}{2}$, T_s, $2T_s$, ..., NT_s. The figure also illustrates the PWM signal of a phase for the maximum PWM update rate condition. Depending on the controller response requirement, sampling rate

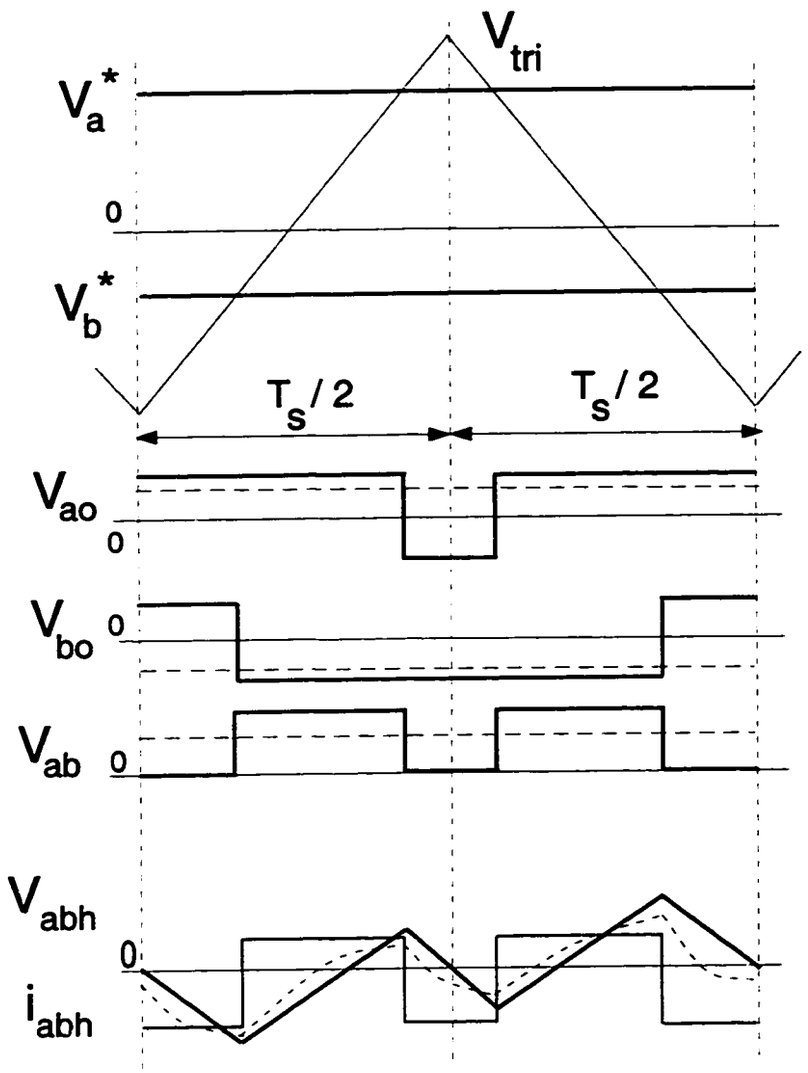

Figure 5.3: Microscopic view of PWM harmonic voltage and current waveforms. In the bottom two plots, the solid lines represent the line to line harmonic currents for purely inductive harmonic model, and the dashed curves illustrate the case with R-L model.

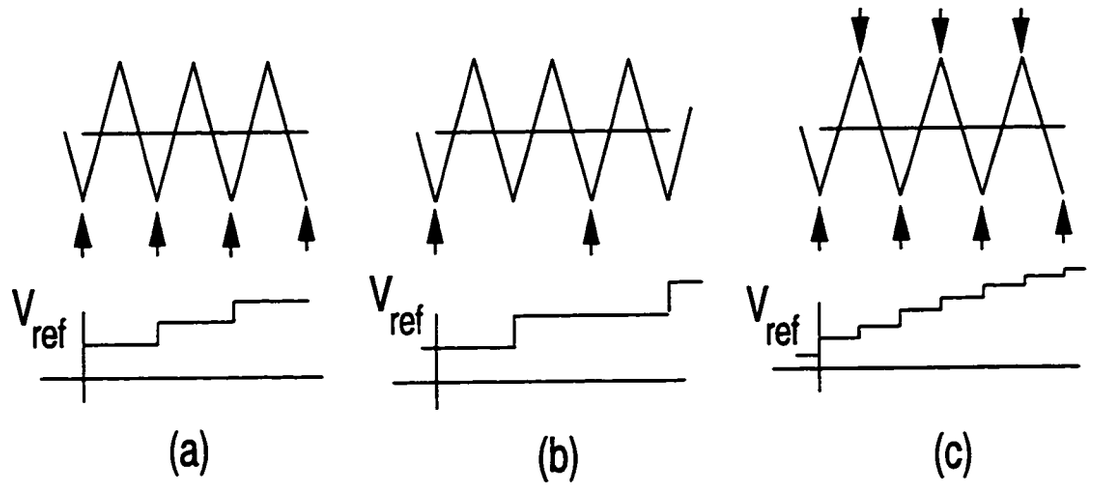

Figure 5.4: Synchronous Sampling Method. (a) : Once per carrier sampling, (b): Half carrier rate sampling, (c): Twice per carrier sampling. Arrows indicate the sampling instants. Bottom traces illustrate the modulation signals with maximum PWM update rate for each sampling case.

available, and processor structure, the most suitable of all the possible sampling rates is chosen. The synchronous sampling technique brings an additional limitation to the digital SFCR dynamic performance. The feedback current sampling rate influences the controller performance as a delay element. Therefore, slower sampling rates imply reduced dynamic performance.

Since in the digital SFCR the feedback current signal is read by the signal processor at most twice per carrier, the controller can at most update the modulation reference waveforms at this rate. As illustrated in Fig. 5.5, the regulator dynamic response is poorer than the analog current regulator case, and its actual value depends on the feedback current sampling rate and measurement method, and PWM write-out rate. As Fig. 5.5(a) indicates, twice per carrier cycle synchronous sampling with twice per carrier PWM signal update rate (the

phase currents are sampled and the PWM signals are output simultaneously at the positive and negative peaks of the triangular carrier wave) result in three-fourth carrier cycle delay (smallest possible). Shown in Fig. 5.5(b), in the more conventional case, once per carrier sampling and update rate (synchronized), the total delay is $1.5T_s$ (from the time the signal is measured, to the first PWM write-out time a T_s time length, and from the PWM write-out time to the weight center of the carrier cycle $\frac{T_s}{2}$). Lower sampling rates and PWM signal output rates imply increased delay and reduced bandwidth. The integral sampling method has an additional latency which equals half the integration time interval. Several feedback current sampling delay compensation methods have been proposed and utilized in applications that the delay degrades the performance significantly [126]. Further improvements on feedback current sampling, signal conditioning, and accurate fundamental component detection have been reported in [12, 39, 73, 184].

As the above discussions indicate, in analog SFCR implementations the PWM delay is small, while in the digital implementation in addition to the PWM delay a feedback signal delay exists. Therefore, with the same controller gains, an analog implementation has superior dynamic performance compared to digital implementation. However, the PWM and feedback current sampling delays are considered second order effects in determining the drive dynamic response and the dynamic performance is mainly determined by the controller proportional and integral gains, integrator limiters and voltage feedforward signals. As all these variables/parameters are practically bounded, both analog

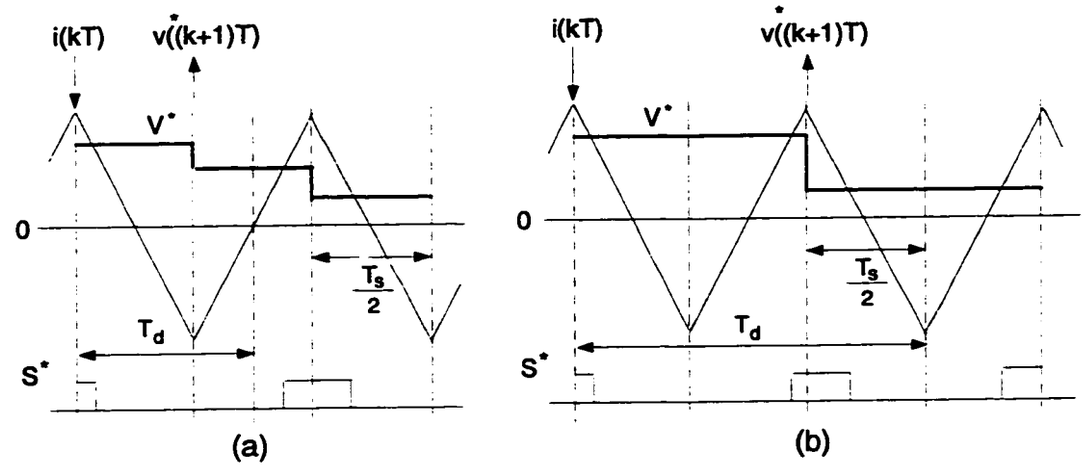

Figure 5.5: Synchronously sampled digital current regulator reference, carrier, and gate signal waveforms, and the delay times: (a): Asymmetric PWM with twice per carrier sampling and PWM write-out rate, (b): Symmetric PWM with once per carrier sampling and PWM write-out rate.

and digital current regulators have finite bandwidth.

The current controller proportional and integral gains are determined by the regulator bandwidth and overshoot requirements. With these performance criteria defined, the controller gains can be easily established analytically or experimentally. Since most PWM-VSI drive applications are electric motors or AC voltage sources (both with R-L-E circuit characteristics), the pole zero cancellation method (also termed as the technical optimum method) provides the best controller performance. The cross-coupling decoupling signals (W*L*I terms) are calculated from the estimated motor parameters, and reference/measured currents. The voltage feedforward terms also require the measured/estimated load parameters/variables. The controller integrator limits are selected as high

as possible so that during a significant transient the controller linearity is retained. With all the components designed carefully, the SFCR performance meets the bandwidth and overshoot requirements of most industrial and motion control applications. With zero steady state error and rapid dynamic performance from zero frequency to the maximum operating frequency, SFCR provides high performance three phase current regulation. Further advanced techniques to obtain high performance from the SFCR (in particular in the high frequency operating region) are discussed in detail in [50]. The performance, however, is only valid in the linear modulation region. Once outside the modulator voltage linearity limit, the current regulator performance experiences significant performance degradation.

The overmodulation region behavior of current controlled drives is complex. In this region the interaction between the control loops (current/speed etc.) and the modulator may result in additional dynamics when compared to the open loop $\frac{V}{f}$ controlled drives. With the modulator being the final element in the cascaded control system, its phase and magnitude error characteristics strongly influence the drive performance. Since the duration of the transients can be smaller than the minimum fundamental cycle (the maximum operating frequency), the per fundamental cycle modulator characteristics (voltage gain) are insufficient and may not be appropriate for the investigation of the dynamic overmodulation behavior of a modulator. The per carrier cycle voltage linearity characteristics are appropriate. Therefore characterization of the modulator reference voltage-output voltage phase and magnitude relations is vital for the

current regulator overmodulation region performance study. The next section reviews the direct digital technique overmodulation magnitude phase relations and then establishes the overmodulation characteristics for the modern triangle intersection PWM methods. Following, the dynamic overmodulation behavior of an AC motor drive is investigated in detail. Finally, the theory is supported with detailed computer simulations and laboratory results.

5.3 Direct Digital PWM Dynamic Overmodulation

Figure 3.4 of Chapter 3 indicates the fundamental component voltage linearity of all the direct digital PWM methods is bounded by the circle which touches the inverter voltage hexagon. The per carrier cycle voltage linearity boundary is the hexagon. However, once the reference voltage vector tip point lies outside the hexagon, (3.13) yields a negative time length, hence an inevitable per carrier cycle volt-seconds error. A voltage vector on the hexagon boundary (the modified reference voltage vector) must be selected and at least one back step has to be taken to re-calculate the vector time lengths that generate the modified reference voltage vector. Shown in Fig. 5.6, the three popular modified reference vector choices are the Minimum Magnitude Error PWM (MMEPWM) method (also called one-step-optimal method) [131, 181], the Minimum Phase Error PWM (MPEPWM) method [58], and the Dynamic Field Weakening PWM

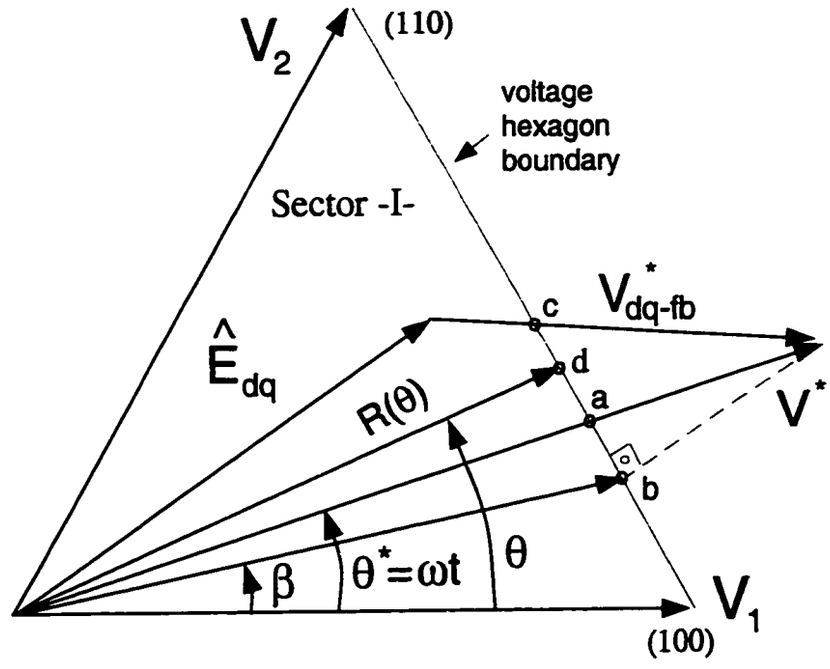

Figure 5.6: Vector space illustration of the popular direct digital PWM technique dynamic overmodulation methods. a: minimum phase error method, b: minimum magnitude error method, c: dynamic field weakening method.

(DFWPWM) method [88, 182]. These methods were evaluated in [88, 182] for induction motor and AC Permanent Magnet (PM) motor drives. The superiority of the last method and the implementation simplicity of the second were shown. The implementation of the first and the third methods is involved (significant computational burden) and the performance of the first is moderate.

In the triangle intersection PWM technique, unlike the direct digital PWM technique, the time lengths of the inverter states are not explicitly calculated: they are an end result of the comparison between the triangular carrier wave

and the modulation waves. Therefore, an overmodulation condition can be detected when the modulation wave signal magnitude exceeds the triangle wave magnitude and switching ceases. The overmodulation intervals, i.e. the time intervals where the reference voltage vectors belong outside the modulator voltage linearity boundaries, exhibit unique voltage error characteristics in each triangle intersection PWM method. These characteristics will be analyzed in detail in the following section.

5.4 Triangle Intersection PWM Dynamic Overmodulation Characteristics

When illustrated in the space vector diagram, the fundamental component voltage linearity boundaries of the triangle intersection PWM methods form circles. As Fig. 5.7 illustrates, the circle radius is smallest in SPWM. SVPWM and all the discussed DPWM methods are linear within the largest circle that fits inside the inverter hexagon. Not shown in the figure, the THIPWM1/6 and THIPWM1/4 methods have linearity circles smaller than the SVPWM circle and larger than the SPWM circle. The THIPWM1/4 circle is smaller than the THIPWM1/6 circle (the diameters can be calculated from the fundamental component linearity modulation indices calculated in the previous chapter). Outside the fundamental component voltage linearity boundaries (circles) the per carrier cycle modulator phase and magnitude characteristics are not well

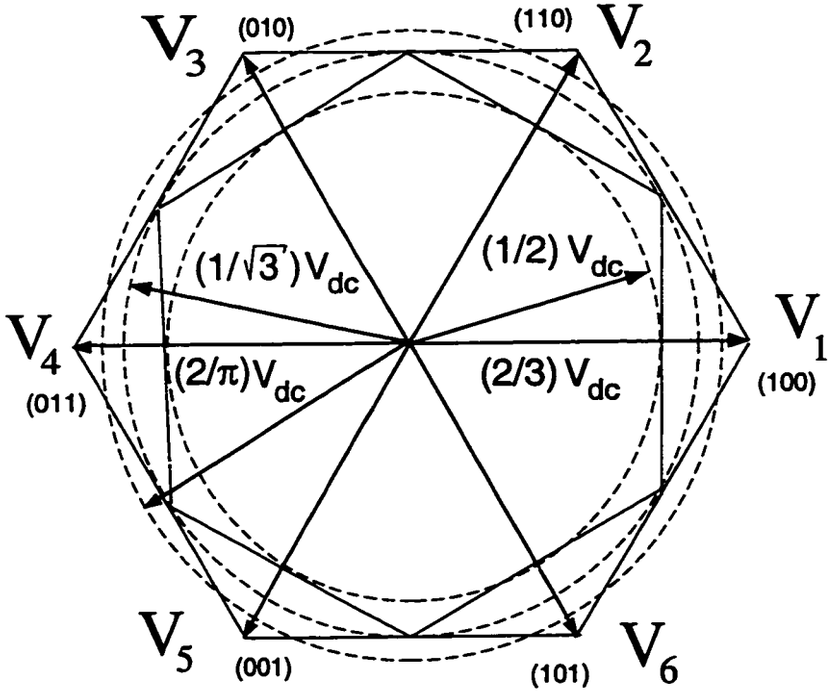

Figure 5.7: Vector space illustration of the PWM inverter voltage linearity limits. The circles illustrate the fundamental component voltage linearity limits.

understood and not reported in the literature.

In the triangle intersection PWM technique, a reference voltage outside the triangle wave boundaries $\pm\frac{V_{dc}}{2}$ can not be generated. Modeling this saturation, dynamic overmodulation characteristics (per carrier cycle phase and magnitude characteristics) of any triangle intersection PWM method can be obtained [65]. With this approach, by passing the reference modulation waves through the limiters shown in Figure 5.8 and employing transformation (3.1), as indicated in Fig. 5.6, for any reference voltage vector $V_{dq}^{*} = \mid V_{dq}^{*} \mid e^{j\theta^{*}}$, an output voltage vector $V_{dq} = \mid R(\theta) \mid e^{j\theta}$ is produced. Since the zero sequence signals of all the popular modulation methods are symmetric and periodic, characterizing the

first sector of the hexagon is sufficient. Note the output voltage vector is the time average value of a sequence of the inverter output voltage vectors applied over a carrier cycle. Time domain waveforms of the d and q axis output voltages can be utilized in calculating the average value of the output voltage vector and its phase relations.

In the SVPWM method and all the discussed DPWM methods, the zero state partitioning may take a zero value, a half, or a unity value. With such zero state partitioning values, the per carrier cycle linearity boundaries of these methods are equal to the linearity boundary of direct digital PWM methods. Therefore, in SVPWM, DPWM0, DPWM1, DPWM2, DPWM3, DPWMMAX, DPWMMIN, and GDPWM the voltage linearity boundary is the inverter voltage hexagon. Since in these methods the hexagon boundaries are known, characterizing the angular relations, $\theta = f(\theta^*, M_i^*)$ is sufficient. For example, in the first sector $R(\theta)$ can be calculated by the following.

$$| v_{dq} | = R(\theta) = \frac{V_{dc}}{\sqrt{3}\sin(\theta + \frac{\pi}{3})} \tag{5.1}$$

The dynamic overmodulation characteristics of the triangle intersection PWM methods shown in Fig. 3.7 have been analyzed with the above approach. The characteristics of SVPWM and all the discussed DPWM methods are summarized in the following, while the SPWM, THIPWM1/4 and THIPWM1/6 characteristics are more involved and will be discussed at a later stage.

In SVPWM, when the modulation signal becomes larger than the saturation

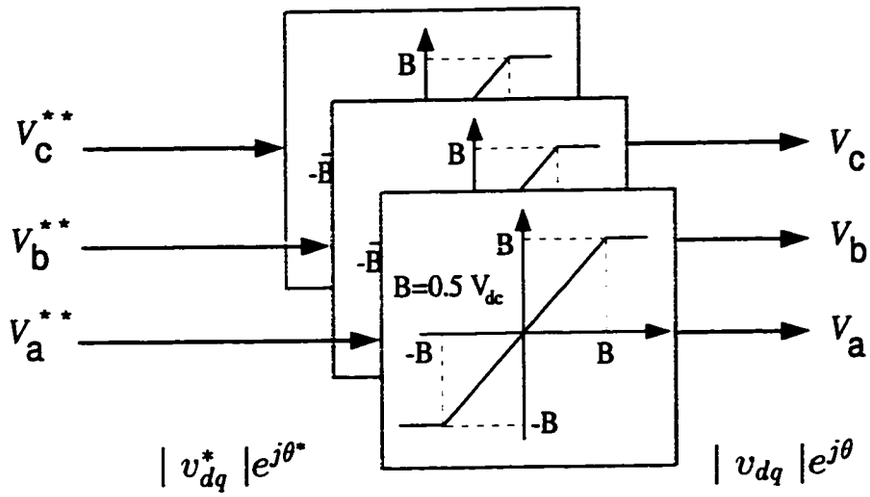

Figure 5.8: The saturation block diagram of the triangle intersection PWM methods.

boundaries $\pm\frac{V_{dc}}{2}$, the saturated modulation signals can be transformed by (3.1) and in the first segment ($0 \leq \theta^* \leq \frac{\pi}{3}$), the output voltage vector angle can be calculated in the following.

$$\theta_{SVPWM} = \arctan\left(\sqrt{3}\frac{1+\frac{6}{\pi}M_i^* cos(\theta^* - \frac{2\pi}{3})}{3-\frac{6}{\pi}M_i^* cos(\theta^* - \frac{2\pi}{3})}\right) \tag{5.2}$$

A software which graphically overlays the MMEPWM, and MPEPWM, and triangle intersection SVPWM dynamic overmodulation reference-output voltage vector trajectories indicated a surprising result: The MMEPWM and SVPWM vectors are exactly the same. Calculated by projecting the tip point of the reference voltage vector on the hexagon side (point b in Fig. 5.6), the analytical angle relation of MMEPWM yields the following formula.

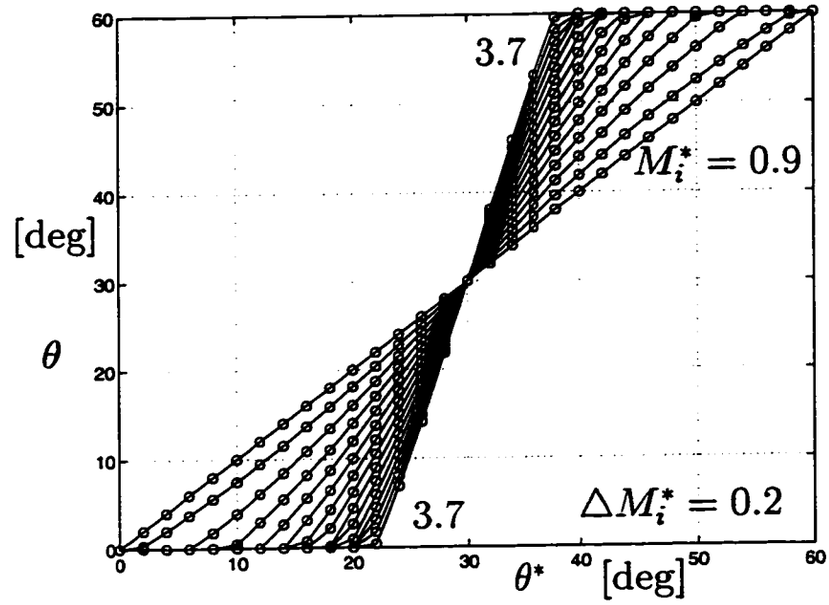

Figure 5.9: SVPWM (-) and MMEPWM (o) $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

$$\theta_{MMEPWM} = \beta = -\frac{\pi}{3} + \arctan\left(\frac{\pi}{2\sqrt{3}M_i^* cos(\theta^* + \frac{\pi}{3})}\right) \tag{5.3}$$

Although (5.2) and (5.3) are different in form, their numerical evaluation which is shown in Fig. 5.9 reveals the fact that their performance is the same. This result indicates when implemented with the triangle intersection technique, the SVPWM method provides very fast (one step optimal) dynamic overmodulation response. The MMEPWM methods employed in practice are complex and computationally involved [131, 181]. The triangle intersection SVPWM, however, can be implemented in hardware or software with minimum complexity.

In the SVPWM method two modulation signals always have the same magnitude and opposite polarity. Furthermore, these phases always have larger magnitude than the third. Therefore, in the overmodulation at least two modulation signals saturate simultaneously. In addition to aiding the explanation of the phase lag (in the first half of the first inverter hexagon segment) and phase lead (in the second), these characteristics appear to be the reason for the one-step-optimal overmodulation behavior. Perhaps, this characteristic can be proven by rigorous algebra. However, with the numerical results being satisfactory and illustrating the importance of this characteristic, no serious attempt is made towards a mathematical proof of this claim.

The DPWM methods of which their waveforms were shown in Fig. 3.7 have found application in high performance current controlled drives due to their low switching loss characteristics and low current ripple characteristics [62, 68]. Dynamic overmodulation characteristics of these modulators can be modeled depending on their zero state partitioning which was summarized in Fig. 3.9. A zero state partitioning of $\zeta_0 = 1$, which corresponds to DPWM0 and DPWMMIN in the first hexagon sector, provides the following phase relations.

$$\theta_{DPWM0} = \arctan\left(\frac{\frac{6}{\pi} M_i^* \sin\theta^*}{2 - \frac{2\sqrt{3}}{\pi} M_i^* \sin\theta^*}\right) \tag{5.4}$$

For DPWM2 and DPWMMAX the zero state partitioning in the first hexagon sector is zero ($\zeta_0 = 0$) and the dynamic overmodulation angle relations are calculated as follows.

$$\theta_{DPWM2} = \arctan\left(\sqrt{3}\frac{1 - \frac{2\sqrt{3}}{\pi}M_i^* \cos\left(\theta^* + \frac{\pi}{6}\right)}{1 + \frac{2\sqrt{3}}{\pi}M_i^* \cos\left(\theta^* + \frac{\pi}{6}\right)}\right) \tag{5.5}$$

Since in DPWM1 the zero state partitioning is $\zeta_0 = 0$ for $0 \leq \theta^* \leq \frac{\pi}{6}$ and $\zeta_0 = 1$ for $\frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3}$, the overmodulation phase relations are calculated from (5.4) and (5.5) in the following.

$$\theta_{\text{DPWM1}} = \begin{cases} \theta_{DPWM2} & 0 \leq \theta^* \leq \frac{\pi}{6} \\ \theta_{DPWM0} & \frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3} \end{cases} \tag{5.6}$$

The dynamic overmodulation characteristics of DPWM3 are found with the same approach in the following.

$$\theta_{\text{DPWM3}} = \begin{cases} \theta_{DPWM0} & 0 \leq \theta^* \leq \frac{\pi}{6} \\ \theta_{DPWM2} & \frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3} \end{cases} \tag{5.7}$$

The following phase error, $\triangle\theta$, definition aids the discussion on the modulator dynamic overmodulation characteristics.

$$\triangle\theta = \theta^* - \theta \tag{5.8}$$

The reference and output voltage vector phase relations of DPWM0, DPWM1, DPWM2, and DPWM3 are shown in Figures 5.10, 5.11, 5.12, and 5.13 for various M_i^* values. In DPWM0 the output vector always leads the reference voltage

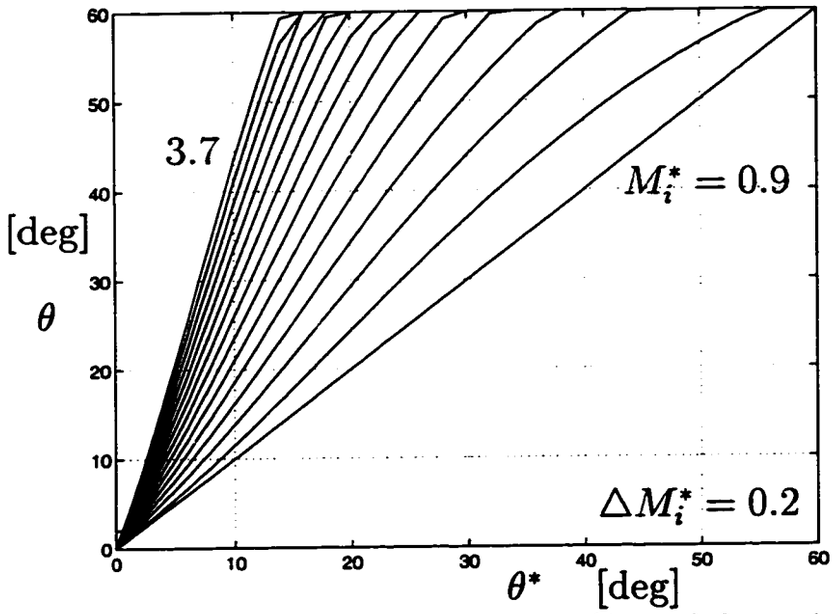

Figure 5.10: DPWM0 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 1$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

vector while for DPWM2 the opposite is true. Since DPWM1 is a combination of DPWM0 and DPWM2, in this case the output vector lags the reference for the first 30° segment of the sector and leads in the following 30° segment. Note the phase error of SVPWM also changes polarity at 30°, however the change is smoother and the error magnitude is smaller. As Fig. 5.13 illustrates, DPWM3 follows the opposite pattern of DPWM1 and both in DPWM1 and DPWM3 the output voltage vector experiences a jump near the midsection of the hexagon sector (avoiding the vector at $\frac{\pi}{6}$). For all the discussed methods the behavior in the first 60° is repeated periodically in the remainder of the sectors. In all the methods, an increase in the modulation index results in phase error increase and the error is the largest in DPWM1.

In the SPWM, THIPWM1/4 and THIPWM1/6 methods, the modulator

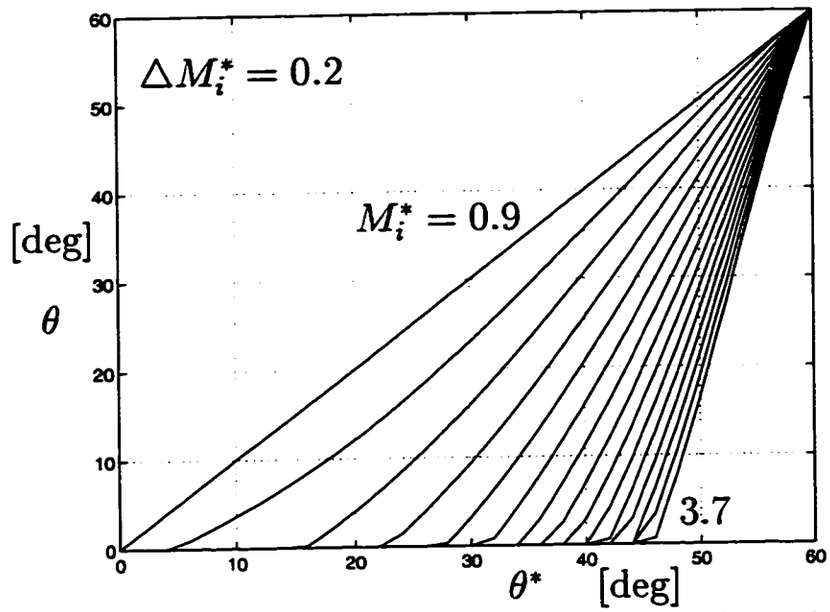

Figure 5.11: DPWM2 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 0$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

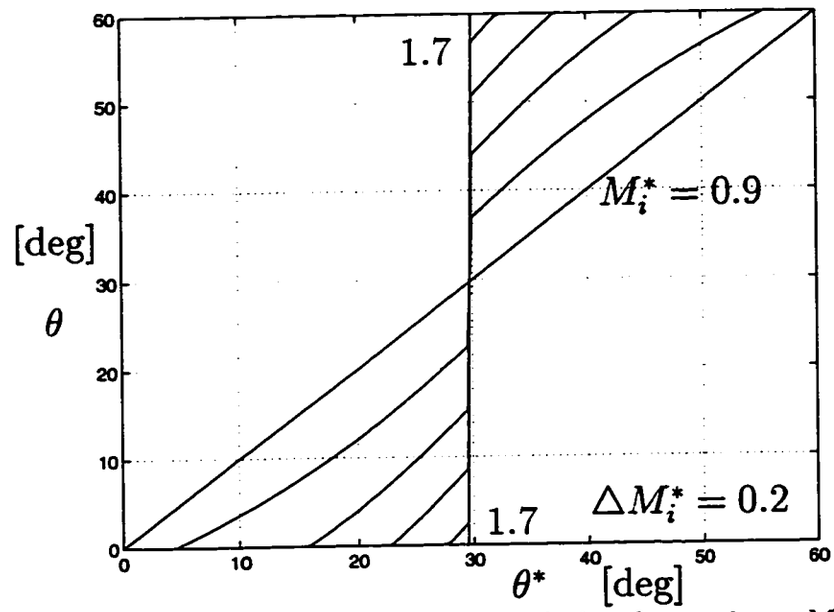

Figure 5.12: DPWM1 $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

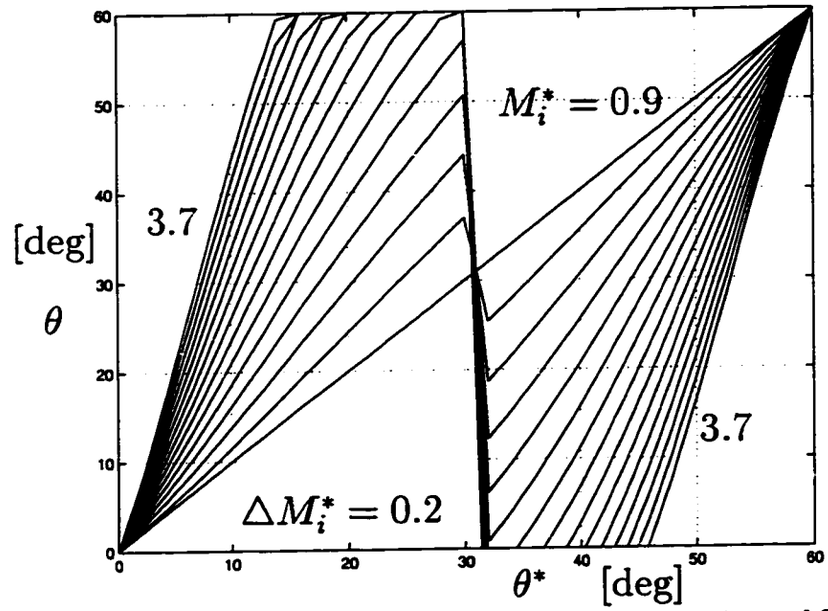

Figure 5.13: DPWM3 $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

phase and magnitude relations are more involved. The per carrier cycle voltage linearity boundaries of these modulators are smaller than the inverter hexagon. These boundaries can be analytically calculated and graphically illustrated. Due to the 60° vector space periodicity, illustration of the boundaries in the first hexagon segment is sufficient. For example, in SPWM the linearity boundaries can be calculated in the following. In the $0° \leq \theta \leq 30°$ segment, phase "a" modulation wave has the largest magnitude. Equating the voltage linearity limit $\frac{V_{dc}}{2}$ to this modulation signal, the voltage linearity boundaries in this region can be easily calculated. In the $30° \leq \theta \leq 60°$ segment, phase "c" has the largest magnitude and determines the linearity boundaries. These relations are summarized in the following.

$$M^{L}_{iSPWM} = \begin{cases} \frac{\pi}{4\cos\theta^*} & 0 \le \theta^* \le \frac{\pi}{6} \\ -\frac{\pi}{4\cos(\theta^*+\frac{2\pi}{3})} & \frac{\pi}{6} \le \theta^* \le \frac{\pi}{3} \end{cases} \tag{5.9}$$

In the THIPWM1/4 and THIPWM1/6 methods the linearity boundaries are calculated in a similar approach, and the results are as follows.

$$M^{L}_{iTHIPWM1/4} = \begin{cases} -\frac{\pi}{4(\cos(\theta^*+\frac{2\pi}{3})-\frac{1}{4}\cos 3\theta^*)} & 0 \le \theta^* \le \frac{\pi}{6} \\ \frac{\pi}{4(\cos\theta^*-\frac{1}{4}\cos 3\theta^*)} & \frac{\pi}{6} \le \theta^* \le \frac{\pi}{3} \end{cases} \tag{5.10}$$

$$M^{L}_{iTHIPWM1/6} = \begin{cases} -\frac{\pi}{4(\cos(\theta^*+\frac{2\pi}{3})-\frac{1}{6}\cos 3\theta^*)} & 0 \le \theta^* \le \frac{\pi}{6} \\ \frac{\pi}{4(\cos\theta^*-\frac{1}{6}\cos 3\theta^*)} & \frac{\pi}{6} \le \theta^* \le \frac{\pi}{3} \end{cases} \tag{5.11}$$

Evaluating the above formulas, the per carrier cycle voltage linearity boundaries of these methods can be found. Figure 5.14 illustrates these boundaries in detail (only the first quadrant of the vector space shown). The internal hexagon is the voltage linearity boundary of SPWM method. The THIPWM1/6 method has elliptic boundaries, while the THIPWM1/4 linearity boundaries resemble the shape of a star with twelve edges. It is apparent from the diagram the per carrier cycle voltage linearity characteristics of these methods are inferior to SVPWM and the DPWM methods. Therefore, SVPWM and DPWM methods are preferred in high performance drives. For the sake of completeness, the non-linear phase and magnitude relations of SPWM and THIPWM methods will be discussed in the following.

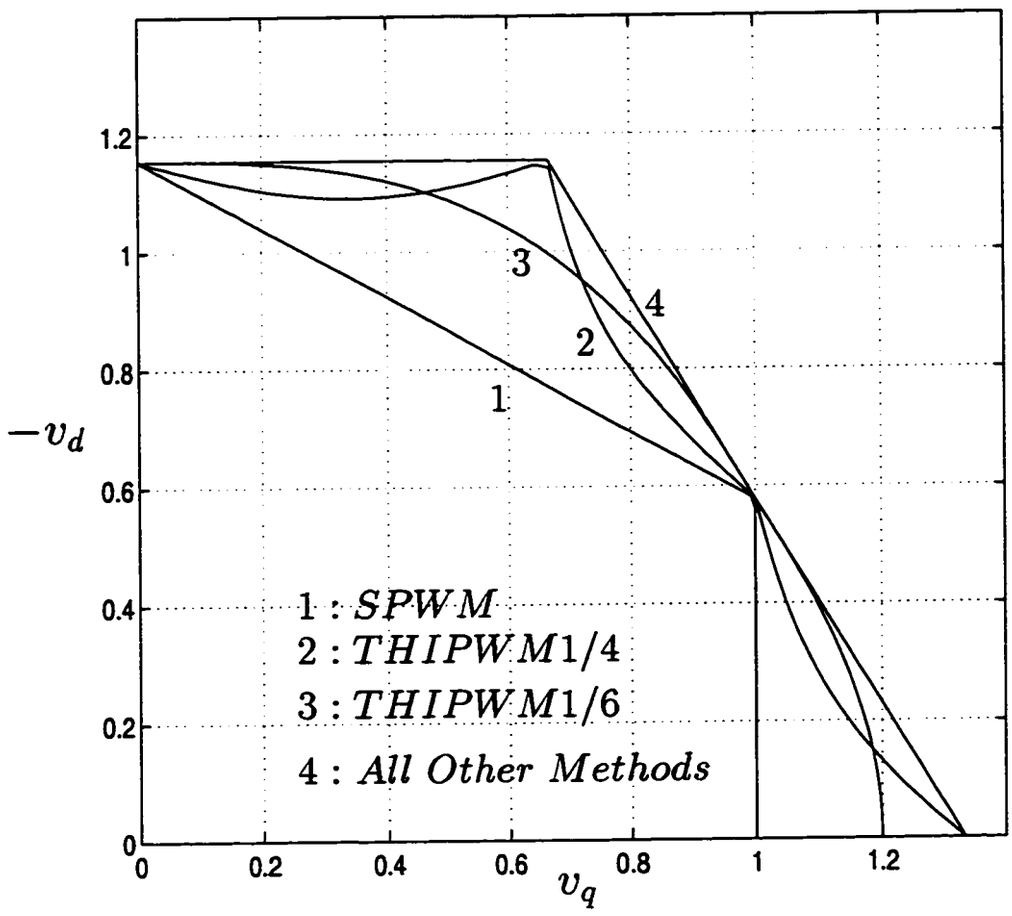

Figure 5.14: Vector space illustration of the modulator per carrier cycle voltage linearity limits. All voltage vectors are normalized to $\frac{V_{dc}}{2}$.

In the SVPWM method, in the overmodulation intervals the modulation waveforms of at least two phases saturate simultaneously. In the DPWM methods, in the linear modulation region one of the three modulation signals clamped to the positive or negative peak of the triangle. In the overmodulation intervals at least one more modulation signal is saturated simultaneously. Therefore, in SVPWM and the DPWM methods overmodulation implies saturation of two phases or three phases. However, in the SPWM and THIPWM methods, a mode with only one phase saturation also exists. For each method and each mode a unique overmodulation phase and magnitude formula exists.

In SPWM, as the modulation signal magnitude increases and becomes larger than $\frac{V_{dc}}{2}$ the one phase saturation mode begins. Further increase in the reference voltage magnitude results in the two phase saturation mode. As the magnitude is further increased the three phase saturation mode is reached. In all the modes the output voltage magnitude is always smaller than the reference voltage magnitude. However, the phase relations are not clear and an analytical investigation is required.

With the reference modulation index defined as a parameter, the dynamic overmodulation phase relations of SPWM can be characterized in three regions. With the SPWM waveforms having space symmetry in a hexagon segment (symmetry about the 30° line), only the first 30° segment need be modeled. The first region covers the $\frac{\pi}{4} \leq M_i^* \leq \frac{\pi}{2\sqrt{3}}$ range and in this region only one phase may saturate (in the first half of the first sector phase "a" saturates). In this region

the phase relations of SPWM are as follows.

$$\theta_{\text{SPWM1}} = \begin{cases} \arctan\left(\frac{3M_i^* \sin\theta}{0.5\pi + M_i^* \cos\theta}\right) & 0 \le \theta^* \le \theta_{b1} \\ \theta^* & \theta_{b1} \le \theta^* \le \frac{\pi}{6} \end{cases} \tag{5.12}$$

$$\theta_{b1} = \arccos\left(\frac{\pi}{4M_i^*}\right) \tag{5.13}$$

The second region covers the $\frac{\pi}{2\sqrt{3}} \le M_i^* \le \frac{\pi}{2}$ range and in this region one or two phases may simultaneously saturate. The relations are calculated in the following.

$$\theta_{\text{SPWM2}} = \begin{cases} \arctan\left(\frac{3M_i^* \sin\theta}{0.5\pi + M_i^* \cos\theta}\right) & 0 \le \theta^* \le \theta_{b2} \\ \arctan\left(\frac{\sqrt{3}(M_i^* \cos(\theta^* - \frac{2\pi}{3}) + \frac{\pi}{4})}{(\frac{3\pi}{4} - M_i^* \cos(\theta^* - \frac{2\pi}{3}))}\right) & \theta_{b2} \le \theta^* \le \frac{\pi}{6} \end{cases} \tag{5.14}$$

$$\theta_{b2} = -\frac{2\pi}{3} + \arccos\left(-\frac{\pi}{4M_i^*}\right) \tag{5.15}$$

The third region covers the $M_i^* \ge \frac{\pi}{2}$ range and in this region two or three phases may simultaneously saturate. The equations are as follows.

$$\theta_{\text{SPWM3}} = \begin{cases} 0 & 0 \le \theta^* \le \theta_{b3} \\ \arctan\left(\frac{\sqrt{3}(M_i^* \cos(\theta^* - \frac{2\pi}{3}) + \frac{\pi}{4})}{(\frac{3\pi}{4} - M_i^* \cos(\theta^* - \frac{2\pi}{3}))}\right) & \theta_{b3} \le \theta^* \le \frac{\pi}{6} \end{cases} \tag{5.16}$$

$$\theta_{b3} = \frac{2\pi}{3} + \arccos\left(-\frac{\pi}{4M_i^*}\right) \tag{5.17}$$

Figure 5.15 illustrates the dynamic overmodulation phase relations of SPWM for various modulation indices. As Fig. 5.15(a) indicates, in the first region, the output vector leads the reference vector in the first 30° segment of the hexagon, and lags in the second 30° segment. However, in this region the phase error is small. As Fig. 5.15(b) indicates, in the second region, the phase error polarity is the same as in the first region. However, the phase error increasingly becomes large. Further increase of the modulation index results in error reduction and as the phase error approaches zero, this region expires. As Fig. 5.15(c) indicates, in the third region, the phase error becomes substantial and in the first 30° segment a lag, in the second a lead occurs. Since at high modulation index values the SPWM and SVPWM modulation signals are similar, in the third region the SPWM phase error behavior approaches the SVPWM phase error behavior. With its phase and magnitude errors being significantly larger than the SVPWM and DPWM method cases, the SPWM method clearly exhibits poor dynamic overmodulation characteristics throughout its overmodulation region.

The phase and magnitude relations of the THIPWM methods can be calculated in a similar manner to the SPWM and SVPWM methods. With its waveform being quite similar to SVPWM, the THIPWM1/6 method has similar dynamic overmodulation characteristics to SVPWM. However, as the fundamental component voltage gain comparisons, and the per carrier cycle voltage linearity boundary comparisons indicated, THIPWM1/6 is slightly inferior to SVPWM and is more difficult to implement. In the region that is outside the THIPWM1/6 ellipse and inside the inverter voltage hexagon the THIPWM1/6

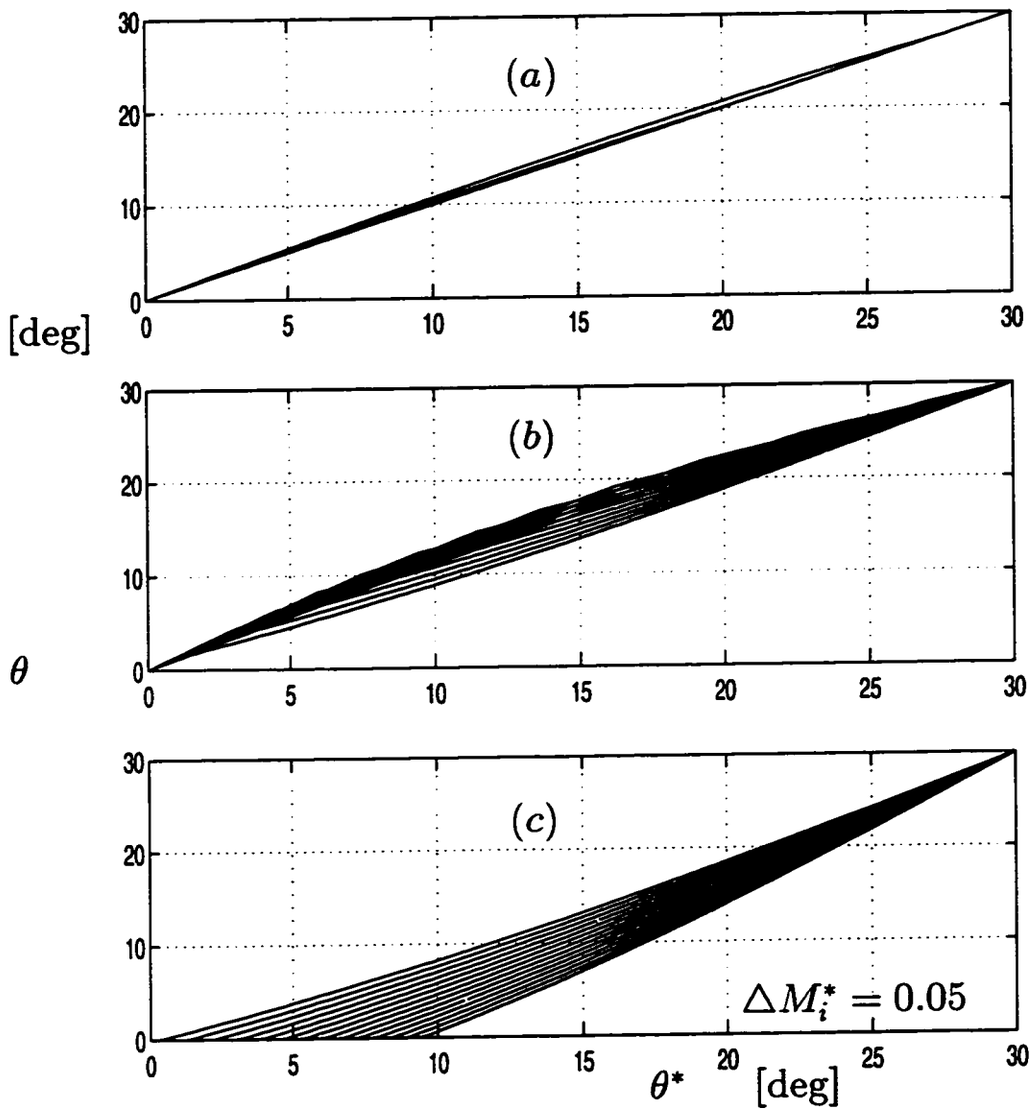

Figure 5.15: SPWM $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.785 and increments with 0.05 units.

has some small phase and magnitude error while SVPWM is linear. Also, outside the hexagon, SVPWM is one step optimal while the THIPWM1/6 is not exactly so. The THIPWM1/4 method has smaller linearity region and its characteristics are inferior to SVPWM and THIPWM1/6. The phase relations of the THIPWM methods will be omitted.

In practice, the theoretical modulator linearity boundaries are further reduced due to the inverter blanking time and/or minimum pulse width constraint of the inverter drives. In the previous chapter it was shown these constraints can strongly affect the fundamental component voltage gain of a modulator. The blanking time and minimum pulse width constraints also affect the dynamic overmodulation characteristics of a modulator. If a narrow voltage pulse is eliminated, the output voltage magnitude becomes larger than the theoretical value and the phase error increases. The phase and magnitude errors are dependent on the minimum pulse width to the carrier cycle ratio and increase with it. Analytical modeling of these second order effects will not be included in this work.

Since the phase error completely determines the dynamic overmodulation performance of a modulator, the $\theta = f(\theta^*)$ (or $\triangle\theta = f(\theta^*)$)relations are the main characteristics in predicting the modulator dependent drive dynamic behavior. The next section discusses the influence of these characteristics on the drive behavior.

5.5 Drive Dynamic Overmodulation Behavior

The dynamic overmodulation performance of an AC motor drive or an AC line connected PWM-VSI is determined by the modulator phase error characteristics, the drive control algorithm, and load characteristics. In the following we first discuss the SFCR design, then investigate the system (SFCR-modulator-load) level overmodulation behavior.

Since the conventional SFCR design assumes modulator linearity, in the overmodulation region significant delays and overshoot can result. The oscillation magnitude may become so large that the drive may become unstable and immediately disabled due to an overcurrent fault. To minimize the performance degradation, antiwindup controllers which bound the integrator outputs of the PI controllers are employed, and selecting a proper integrator limit value is vital in maximizing the dynamic performance [9]. The theory of advanced antiwindup controllers is involved and will be omitted from this work. A relatively simple approach that is based on recalculating the SFCR integrator variables from the output voltage vectors on the modulator voltage linearity boundary [88, 182] has been found adequate for the purpose of the study in this chapter. In this approach, shown in Fig. 5.16, the SFCR discrete time signal flow diagram antiwindup limiters are only activated in the overmodulation region. During the (n)'th carrier cycle, the (n+1)'th cycle reference voltages v_{qe}^* and v_{de}^* are calculated and transformed to stationary frame *"abc"* variables. In the modulator block, a zero sequence signal is injected to the *"abc"* voltages to form

the modulation signals. These signals are passed through the saturation limits of Figure 5.8 and rotated to the synchronous frame to predict the (n+1)'th cycle output voltages v_{qe} and v_{de}. If the reference and output signals are different (indicating a dynamic overmodulation condition), then the antiwindup signals reset the integrators to the boundary values ib_{qe} and ib_{de} (signal flow through "NL"), otherwise the linear modulation operating mode resumes (signal flow through "L"). In the overmodulation region, the "q" and "d" channel integrators are reset to $v_{qe} - v^*_{qeff}$ and $v_{de} - v^*_{deff}$ values so that in the following carrier cycle the calculated reference voltage vector is close to the hexagon boundary. With this approach, if the error reverses polarity, the linearity region is immediately re-entered. If the error is zero or its polarity does not change, then the reference voltage remains near the modulator linearity boundary, however may be at a different point. This intuitive method is apparently simple and has implementation advantage over computationally involved methods.

Along with the modulator and SFCR with antiwindup, the inverter DC voltage source and AC load characteristics define the system overmodulation behavior. Perhaps the most intuitive explanation of the drive behavior is to consider the effect of the phase error on the synchronous frame reference and output voltage vector "d" and "q" components. Depending on the modulator phase error value, during a dynamic overmodulation condition the inverter output voltage vector may lead or lag the reference voltage vector, and the lead and lag conditions result in different "de" and "qe" axis voltages. As a result the drift of the "de" and "qe" axis currents from the reference values may be

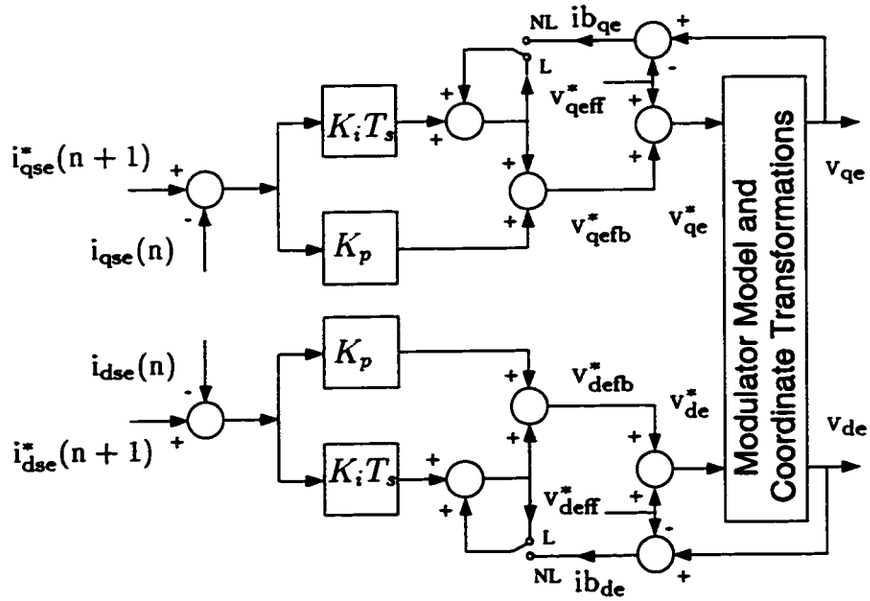

Figure 5.16: Discrete time signal flow diagram of the synchronous frame PI current controller with anti-windup.

quite different in the lagging and leading conditions. Therefore, the currents drift from the reference values according to the modulator phase error characteristics. For example, with SVPWM the drift always yields the smallest current error vector every carrier cycle and therefore SVPWM is suitable for applications where the inverter AC side current error minimization is of prime interest. However, in most cascade controlled motion control systems (from the outmost to the innermost loops, position-speed-current control loops form the cascade control system) the primary goal is to maintain the motion quality. A dynamic overmodulation condition implies an increase in the demanded torque and torque maximization is the prime concern. Since the torque maximization criteria and current error minimization criteria may require two different voltage vectors, the influence of the modulator phase error on the drive motor

torque must be clearly understood. Therefore, the motor dynamic behavior has to be considered. In this work mainly the induction motor behavior will be discussed. However, the dynamic overmodulation behavior of other motor types and utility interfaced PWM-VSI have similar characteristics and the results of this investigation can be interpreted for such applications.

To establish an intuitive background for the drive dynamic overmodulation study, the steady state behavior of the Rotor Flux Oriented (RFO) field oriented induction motor will be briefly discussed first. Then the deviation from steady state and entrance to the overmodulation region will be considered. As shown in Fig. 5.17, during steady state, the reference and output voltages of the RFO-IFOC drive are in phase and they have equal magnitude. The inverter output voltage balances the motor emf and the voltage drop across the equivalent impedance [145]. Since the EMF is on the qe axis and it increases with speed, at higher speeds the qe axis reference voltage becomes significantly larger than the de axis reference voltage. Therefore, as the speed increases the de axis voltage margin decreases and it becomes increasingly difficult to maintain/build the torque producing current. In field/flux weakened AC machines, the flux producing component of the stator current is decreased in a manner to provide a sufficient de axis voltage for torque producing current regulation [99, 100, 180]. As a result, overmodulation is avoided as much as possible. However, field weakened drives with rapid acceleration requirements and including such drives most current controlled motor drives under DC bus and load torque

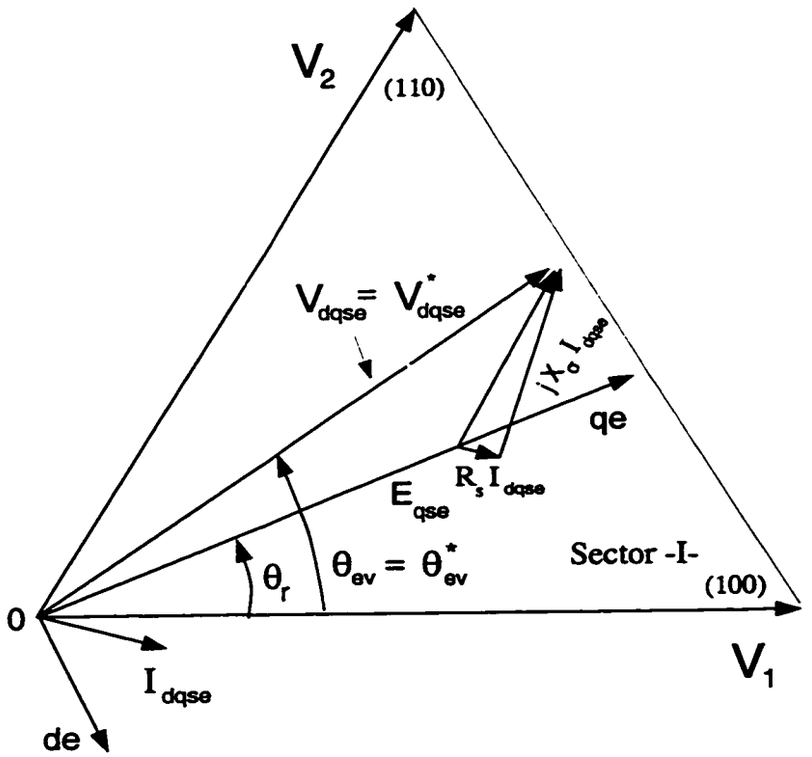

Figure 5.17: Synchronous frame rotor flux oriented induction motor voltage vector diagram illustrated along with the inverter voltage vector diagram.

disturbance conditions enter the overmodulation region and performance degradation results.

As shown in Fig. 5.18, the rotor flux oriented synchronous frame induction motor overmodulation voltage vector diagram indicates during overmodulation condition the "*qe*" and "*de*" axis stator voltages are different from the reference values and as a result the "*qe*" and "*de*" axis currents drift from their reference values. Thus, the motor torque linearity is lost ($T_e = K_{te}(i_{qse}\lambda_{dse} - i_{dse}\lambda_{qse})$) and motion quality degrades. For example, if v^*_{dqse}, v_{dqse} and the "*qe*" axis are

in the first 30° segment of a hexagon sector, and v_{dqse} lags v^*_{dqse}, then the overmodulation condition results in a smaller v_{dse} and larger v_{qse} compared to the phase error lead condition. As a result i_{qse} becomes larger and i_{dse} smaller than the lead case. Although this dynamic field weakening condition may transiently increase the drive torque, motion quality degrades due to the loss of torque linearity. As the current regulation becomes poor and the field orientation condition is lost, the rotor flux varies and dynamics are excited. Beyond this point the dynamics can not be described with the steady state equivalent circuit of the motor drive; therefore a full dynamic model is required for a detailed investigation. However, the above discussed simple model illustrates the importance of the modulator phase error and also aids in explaining the influence of the phase lag and lead conditions. The most important conclusion of this intuitive example is that with a strong dynamic field weakening condition or the opposite effect the drive performance may significantly degrade. Therefore, the modulator phase error must be controlled in a manner to maintain good drive performance as much as possible.

Triangle intersection PWM methods exhibit unique phase error characteristics; therefore, it is expected that a drive perform differently with different modulators. Since the current controller antiwindup limiters bound the reference voltage magnitude (i.e. M^*_i), the phase error magnitude is also practically bounded. With the proportional and integral gains of the current controller selected according to the technical optimum criteria, the dynamic overmodulation

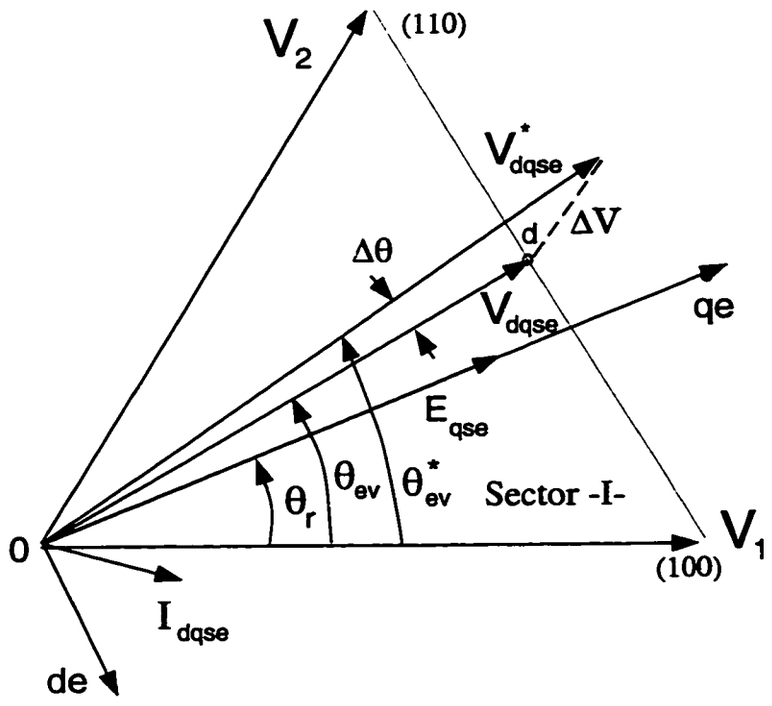

Figure 5.18: Synchronous frame rotor flux oriented induction motor voltage vector diagram representing an overmodulation condition.

conditions can result in reference voltages vectors with a magnitude comparable to the inverter hexagon boundaries. Therefore, the phase errors are also limited by the antiwindups and this limits strong dynamic transients and oscillations. Thus, the antiwindup limiters are essential in avoiding unwanted dynamics. However, the antiwindup limiters may not be sufficient to obtain high performance (any motor torque is a strong function of the phase error and even a small phase error may result in a strong dynamic condition) and a system level study is required. In the following section, detailed induction motor drive simulations address these performance issues.

5.6 Computer Simulations

The theoretical modulator characteristic study has been supported by detailed induction motor drive simulations. A 5 HP, 1745 RPM, 460 V, 6.9 A, 4 pole induction motor with the lumped equivalent circuit parameters of $r_s = 1.97$ Ohm, $r_r = 1.73$ Ohm, $L_{ls} = L_{lr} = 11.2$ mH, $L_m = 275.6$ mH is driven through a PWM-VSI drive. The inverter DC bus voltage is 620 V (stiff DC bus voltage is assumed), and the carrier frequency is 5 kHz. The drive employs an indirect field orientation control algorithm [145], and a fully digital synchronous frame PI current controller with voltage feedforward and antiwindup provides high performance current regulation. The digital current controller employs the synchronous sampling technique with 5 kHz sampling rate (once per carrier cycle feedback current sampling and once per carrier cycle PWM signal

write-out). The current controller bandwidth is 250 Hz. The rated synchronous frame stator "d" and "q" axis currents are $I_{dseR} = 3.38$ A, and $I_{qseR} = 9.12$ A. The drive speed is controlled with a digital PI controller with antiwindup (the previously described antiwindup method) and the antiwindup limit equals the inverter maximum current capability (150 % rated motor current). The speed controller sampling rate is 1 kHz and the speed loop has a 25 Hz (electrical) bandwidth. The drive total inertia is $J_m = 0.05 kgm^2$.

The computer simulation of Fig. 5.19 illustrates the drive linear modulation range dynamic performance with SVPWM. While the drive is operating at 1000 RPM and no load, a transient condition is generated with a speed reference change and application of a load torque. A speed ramp command, ω_r^*, at t=0.65 [s] increases the speed from 1000 RPM to 1050 RPM in 12 ms, and the load torque, T_L, increases at t=0.71 [s] from zero to 25% of the rated motor torque. As the figure illustrates, both the speed regulation and torque disturbance rejection capabilities of the drive are satisfactory. A small overshoot in the speed and torque regulation occurs. However, the error rapidly decays to zero and steady state operation resumes. Since during the transient the modulator remains in the linear modulation region, the influence of the modulator type on the dynamic performance is negligible. Therefore, modulators with the same voltage linearity boundaries as the SVPWM linear modulation boundary (i.e. all the DPWM methods) exhibit the same dynamic performance. For this reason, the linear modulation region dynamic behavior of the DPWM methods is not illustrated and will not be discussed.

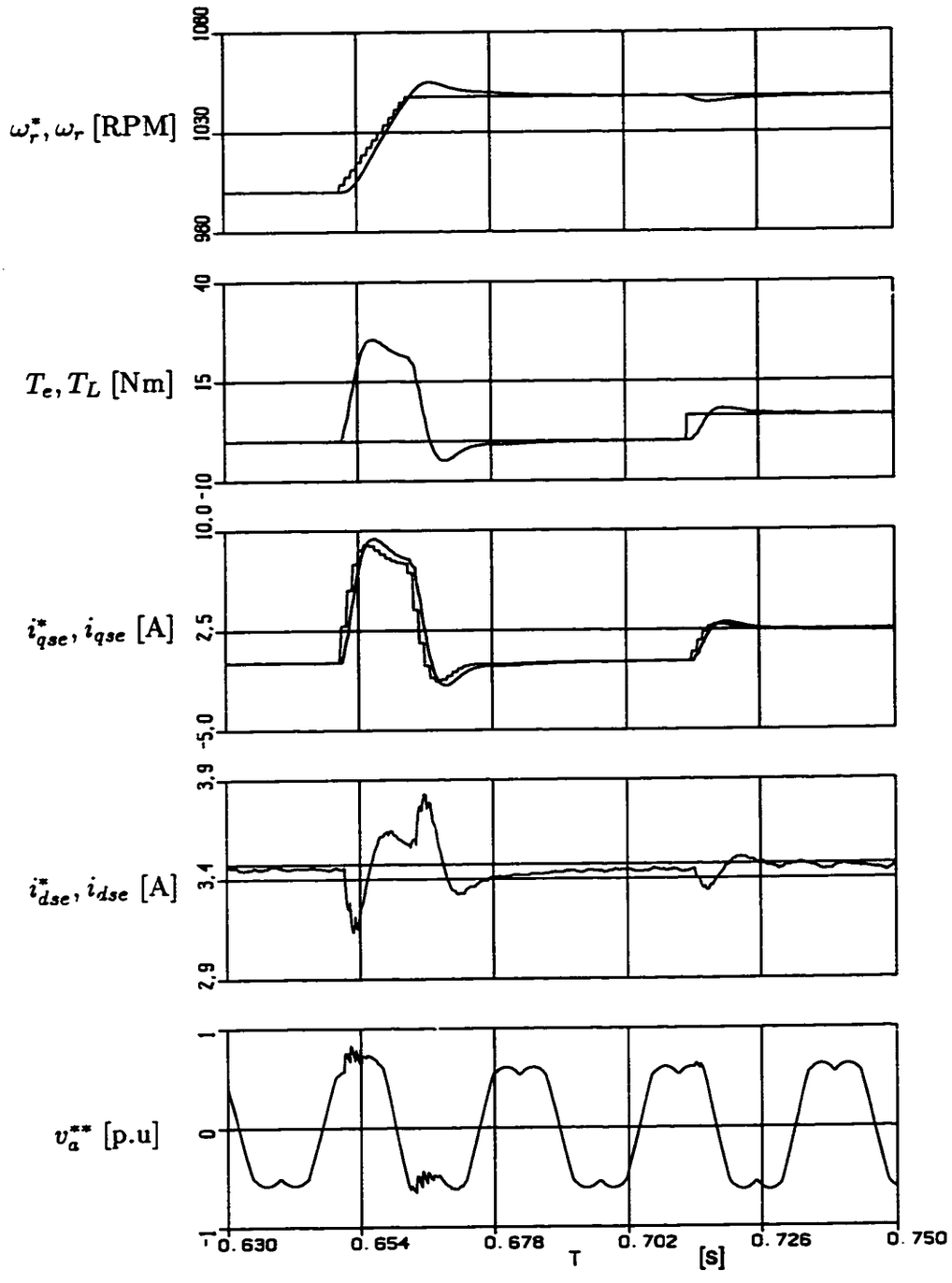

Figure 5.19: Induction motor drive SVPWM linear modulation behavior under speed reference ramp change and load torque step change.

The computer simulations of Figure 5.20 to Figure 5.23 illustrate drive overmodulation performance with various modulators. While the drive is operating at 1500 RPM and no load, an overmodulation condition is generated with a speed reference change and application of a load torque. A speed ramp command, ω_r^*, at t=0.65 [s] increases the speed from 1500 RPM to 1600 RPM in 24 ms, and the load torque, T_L, increases at t=0.71 [s] from zero to 50% of the rated motor torque. Figure 5.20 illustrates the dynamics with SVPWM. The voltage vector phase error polarity and magnitude vary according to Figure 5.9. The current controller antiwindup channels keep the reference voltage vector near the hexagon boundary (M_i^* of (7) is kept small) and the SVPWM method selects a vector close to the reference vector (one-step-optimal) resulting in a small phase error. As Figure 5.20 indicates, SVPWM provides good performance.

Shown in Figure 5.21, the DPWM0 modulated system always has a negative phase error, consistent with the theoretical prediction. As the output voltage vector leads the reference voltage vector more than the SVPWM case, the field current experiences poorer regulation. Although results show an increase in torque and slightly better speed response, the oscillatory behavior can eventually result in a drive failure under certain operating conditions. Shown in Figure 5.22, the DPWM1 modulated system exhibits similar behavior to SVPWM, however its phase error magnitude is larger and the field current regulation capability degrades as in the DPWM0 case. Although DPWM1 has a substantially higher fundamental component gain than the other modulators [64], its

dynamic performance is poorer than SVPWM. Therefore, it becomes clear that the open loop drive overmodulation performance criteria which suggests the modulator with the highest voltage gain is superior to the rest, and the closed loop system dynamic overmodulation performance criteria which suggests the modulator with the best speed response (in speed regulated drives) and disturbance rejection is superior to the rest, are different and result a in different modulator selection.

Shown in Figure 5.23, the DPWM2 modulated system simulations illustrate the dynamic overmodulation performance deficiency of this method. The phase error is large and always positive (lagging); the field current increases and results in reduced torque, hence very poor dynamics. Although in induction motor drive applications the linear modulation range switching loss characteristic of DPWM2 is superior to other modulators [62], its overmodulation performance is quite poor. Therefore, in current controlled drives operation of this modulator in the overmodulation region should be prohibited and further control algorithm modifications are required.

The above simulation results indicate the SVPWM dynamic overmodulation performance is superior to all the other triangle intersection PWM methods. The modulator generates an output voltage vector with a small phase error and its one-step-optimal current regulation characteristic can successfully manipulate most dynamic conditions. However, very low inertia and very abrupt dynamic conditions could still not be properly manipulated and sufficiently large

phase error intervals may result in unstable behavior and unacceptable drive performance. Therefore the modulator choice must be carefully made.

Since the above simulation studies suggest the DPWM methods have poor dynamic overmodulation characteristics and their large phase errors result in strong unwanted dynamics, it becomes inevitable to make modifications to the drive control algorithm when employing such modulators. Since the DPWM methods have superior linear modulation range switching loss and waveform quality characteristics, their utilization in many applications is favorable and a moderate increase in the control algorithm complexity and drive cost can be easily compensated with the performance gain. In this work two modification methods are suggested.

In the first approach, the DPWM method of choice is combined with SVPWM and when a dynamic overmodulation condition is detected, SVPWM is activated while in the linear region the DPWM method resumes control. Figure 5.24 illustrates the drive dynamic behavior with this algorithm. As the simulation waveforms indicate, in the linear modulation region DPWM2 is active, however as a dynamic overmodulation condition occurs the SVPWM signals are activated and the dynamics are rapidly manipulated. Since recent commercial drives often employ SVPWM and a DPWM method in combination to improve the linear modulation range waveform quality (for small M_i SVPWM and for large M_i DPWM is selected) and reduce switching losses [62], the modulation signal generating blocks may already exist in a drive and only an additional

loop and re-calculation of the modulation signals is required. In particular implementing such an algorithm in a DSP based controller is an easy task.

In the second approach a more complex and higher performance algorithm, the dynamic field weakening method can be adapted from the direct digital technique [88, 182]. As shown in Figure 5.6, in this approach, the motor back EMF, $\hat{E}_{dqe}$, (calculated from the estimated stator flux) and the PI current controller outputs V^*_{dqefb}, are vectorially added and the intersection point with the hexagon (point "c" in the figure) is the tip point of the vector that forces the current error vector to move in the controller reference direction. By employing this algorithm, the reference voltage vector which is outside the inverter hexagon, is modified and returned to the inverter hexagon with a corrected phase such that any modulation method will exactly match the modified reference vector. Therefore, the modification algorithm performs equivalently with all the triangle intersection modulation methods. The simulation waveforms in Figure 5.25 illustrate the performance of DPWM2 combined with the dynamic field weakening method. When a dynamic overmodulation condition occurs, the dynamic field weakening algorithm is activated and the reference vector is modified and returned to the hexagon boundary such that DPWM2 exactly generates this vector. Note that this method generates a significantly small phase error and the field current experiences less transients than the SVPWM case. Also note the phase error alternates and during the speed ramp the field current increases for a short time interval. Due to this reason, a better term for the method would be "a phase error regulation method." This method however

is fairly complex and requires substantial amount of calculations for relocating the reference voltage vector. Hence, only suitable for high performance fully digital drives with fast DSP controllers.

It should be noted for rapid torque regulation purposes, the SVPWM method provides a superior dynamic overmodulation response compared to all other methods due to its inherent one step optimal current regulation attribute. However, with SVPWM the rotor flux experiences more oscillations than DFW and under longer dynamic overmodulation transients, the SVPWM torque response superiority is lost.

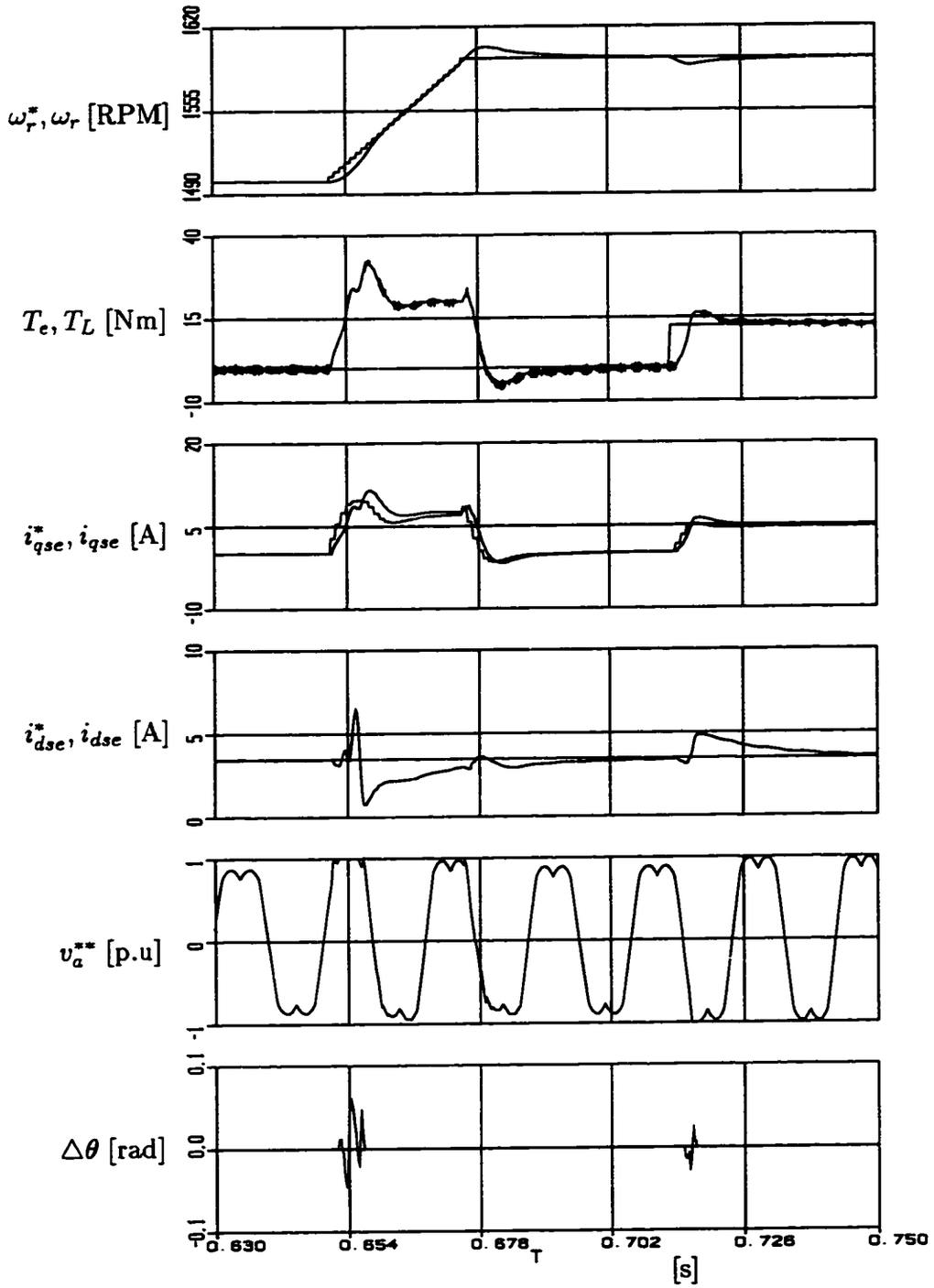

Figure 5.20: Induction motor drive SVPWM dynamic overmodulation behavior under speed reference ramp change and load torque step change.

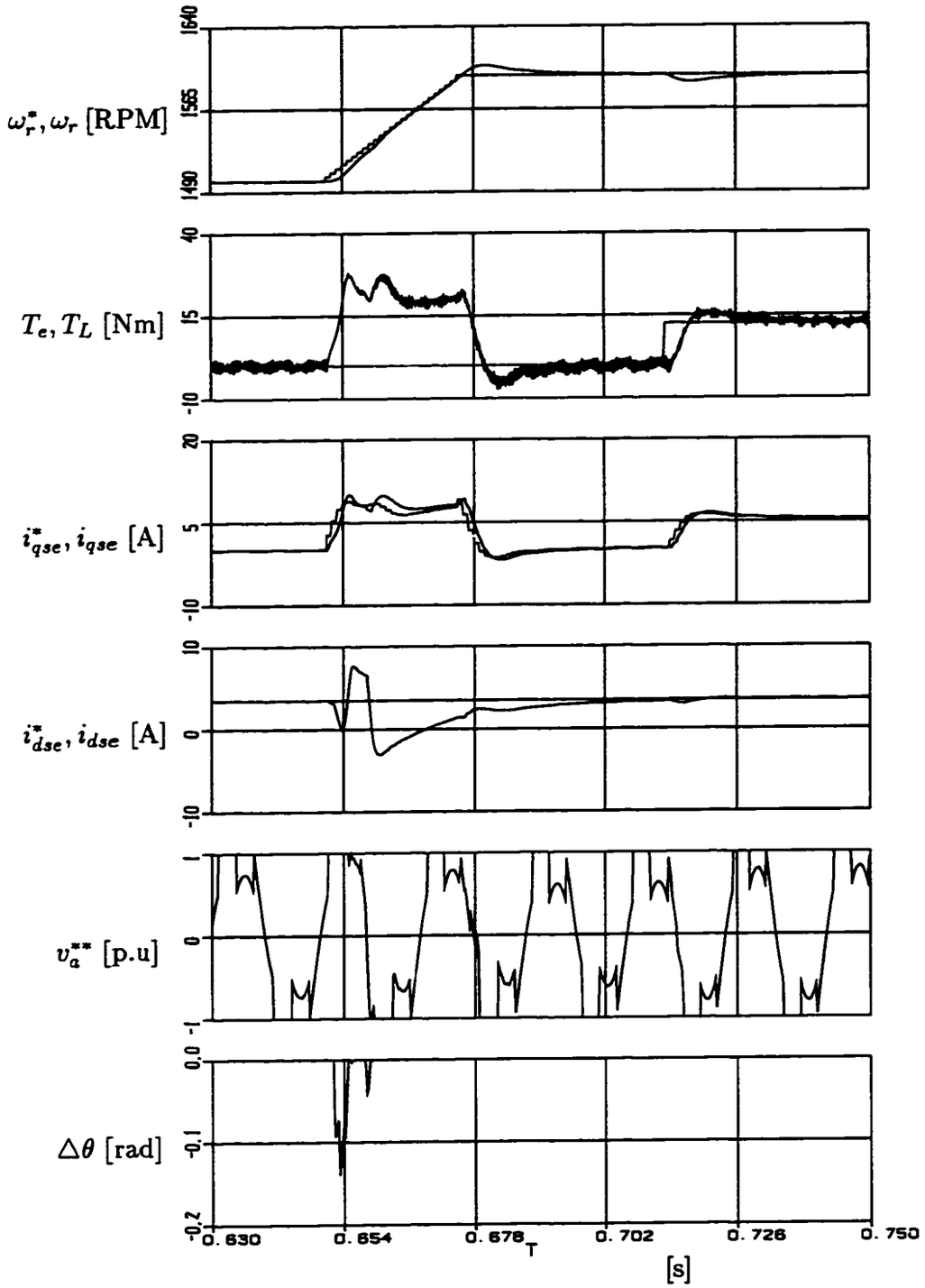

Figure 5.21: Induction motor drive DPWM0 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

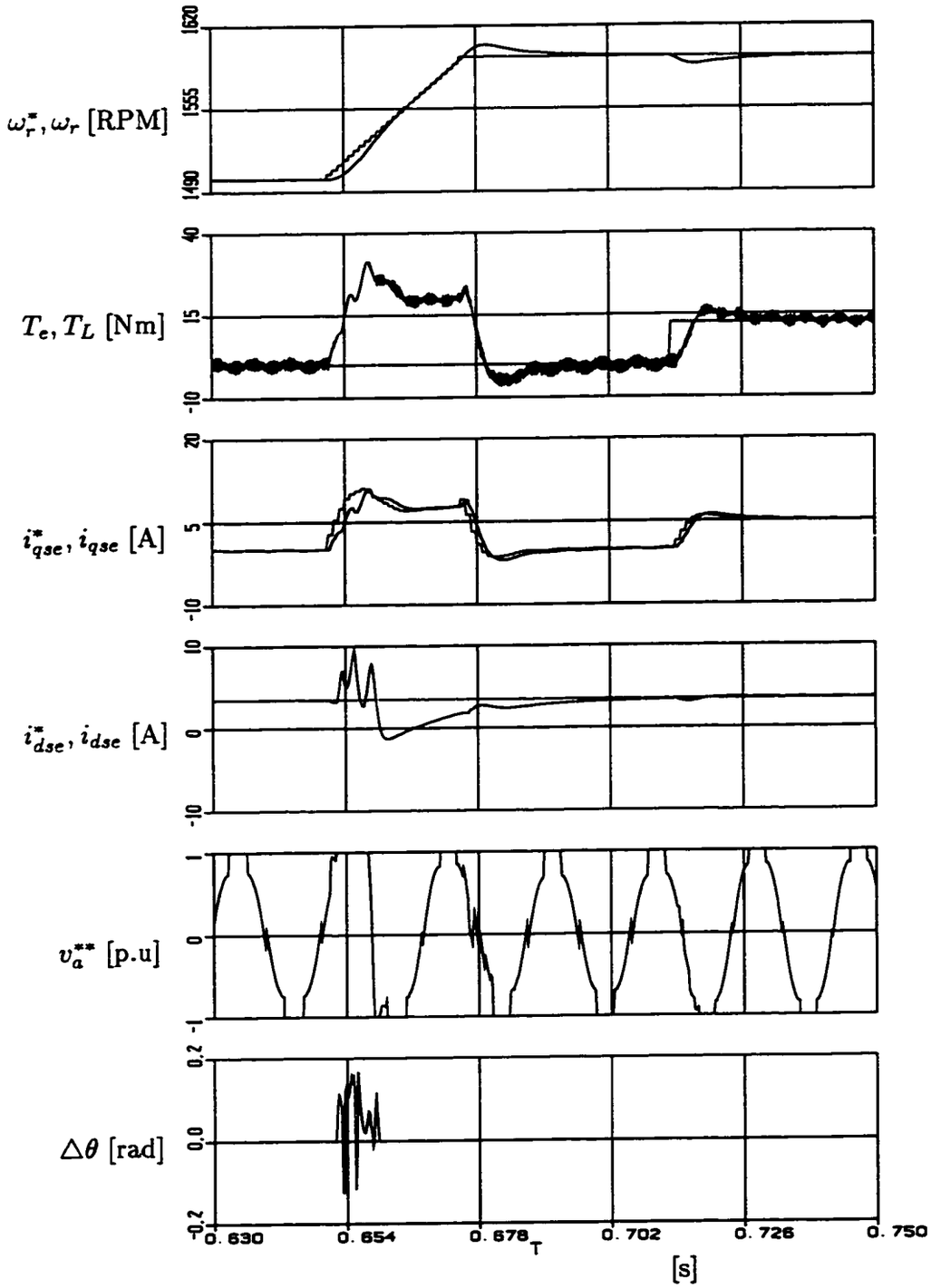

Figure 5.22: Induction motor drive DPWM1 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

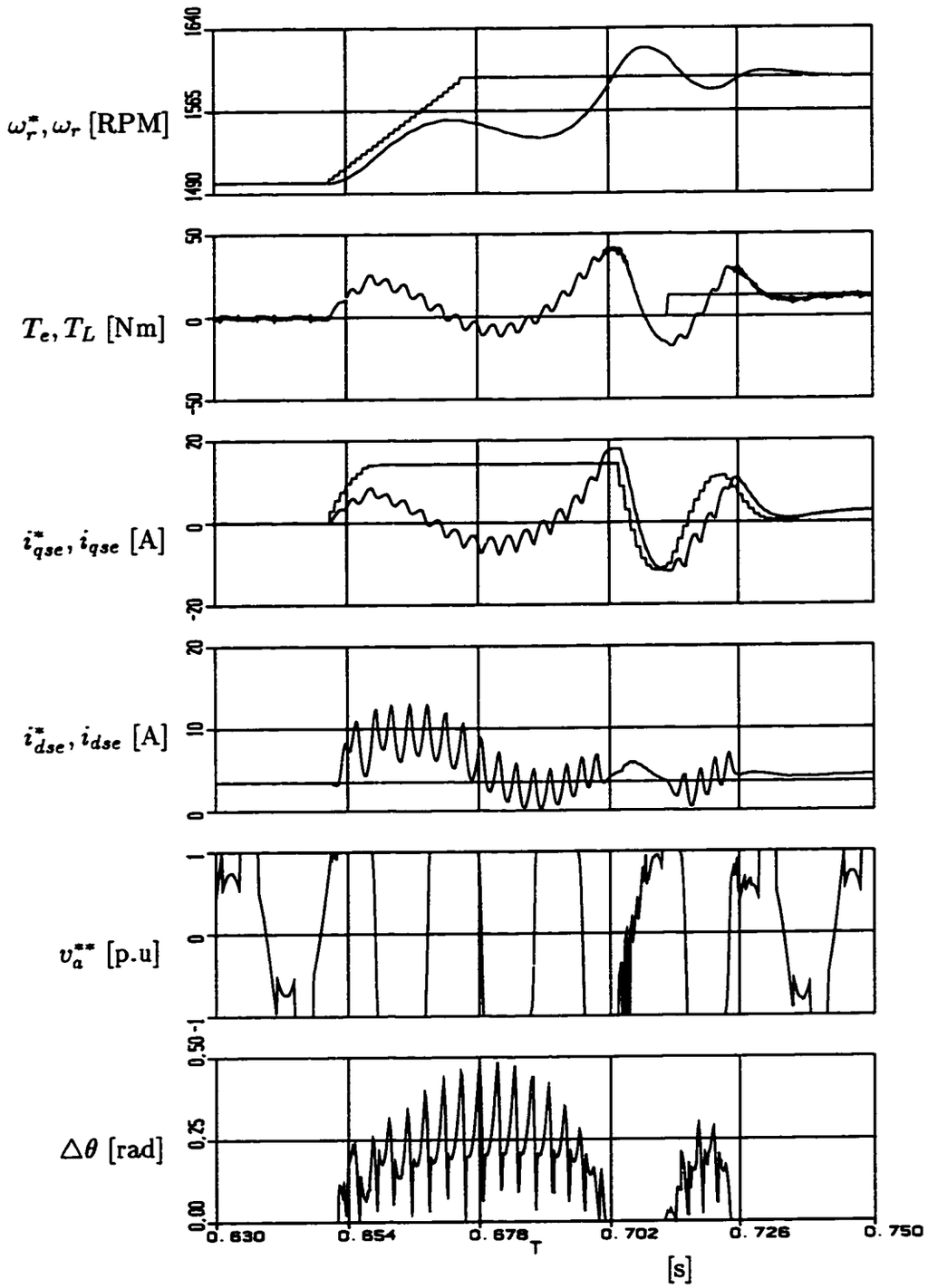

Figure 5.23: Induction motor drive DPWM2 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

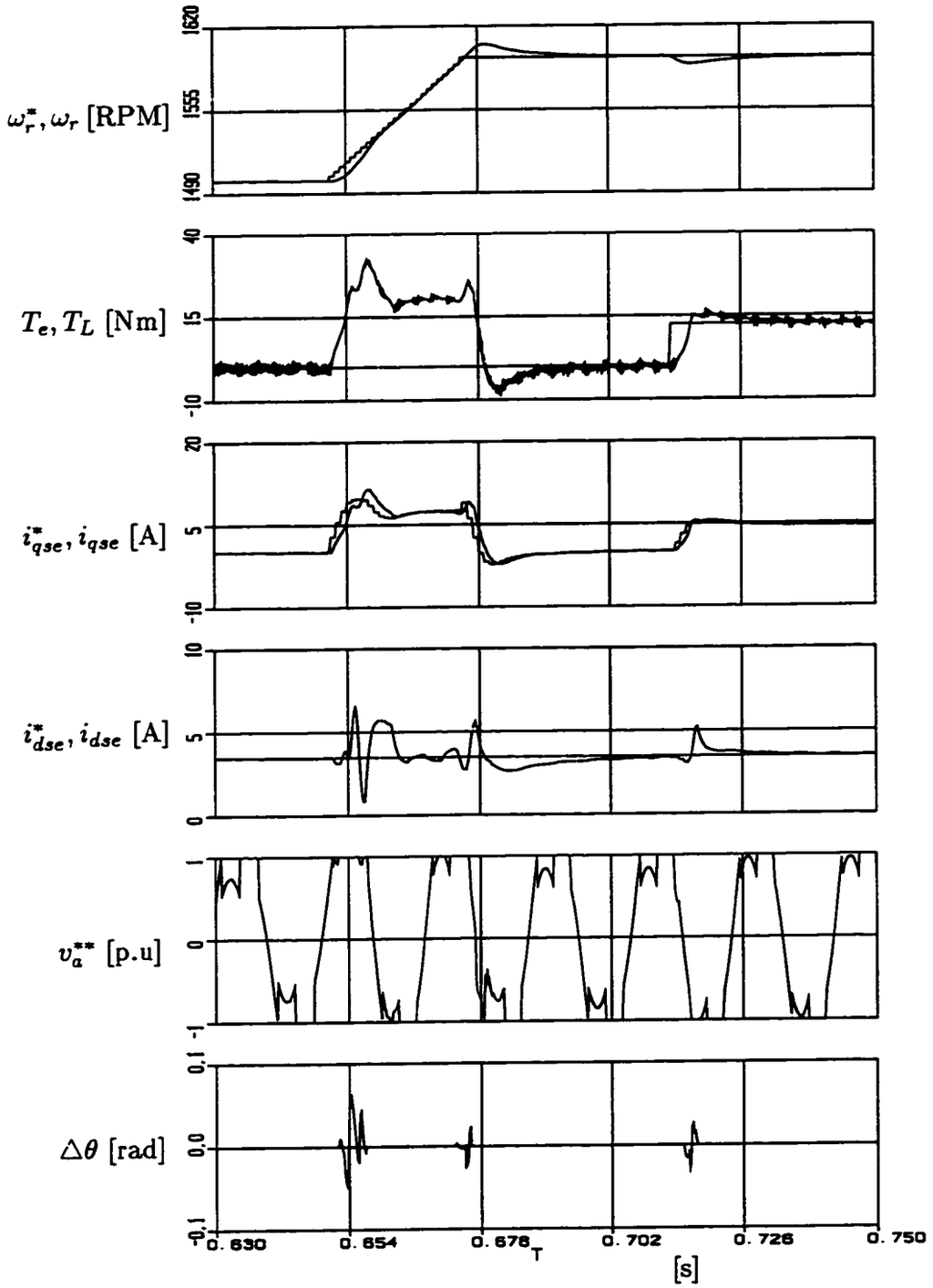

Figure 5.24: Induction motor drive DPWM2 (linear mode) and SVPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

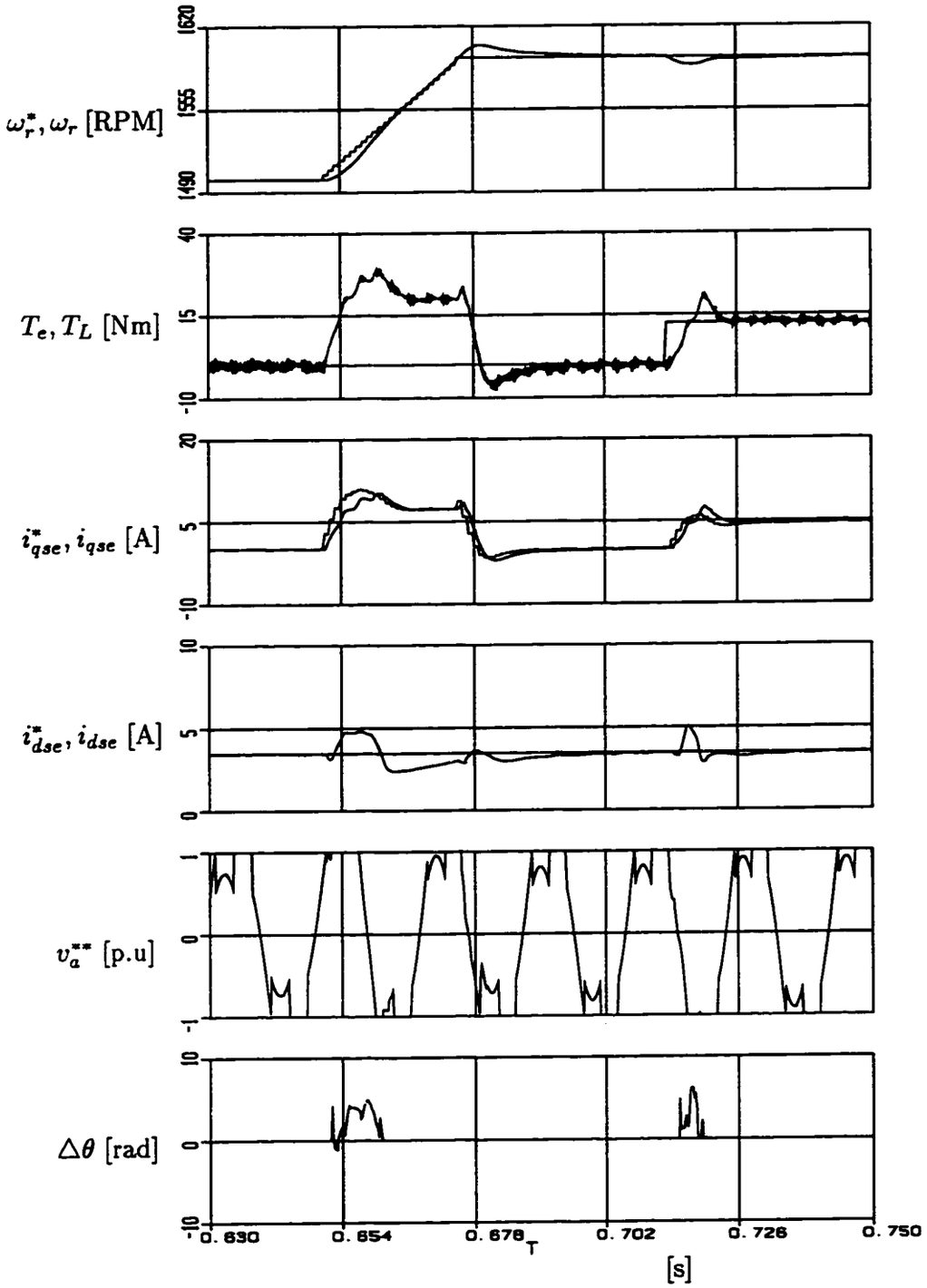

Figure 5.25: Induction motor drive DPWM2 (linear mode) and DFWPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

5.7 Experimental Results

In this section the dynamic overmodulation behavior of an IFOC algorithm based induction motor drive is experimentally investigated. The drive employs digital SFCR to achieve high bandwidth current regulation. Due to the laboratory limitations only an induction motor without load and without additional inertia could be tested.

A prototype digital control board (developed at Rockwell Automation-Allen Bradley, Inc. for PWM-VSC applications) and a commercial PWM-VSI (20 kW, 620 VDC, 460 V, 21 A, PWM-VSI by Rockwell Automation-Allen Bradley, Inc.) were interfaced to form the laboratory PWM inverter drive. The inverter was diode rectifier front end type. All the control tasks were performed by a digital signal processor (MOTOROLA 56005 DSP [80]) with a 40 MHz clock frequency (25 ns instruction cycle). Originally designed for computer disk drive applications, this DSP chip has six PWM counter comparators (analog/digital hardware triangular wave carrier signal and comparator circuits eliminated). Once loaded with the duty cycle count, each PWM counter increments the count, compares to the reference, and outputs a gate drive logic signal. Also, with the built in inverter blanking time generation circuit (digital), this PWM generator eliminates the need for hardware blanking time generation circuits. Since the digital control board was designed for PWM-VSC applications, it had no digital motor shaft encoder interface capability and therefore the incremental position information was absent in the controller. This hardware constraint

limited the drive bandwidth and the experimental investigation of drive dynamic performance.

The controller board employed the synchronous sampling technique to measure the motor feedback currents. An A/D converter with 2 μs conversion time and an eight-channel-multiplexer were utilized to sample the three phase motor currents, the DC link voltage, and several other analog input signals (analog speed feedback, speed reference and controller gains). The A/D sampling process was triggered every carrier cycle at the instant the PWM counters were loaded with the new duty cycle value (equivalent to triggering at the peak of the triangle). The multiplexer sequentially selected the analog signals to be sampled until all the analog inputs were sampled, held, put in a register, and finally stored in a memory location for access by the DSP.

With the motor currents being sampled first, the values of the first two currents could be utilized to calculate the third current. With this approach, the first feedback current was precisely measured (synchronous sampling), the second feedback current was measured with 2 μs delay. The current transducer (closed loop hall effect current transducers by LEM Inc.) offset errors were subtracted from these signals by the DSP (offsets were read and stored in the DSP memory with the inverter disabled during initialization). The third current was calculated from the first two and has an equivalent delay of 1 μs (average delay of the other two signals). Therefore, the feedback current values represented the per carrier cycle average currents with reasonable accuracy. This single A/D

solution resulted in a low cost controller and is suitable in many applications (Worthwhile to mention is some recent motion control DSPs utilize two parallel A/D channels and can sample two feedback currents simultaneously such that true synchronous sampling is possible [155]). The DC link voltage and other analog input signals were also sampled at the carrier frequency rate. However, due to the slow variation of these signals, they could be updated at the speed loop sampling rate (five times smaller than the carrier frequency).

Synchronous frame current controller with antiwindup structure (the algorithm described in the simulations section of this chapter) was implemented in the DSP and the controller calculations were updated once every carrier cycle. The carrier frequency was selected as 5 kHz (200 μ s carrier cycle). The speed loop and DC buc voltage disturbance rejection controller were also programmed in the DSP and the update rate was selected as 1 kHz (once every five carrier cycles). The speed loop antiwindup structure was similar to the current loop antiwindup structure and it had a constant maximum output signal limit (the maximum I_{qe} limit of the inverter drive).

Due to the lack of the digital encoder feedback signal interface capability, the experimental system had limited motion control performance. However, an analog speed feedback was utilized in order to achieve sufficient bandwidth to illustrate the dynamic overmodulation performance characteristics of various PWM methods. For this purpose, a digital incremental encoder was mounted on the shaft of the induction motor and an Allen Bradley encoder interface and

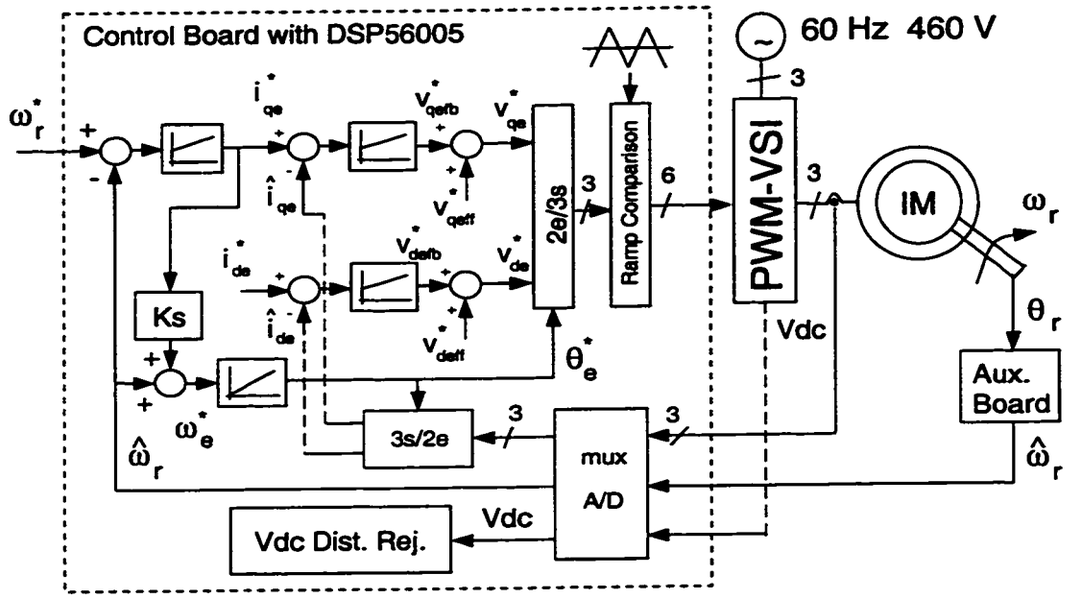

Figure 5.26: The experimental RFO-IFOC drive control diagram.

motion control circuit board (will be termed as the auxiliary board) which could provide analog speed signal output was interfaced with the encoder. The auxiliary board calculated the shaft speed and generated an analog output signal at a 1 kHz rate. This analog speed signal was input to the DSP through the analog input channels. It was processed through the A/D converter and updated once every five carrier cycles (at 1 kHz rate). Therefore, the total speed measurement delay was at least 2 ms (1 ms delay in each unit). The small delays of the several hardware and digital signal conditioning filters slightly contributed to the measurement delay. The experimental drive control diagram is illustrated in Fig. 5.26 in detail.

As illustrated in Fig. 5.26, the speed feedback signal, and the slip frequency (computed by multiplying the slip gain with I_{qe}^{*}) are added to generate the

electrical frequency reference. This signal is integrated to generate the electrical angle reference for the controller. Unlike the conventional industrial drives, which measure the shaft position and estimate the speed by computational procedures, the laboratory drive employed the reverse procedure. Therefore, the precision of the speed measurement could lead to a significant error between the shaft position and its estimate. Since the IFOC system dynamic performance is strongly affected by the position error, the bandwidth of such a system is expected to be significantly smaller than a system with an accurate position estimate. Therefore, the drive controller gains were tuned for a relatively low bandwidth. The speed loop proportional and integral gains of the laboratory drive were experimentally optimized and a 5 Hz bandwidth with unity damping could be obtained. This bandwidth value is significantly below the bandwidth of the industry standard IFOC controlled industrial drives with encoder feedback (typically 30 Hz and above is achievable) and comparable to the bandwidth of observer based drives. However, this bandwidth was sufficient to generate a notable dynamic overmodulation condition and illustrate the performance of the laboratory drive with various modulators.

The experimental motor is a four pole squirrel cage induction motor (US Motors Inc.) with the following nameplate: 5 HP, 60 Hz, 460 V, 6.9 A, 1745 RPM. The motor lumped equivalent circuit parameters were obtained by measurement and estimation (from Auto-tuning test with a commercial drive). The stator phase resistance was measured as 1.969 ohm per phase. The stator transient inductance estimated as 22.39 mH, the stator magnetizing inductance as 0.276 H,

the rotor inertia as $0.07kgm^2$, the rated magnetizing current as $I_{deR} = 3.4734A$, the slip gain as $K_s = 1.263$, the rated slip as $s\omega_{eR} = 11.52rad/s$ (55 RPM mechanical radial speed), and the rotor resistance as 1.73 ohm. The rated torque current was calculated as $I_{qeR} = 9.119A$. And the maximum torque current limit of the current controller was set to 150 % of the rated torque current, i.e. $I^*_{qemax} = 14.22A$.

In order to illustrate the dynamic overmodulation performance of the SFCR based drive with different modulators, a dynamic overmodulation condition was forced by rapidly varying the speed reference signal. While the drive was operating at 1350 RPM (45 Hz electrical frequency) at steady state and no load conditions, the speed reference was increased to 1650 RPM (55 Hz electrical frequency) in 50 ms with a ramp function. The speed ramp signal was programmed with the DSP by incrementing the signal at 1 ms rate and it was externally triggered. Since the analytical investigation clearly illustrated the inferior performance characteristics of SPWM and the THIPWM methods, experimental investigation of these methods was omitted. Therefore, the dynamic overmodulation test was conducted with SVPWM, DPWM0, DPWM1, and DPWM2. In each case the motor phase currents and speed, the modulation waves, and the controller signals (obtained through the D/A channels of the DSP board) were recorded. Since the laboratory oscilloscope channel capacity was limited to four, for each modulator the experiments had to be repeated several times to observe and record all the important the waveforms.

The dynamic overmodulation behavior of DPWM0 is illustrated in Figures 5.27,5.28,5.29,5.30, 5.31,5.32, and 5.33 with both zoomed and long time behavior waveforms. As Fig. 5.28 clearly illustrates, the saturated modulation wave indicates the drive exhibits dynamic overmodulation. Due to the saturation, the motor d and q axis current regulation becomes poor and the current and speed errors become large and oscillatory. As the speed reference is rapidly increased, first the speed regulator delay and following the current controller saturation limit the drive torque and the actual speed lags the reference significantly. With the overmodulation condition enduring, the speed loop exhibits oscillation. Note as illustrated in Fig. 5.28, the motor currents within the first few overmodulation cycles are similar to the six step mode waveforms. However, as the speed error gradually decreases to zero (in about six fundamental cycles) the linear modulation region is approached, the next steady state operating point is reached and the current waveforms become more sinusoidal. Note the new steady state operating point is slightly outside the linearity limit of this modulator. Although the final speed is smaller than the rated speed, and the drive is expected to operate in the linear modulation region, this does not occur. As Fig. 5.31 and Fig. 5.32 illustrate, in the new steady state, the d axis current is larger than its reference value. This condition implies that correct field orientation is not achieved due to the difference between the actual rotor flux angle and the flux angle the position estimator computes. Also, as a result of the incorrect field orientation the drive requires higher terminal voltage than the voltage required for the intended steady state operating speed. Therefore,

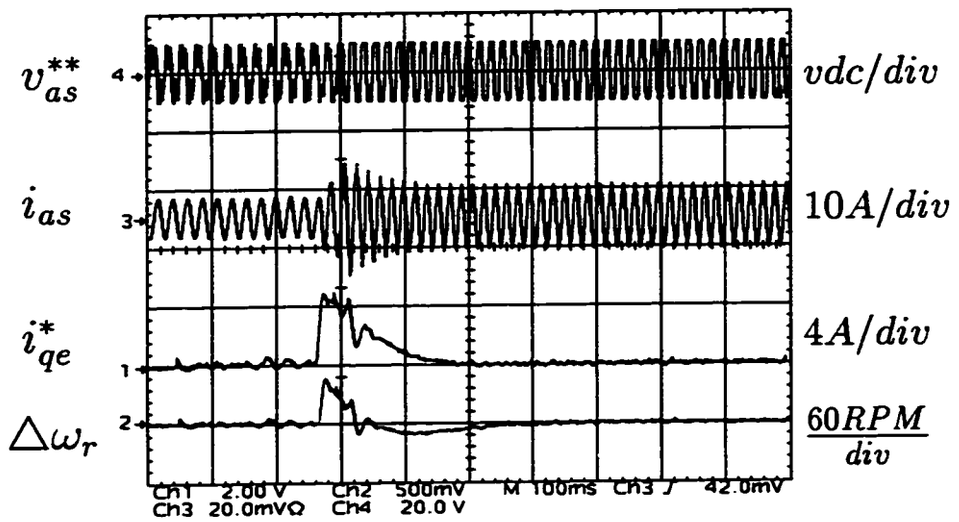

Figure 5.27: DPWM0 modulation signal, phase current, q axis current reference, and speed error oscillograms.

following the dynamic overmodulation transient, the new steady state operating point is slightly outside the linear operating region, i.e. in the overmodulation region. However, the experimental waveforms clearly illustrate the dynamic overmodulation condition and provides a base for comparing the performance of all the discussed modulators.

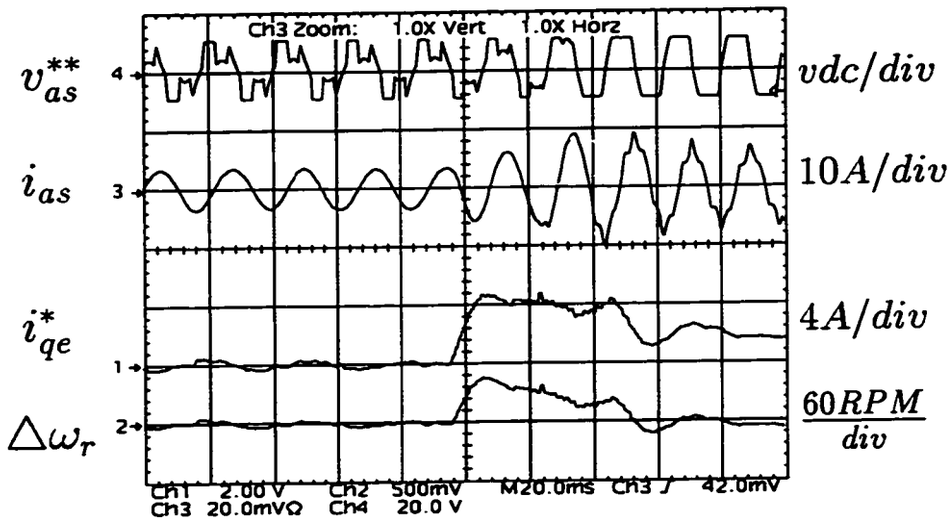

Figure 5.28: DPWM0 modulation signal, phase current, q axis current reference, and speed error oscillograms: zoomed view of the first few cycles.

Shown in Figures Fig. 5.34, Fig. 5.35, Fig. 5.36,the DPWM1 dynamic overmodulation waveforms exhibit similar characteristics to DPWM0. With the DPWM1 method having higher fundamental component voltage gain and the transients enduring several fundamental cycles, the DPWM1 method output voltage has stronger dynamics. It responds faster. However, it is more oscillatory. The speed error peak value of DPWM1 is larger than the DPWM0 case. Also the phase currents of DPWM1 have larger peak value. The large phase error and high fundamental component voltage gain characteristics of this method result in poorer dynamic overmodulation performance of this method compared to DPWM0. As the waveform of Fig. 5.36 illustrates, with this method also correct field orientation is not achieved due to the incorrect rotor flux angle estimation and at the final operating point the d axis current is larger than

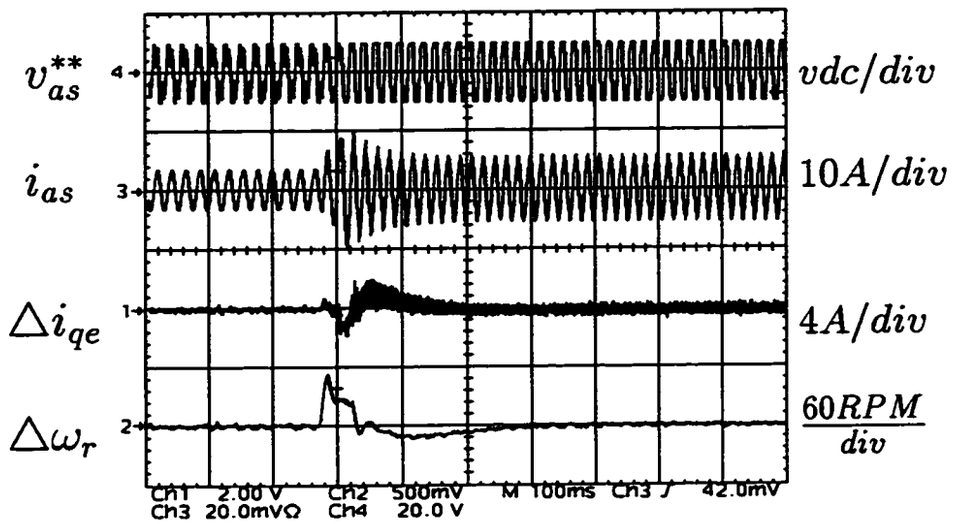

Figure 5.29: DPWM0 modulation signal, phase current, q axis current error, and speed error oscillograms.

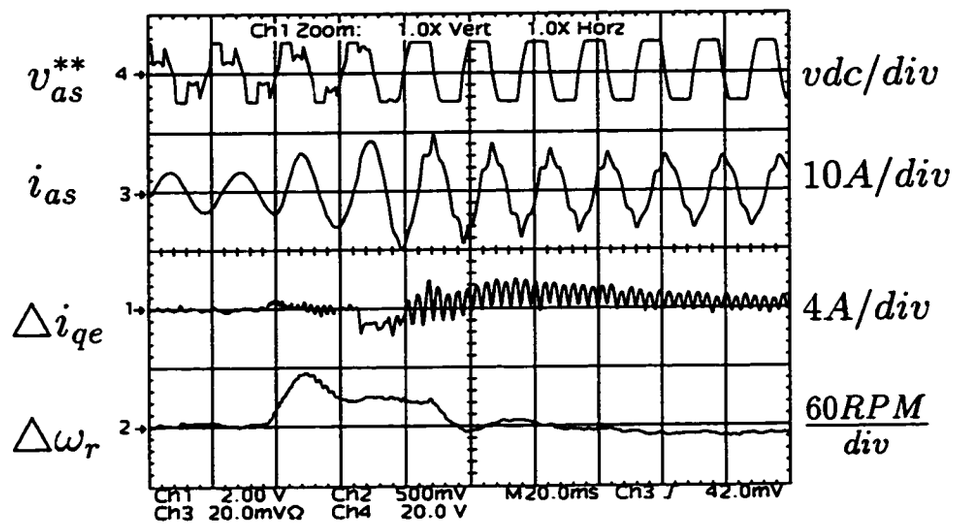

Figure 5.30: DPWM0 modulation signal, phase current, q axis current error, and speed error oscillograms: zoomed view of the first few cycles.

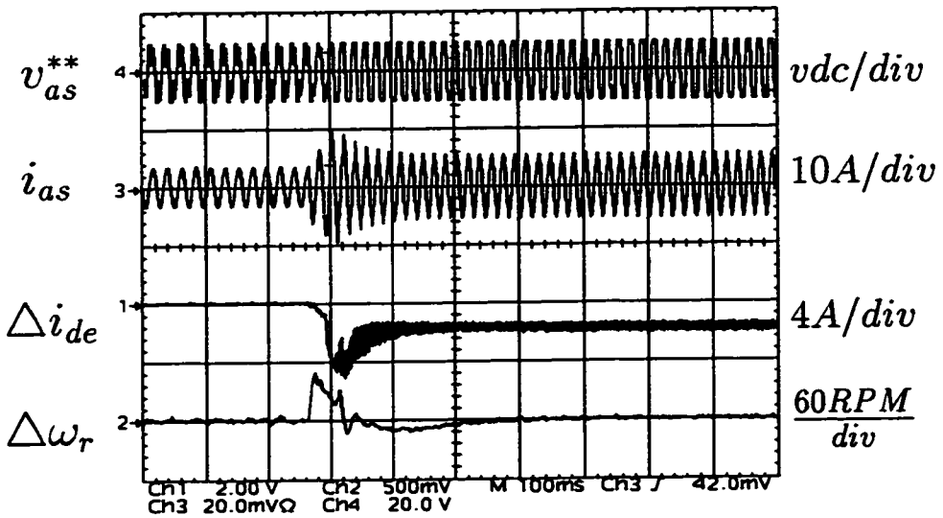

Figure 5.31: DPWM0 modulation signal, phase current, d axis current error, and speed error oscillograms.

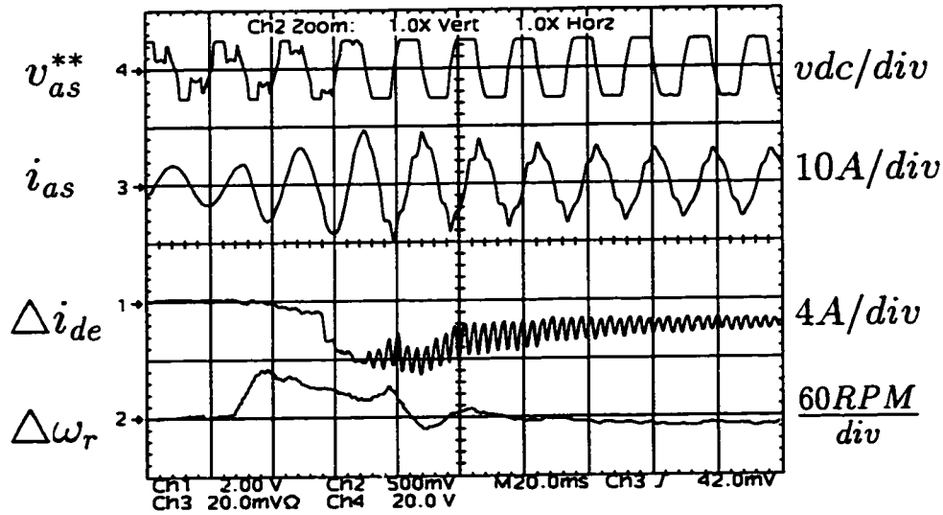

Figure 5.32: DPWM0 modulation signal, phase current, d axis current error, and speed error oscillograms: zoomed view of the first few cycles.

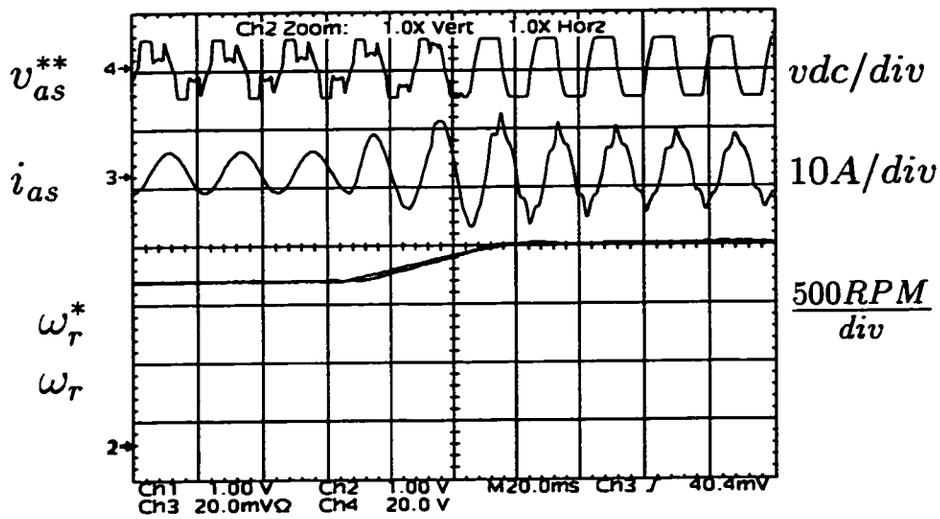

Figure 5.33: DPWM0 modulation signal, phase current, speed and speed reference oscillograms.

the reference value. Therefore, at the final operating point this modulator also operates outside its voltage linearity region. The long term waveforms of this case will be omitted and they are similar to the DPWM0 waveforms.

Figures Fig. 5.37, Fig. 5.38, Fig. 5.39, and Fig. 5.40 illustrate the DPWM2 dynamic overmodulation characteristics. It is apparent from the waveforms that the poor phase error characteristics of this modulator result in poorer response compared to DPWM0 and DPWM1. As the all the three figures illustrate, the speed error is more oscillatory and the maximum error is significantly larger than the DPWM0 and DPWM1 case. Under a dynamic overmodulation condition, DPWM2 results in poor d and q axis voltage partitioning and results in significantly larger flux current and significantly smaller torque current. As a result, the dynamic performance significantly degrades. Although the zoomed

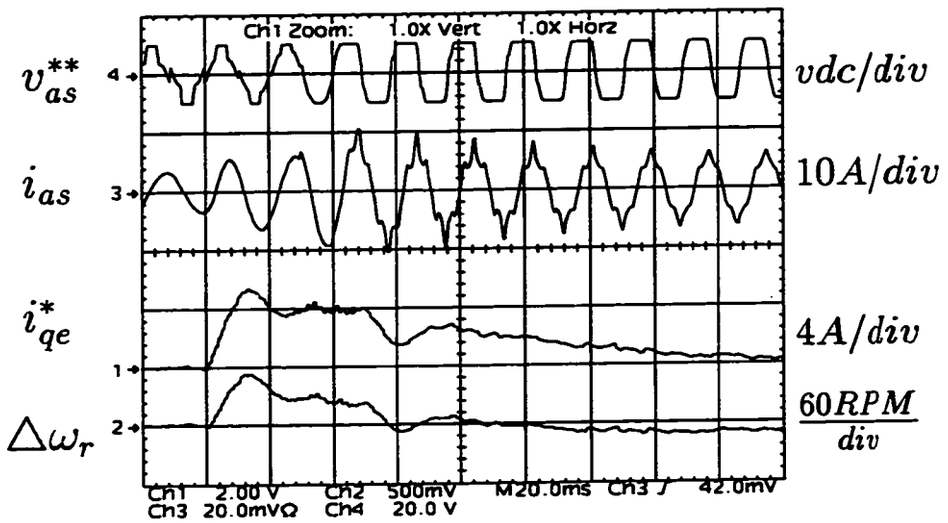

Figure 5.34: DPWM1 modulation signal, phase current, q axis current reference, and speed error oscillograms.

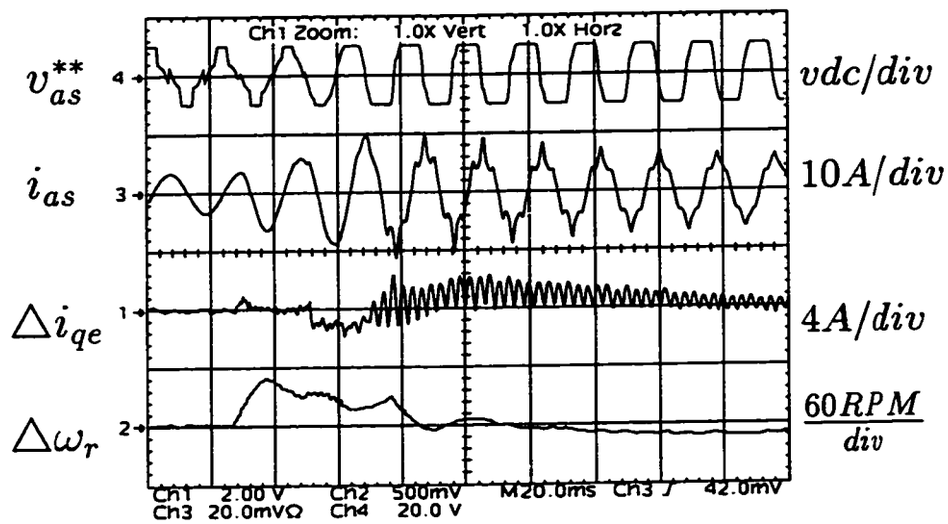

Figure 5.35: DPWM1 modulation signal, phase current, q axis current error, and speed error oscillograms.

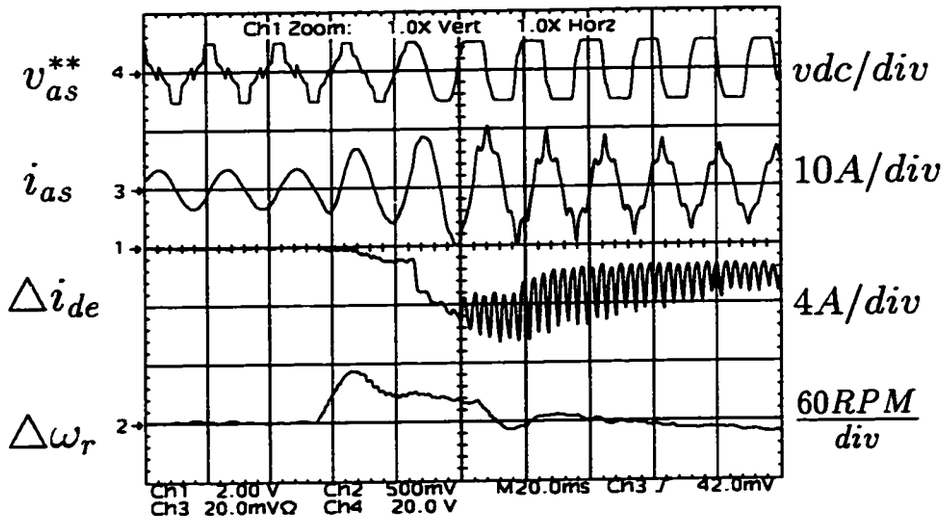

Figure 5.36: DPWM1 modulation signal, phase current, d axis current error, and speed error oscillograms.

view of Fig. 5.39 illustrates the d axis current error is more successfully manipulated than the other cases (at least for the first few cycles), as the speed error is not rapidly manipulated, the d axis current error increases again and the incorrect flux orientation (due to incorrect flux angle estimation) yields a final operating point in the overmodulation region.

Figures Fig. 5.41, Fig. 5.42, and Fig. 5.43 illustrate the SVPWM dynamic overmodulation performance. As the figure indicates, the SVPWM performance is less oscillatory than DPWM1. However, a comparison between SVPWM and the DPWM1 and DPWM0 indicates these modulators perform quite similarly. This is due to the fact these methods exhibit similar phase characteristics. DPWM0 phase error is positive, however small. DPWM1 phase error is larger, however its polarity alternates and for dynamics enduring a period of one-sixth

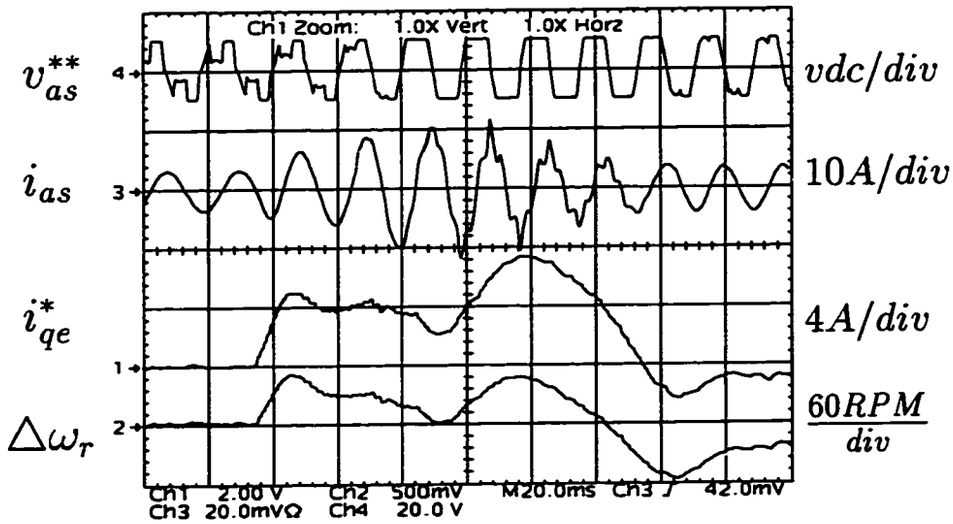

Figure 5.37: DPWM2 modulation signal, phase current, q axis current reference, and speed error oscillograms.

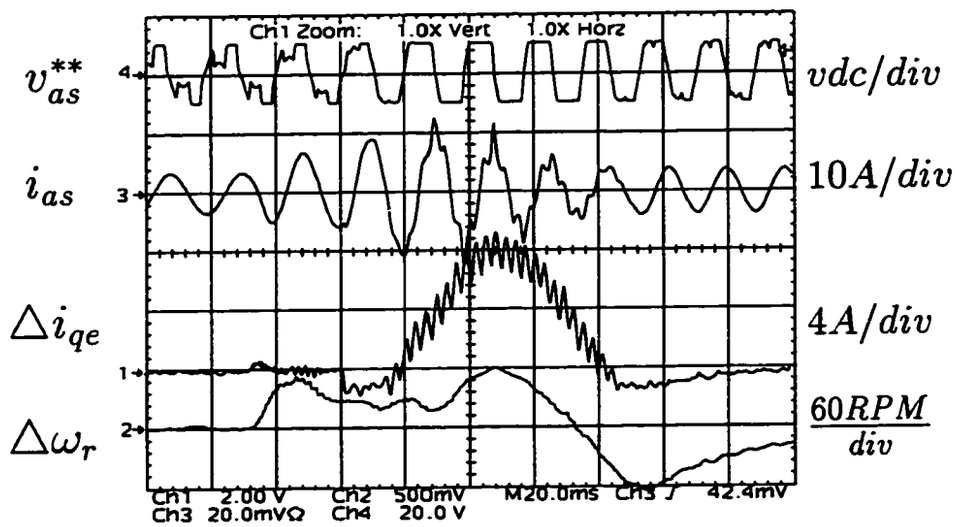

Figure 5.38: DPWM2 modulation signal, phase current, q axis current error, and speed error oscillograms.

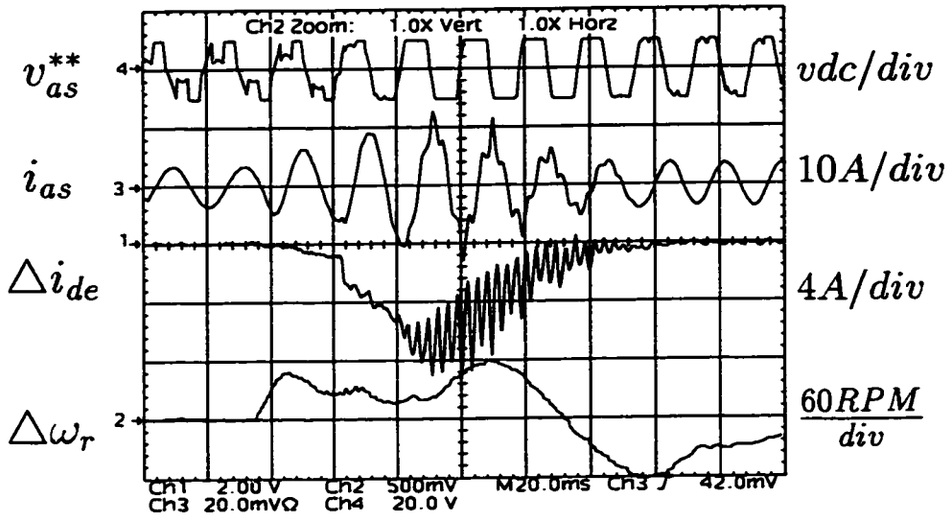

Figure 5.39: DPWM2 modulation signal, phase current, d axis current error, and speed error oscillograms.

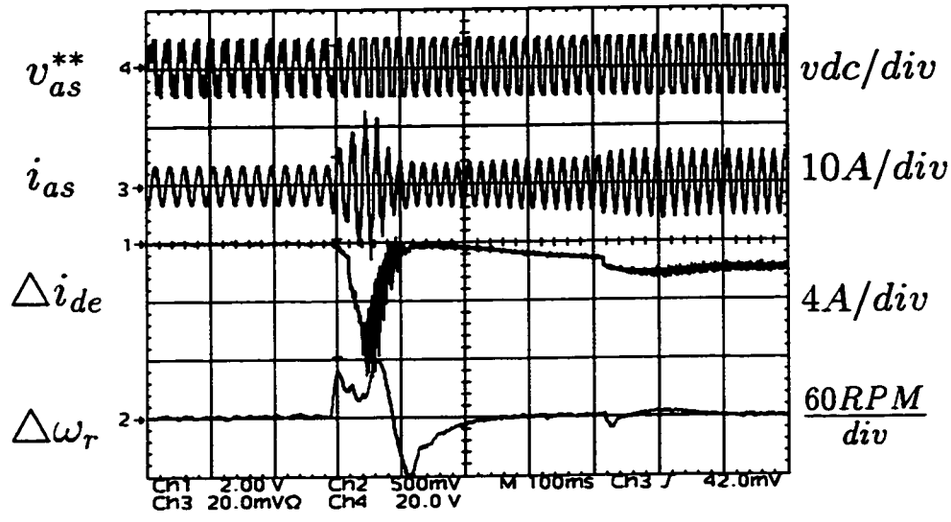

Figure 5.40: DPWM2 modulation signal, phase current, d axis current error, and speed error oscillograms.

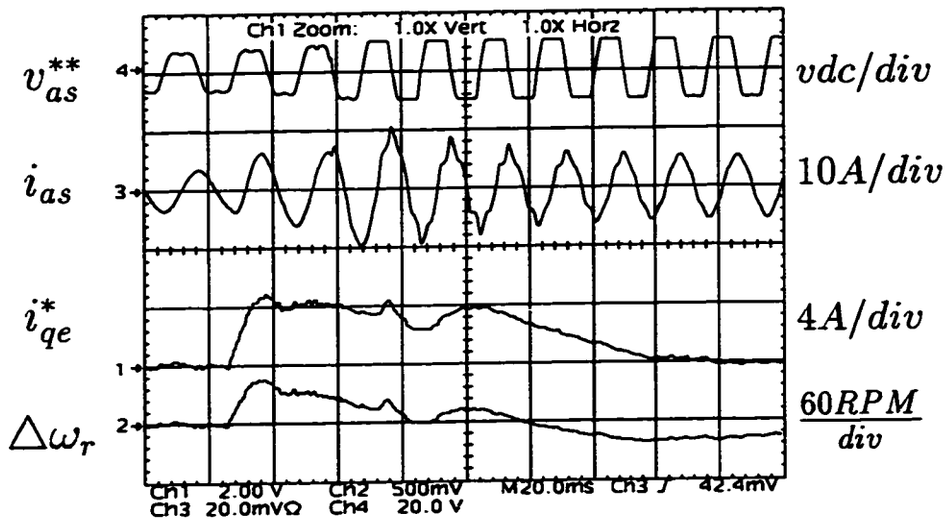

Figure 5.41: SVPWM modulation signal, phase current, current reference, and speed error oscillograms.

of a fundamental cycle or longer, it yields practically a small average value. Although for different reasons, both DPWM methods exhibit a performance similar to SVPWM. However in a higher bandwidth drive, dynamics enduring shorter time intervals are expected to yield distinguishable differences between all the methods (as predicted by analytical models). Due to its one-step-optimal performance, the SVPWM method manipulates the flux oscillation more rapidly and in the final operating point the motor phase current is more sinusoidal indicating an operating point closer to the maximum linear modulation boundary. Partially, the current waveform is more sinusoidal due to the fact the effective PWM frequency of DPWM methods is 66 % of the SVPWM method.

Although the overshoot and the initial response characteristics vary, the settling time is practically the same in all the modulator cases. This is due to the

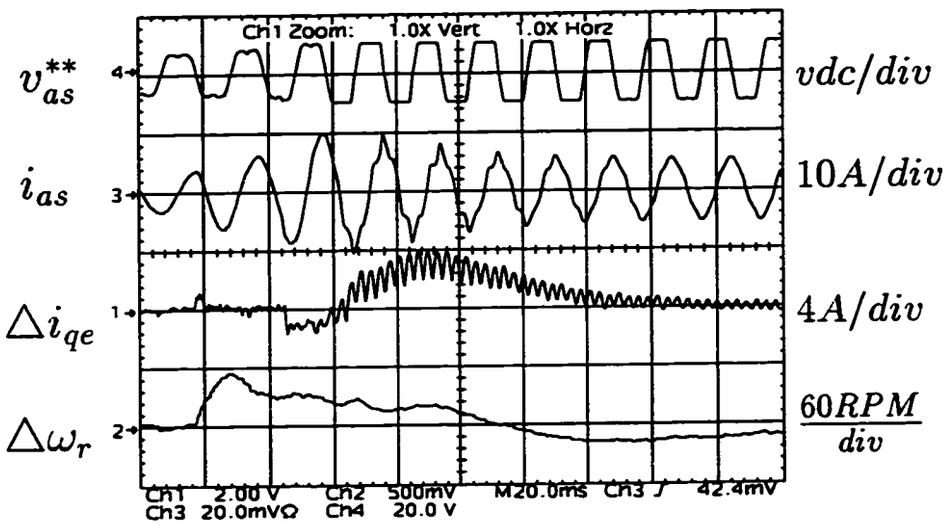

Figure 5.42: SVPWM modulation signal, phase current, q axis current error, and speed error oscillograms.

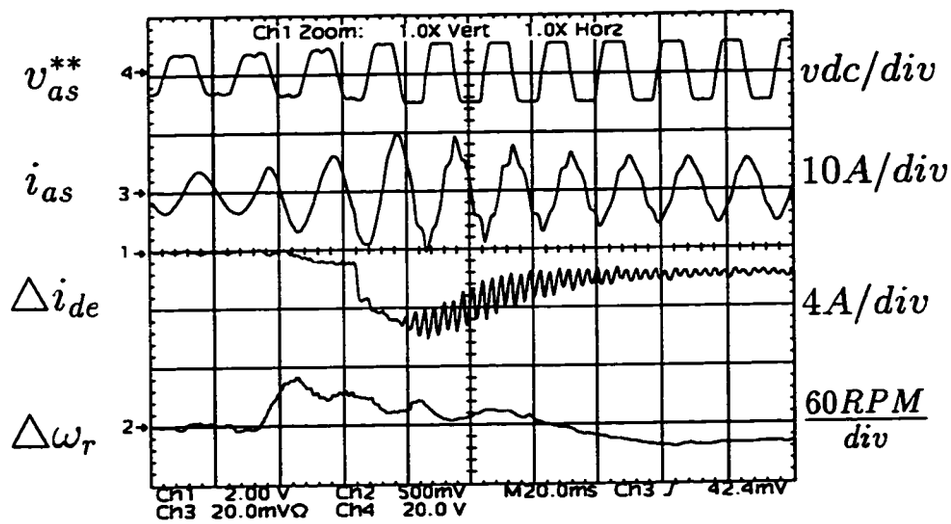

Figure 5.43: SVPWM modulation signal, phase current, d axis current error, and speed error oscillograms.

fact that the drive bandwidth is small (the proportional and integral gains are small) and the antiwindup controllers limit the reference voltage vector magnitude to be only slightly larger than the hexagon boundary (relatively small modulation index values). As all modulators have small phase and magnitude error for small modulation index values, the response is slow and takes several fundamental cycles. Over such a long period the fundamental component gain concept is valid in predicting the performance. With the modulation signals limited to the neighborhood of the hexagon, the voltage gain values of the discussed modulators are comparable, therefore the settling time of the speed controller (or the average response time) is practically the same in all the modulators tested in the laboratory. However, as illustrated, the maximum error and oscillations are different, and determined by the modulator characteristics.

Since the dynamic overmodulation behavior is dependent on the position of the voltage vector immediately before the transient (i.e. the rotor position at the triggering instant), randomly triggering the dynamic overmodulation mode results in slight differences in the dynamic performance. If the reference vector is closer to the hexagon sides than the middle, initially there exists more voltage to manipulate the dynamics (same in any segment). Therefore, the dynamic behavior is dependent on the initial (previous to dynamic overmodulation) position of the reference vector phase angle. However, with the experimental system having a relatively low bandwidth, and the dynamics lasting significantly longer than a time period corresponding to a hexagon segment, the triggering instant

of the dynamic overmodulation condition had little effect on the transient period and the peak speed ripple. Therefore, the initial conditions deserve less attention than the overall dynamic behavior. A large number of dynamic overmodulation tests triggered at different voltage vector spatial positions indicated the triggering point sensitivity of the dynamics was negligible. Therefore, the remaining experiments were conducted with no significant attempt to repeat the same exact initial conditions in each case.

Although the experimental system could not exhibit a true IFOC performance due to the inaccuracy involved in measuring the rotor angle, the experiments were sufficient to illustrate the modulator dependent dynamic overmodulation behavior of the drive. With a high bandwidth controller and accurate rotor angle measurement, the modulator characteristics could be illustrated into more detail, as the simulation results indicated.

The experimental results of this section clearly illustrated the influence of the modulator phase and magnitude characteristics on the drive dynamic performance in the overmodulation region. The experiments suggest the SVPWM has better performance than DPWM methods, and DPWM2 in particular performs poorly and may render the drive unstable. It is apparent that combining several modulators and in the overmodulation region selecting a higher performance modulator will yield a high dynamic performance. While in the linear modulation region, GDPWM or a DPWM method of choice can be selected for low switching losses. During dynamic overmodulation, SVPWM or other

methods discussed in the simulation section could be selected. Such a hybrid algorithm could be successfully implemented in modern digital platforms and result in an overall high performance drive.

5.8 Steady State Overmodulation In Current Controlled Drives

As the previous chapter illustrated, voltage feedforward drives could be successfully operated in the overmodulation region. However, the dynamic performance and steady state output voltage/current waveform quality of the drive would degrade in the overmodulation region. As the overmodulation region is entered, the PWM output voltage begins to contain a considerable amount of subcarrier frequency harmonic content. The waveform distortion rapidly increases with the modulation index, and becomes maximum at the six-step operating point. The degree of performance loss is secondarily dependent on the modulator type and as clearly illustrated, DPWM methods are superior to all other modulators. With the overmodulation performance of voltage feedforward drives being limited, certain applications involving such drives may limit the drive maximum output voltage to a value smaller than the six-step voltage value (a modulation index smaller than unity). As the theoretical and experimental investigations indicated, all high performance modulators (including DPWM methods) exhibit rapid performance deterioration after approximately 0.95 modulation index. In

waveform distortion sensitive applications this approximate value may be utilized as the maximum modulation index limit. As a result, voltage feedforward controlled drives can be operated in the overmodulation region and power electronics devices of the inverter can be utilized at high capacity and the drive can perform in a wider operating range with improved DC bus voltage disturbance rejection. In high performance current regulated drives, however, the overmodulation region is less efficiently utilized than in voltage feedforward drives.

As the dynamic overmodulation studies of this chapter indicated, in the overmodulation region, current controlled drives exhibit strong interaction between the modulator and the current controller (and possibly outer control loops also). This interaction results in significant current, torque, and speed oscillations and degrades the performance. As the simulations and experimental investigations illustrated, dynamic overmodulation performance of current controlled drives could be enhanced by employing antiwindup controllers, careful current controller design, and proper modulation algorithm choice. Regardless of the controller type and performance, however, the overmodulation performance remains inferior to the linear modulation region performance.

Due to the high performance motion quality requirements, in most current controlled drives the intended steady state operating region is the linear modulation region and the overmodulation region may only be entered during transients. However, in certain applications steady state operation in the overmodulation may be allowed. For most electric motor drives steady state

overmodulation occurs at high shaft speed, and the torque ripple generated due to overmodulation harmonics could be sufficiently suppressed by the shaft inertia and speed regulation can be satisfactory. In particular, this is true for induction motors with relatively large leakage inductance. Since the leakage inductance suppresses the overmodulation harmonic currents, with higher leakage inductances the associated torque ripple is relatively small. Perhaps, PM motors with small leakage inductance values would have significant harmonic current and the associated torque ripple would be prohibitive in certain applications. Therefore, current controlled AC motor drives with moderate high speed regulation requirements and suitable motor characteristics could be operated in the overmodulation region not only during transients, but also at steady state (at least in the lower overmodulation region). In this section the performance issues of current controlled drives when operating in the overmodulation region at steady state will be investigated.

While within the linear modulation range, the steady state voltage and current waveform characteristics of an SFCR controlled drive are the same as the voltage feedforward drive for the same modulator and operating conditions. However, in the overmodulation region the SFCR controlled drive (with or without current controller antiwindups) exhibits poorer steady state performance than the voltage feedforward type. This performance degradation is due to the fact that the feedback currents affect the current controller performance.

In voltage feedforward drives when operating in the overmodulation region,

the overmodulation harmonics result in current harmonics at their associated frequencies. In particular, the first few harmonics, the 5th, 7th, 11th, and 13th are large in magnitude. They induce torque ripple that results in speed oscillations and performance degradation. Since the $\frac{V}{f}$ controller and the modulator are feedforward no additional dynamics are generated. In current controlled drives, however, the feedback current overmodulation harmonics affect the drive performance significantly. As they are fed to the proportional and integral blocks of the controller, the controller generates modulation signals with overmodulation harmonic components and oscillatory behavior results. Intelligently designed antiwindup controllers partially limit these voltages and the associated oscillations. However, they introduce additional voltage nonlinearity to the drive and limit the voltage range of the drive. It is apparent that for superior steady state overmodulation performance of current controlled drives, the overmodulation harmonic currents should be removed from the measured feedback current. In addition the modulator fundamental component voltage gain loss in the overmodulation region could be compensated by employing the inverse gain compensation technique. However, both modifications degrade the drive dynamic overmodulation performance. Inverse gain compensation increases the current controller overshoot and eliminating the overmodulation harmonics from the feedback currents by filtering techniques increases the controller delay. Also, with the overmodulation harmonics absent from the feedback path, the current controller can no more provide inherent overcurrent protection. The above discussions clearly illustrate the trade-off between the steady

state and dynamic overmodulation performance of the current controlled drives. Therefore, steady state overmodulation of most current controlled drives in the overmodulation is limited to less than 0.95 modulation index (in particular, for drives employing motors with relatively small leakage inductances) and the effect of the overmodulation harmonics is only suppressed by the antiwindup controllers. This performance limitation is valid for all the carrier based and on-off current controllers. Therefore, the discussion involving the high performance SFCR is sufficient. However, it should be noted, on-off current controllers such as the hysteresis current controller have inferior steady state overmodulation and superior dynamic overmodulation performance to SFCR. In the following, a simulation study will attempt to illustrate the steady state overmodulation performance issues of current controlled drives and describe a method to provide enhanced steady state current controlled drive performance. Perhaps, such studies are necessary to initiate thoughts for developing current controllers with better overall characteristics than the conventional current controllers.

5.8.1 A Simulation Study of Steady State Overmodulation

In this section, the current controlled drive steady state performance will be investigated by a computer simulation. For the sake of simplicity, a simple three phase load consisting of resistance, inductance, and sinusoidal voltage connected in series (per phase) will be simulated. The load parameters are

$L_\sigma = 12.79mH$, $R_\sigma = 0.4425ohm$, $f_e = 60Hz$, and $E_{max} = 310.0V$. A digital SFCR with once per carrier cycle synchronous sampling and PWM write-out rates will be employed. The carrier frequency is 5 kHz. Except for the antiwindup controllers, the current controller is designed in the same manner as for the simulations in the dynamic overmodulation study. In the simulation, the current controller does not employ any antiwindup on the PI controller such that the influence of overmodulation harmonics on the drive performance could be clearly observed. The DC bus voltage of the inverter is fixed at 620 V. Only the DPWM1 method is simulated.

The system is first operated at 0.933 modulation index until $t = 0.1s$ (with $E_{max} = 365V$ an overmodulation condition is created), then the d axis current command is stepped up to a value to yield approximately a modulation index of 0.975. Figure 5.44 shows the corresponding current, modulation, and controller signal waveforms during overmodulation. As the figure indicates, in particular in the higher overmodulation region, the currents contain large amount of overmodulation harmonics. The PI controller signals are oscillatory and they generate modulation waves with no quarter-wave symmetry. Hence, increased current harmonic content and oscillatory behavior compared to an open loop overmodulation operating condition.

In Figure 5.45, a small portion of the previous figure is shown. Generated from the synchronously sampled phase currents, the d and q axis currents, labeled in the figure as IQSE, and IDSE, have significant ripple, mainly at $6f_e$

frequency. Since the 5th and 7th overmodulation harmonics form a 6th harmonic in the synchronous frame, this result is to be expected. The PI controllers respond to these harmonics and generate modulation signals with such harmonic components and the modulator quarter-wave symmetry is lost. Figure 5.46 provides a more detailed view of the modulation and phase current waveforms at $M_i = 0.933$. It is clear from the figure that the modulation wave is not quarter-wave symmetric. Operating at higher modulation indices (as the 0.975 modulation index case illustrated) increases the asymmetry and the distortion, such that the performance is unacceptable. Therefore, without proper structural modifications, the SFCR controlled drive can not successfully operate in the higher overmodulation region at steady state.

5.8.2 Steady State Overmodulation Performance With Feedback Current Harmonic Reduction

Having demonstrated the steady state overmodulation performance deficiency of the SFCR controlled drive in the previous section, we next investigate the performance of such a drive when the overmodulation harmonics are eliminated from the feedback path of the controller. An overmodulation harmonic current estimation method will be developed and the estimation method will be employed in eliminating the harmonic currents from the controller feedback simulated in the previous section. The simulation results will be evaluated and compared to the previous case.

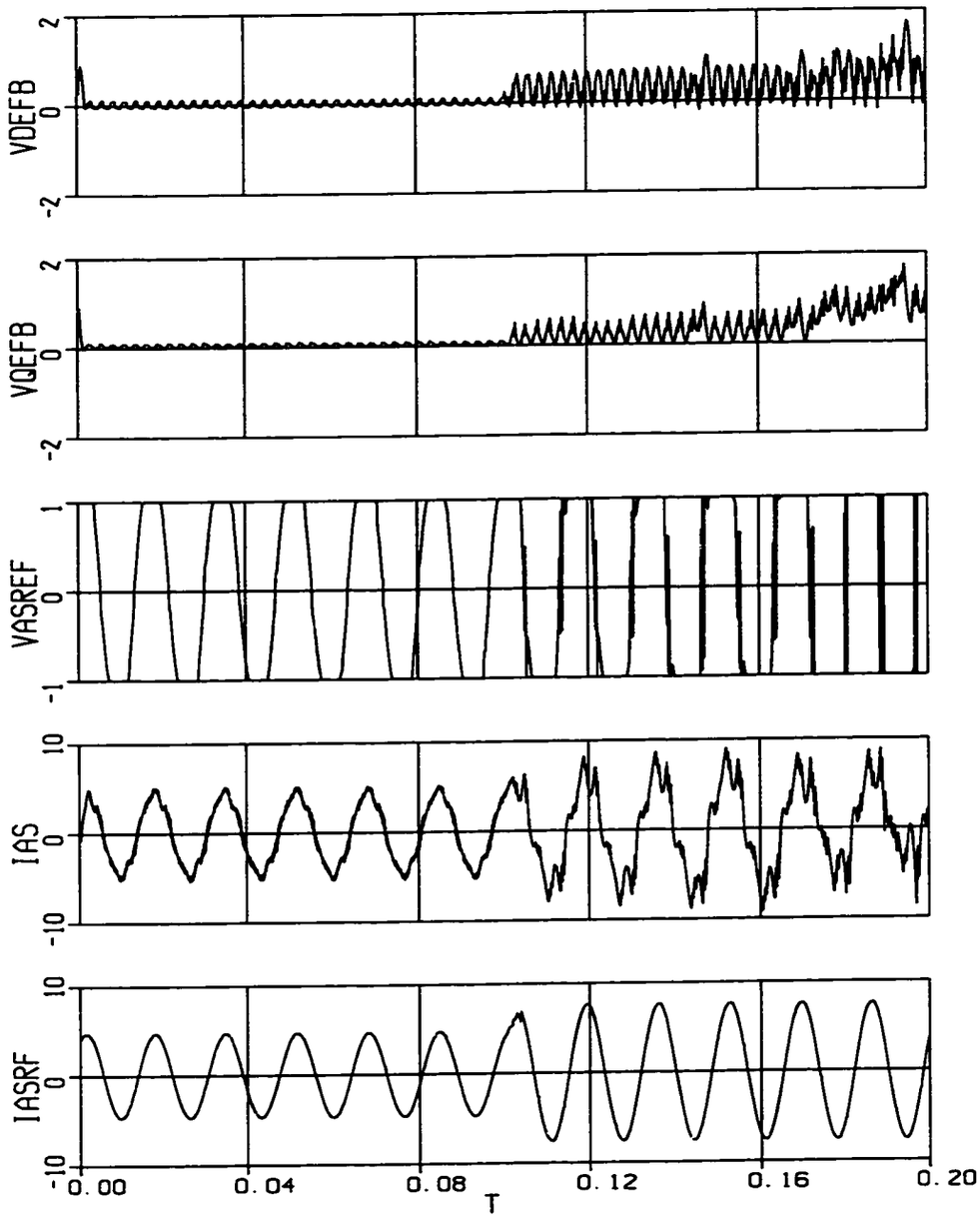

Figure 5.44: SFCR based system simulation waveforms in the overmodulation range. Traces (bottom to top): reference and actual phase currents, DPWM1 modulation wave, q and d axis PI controller outputs. At $t = 0.1s$, M_i is increased from 0.933 to 0.975.

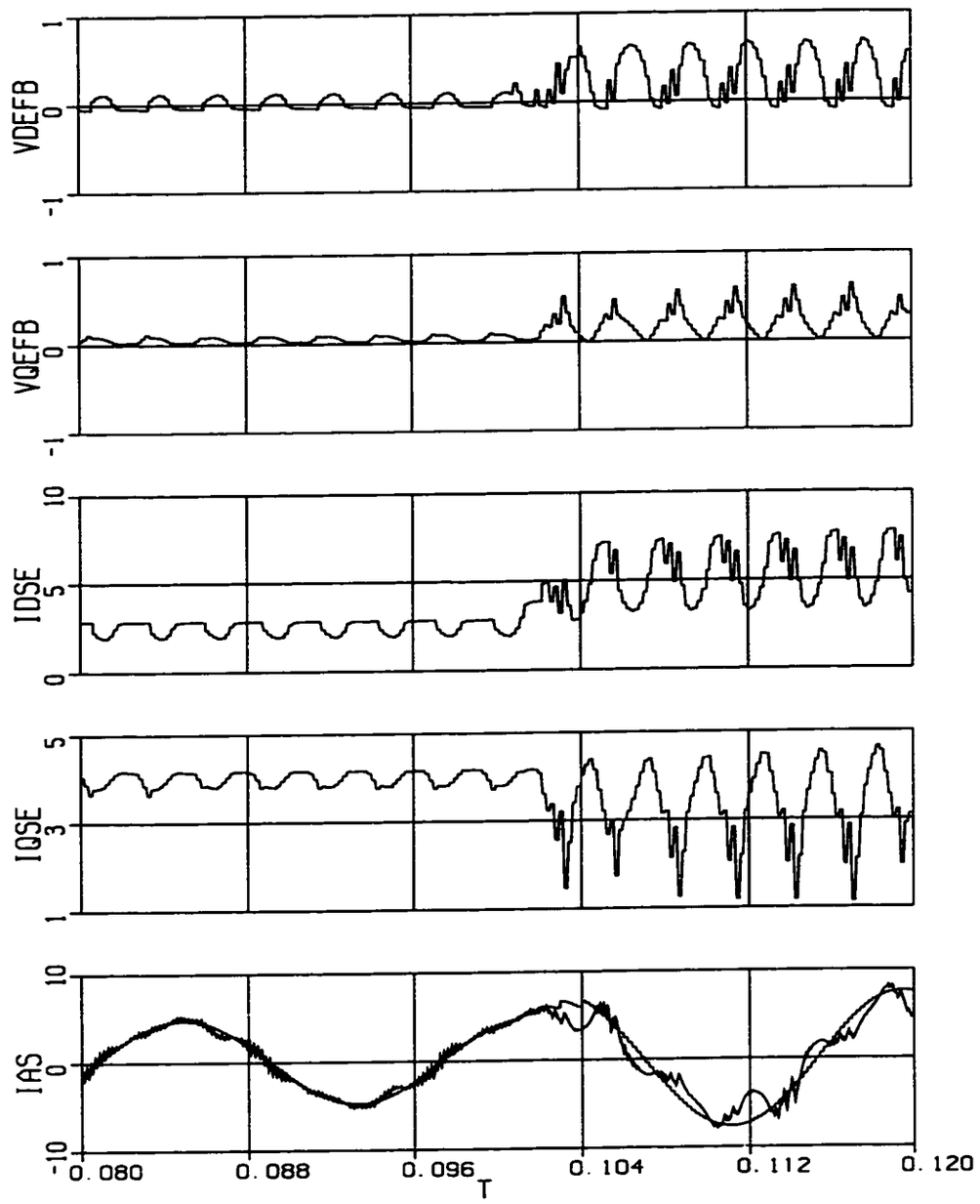

Figure 5.45: Detailed view of the system characteristic waveforms in the over-modulation range. Traces (bottom to top): reference and actual phase currents, discretized q and d axis currents, q and d axis PI controller outputs.

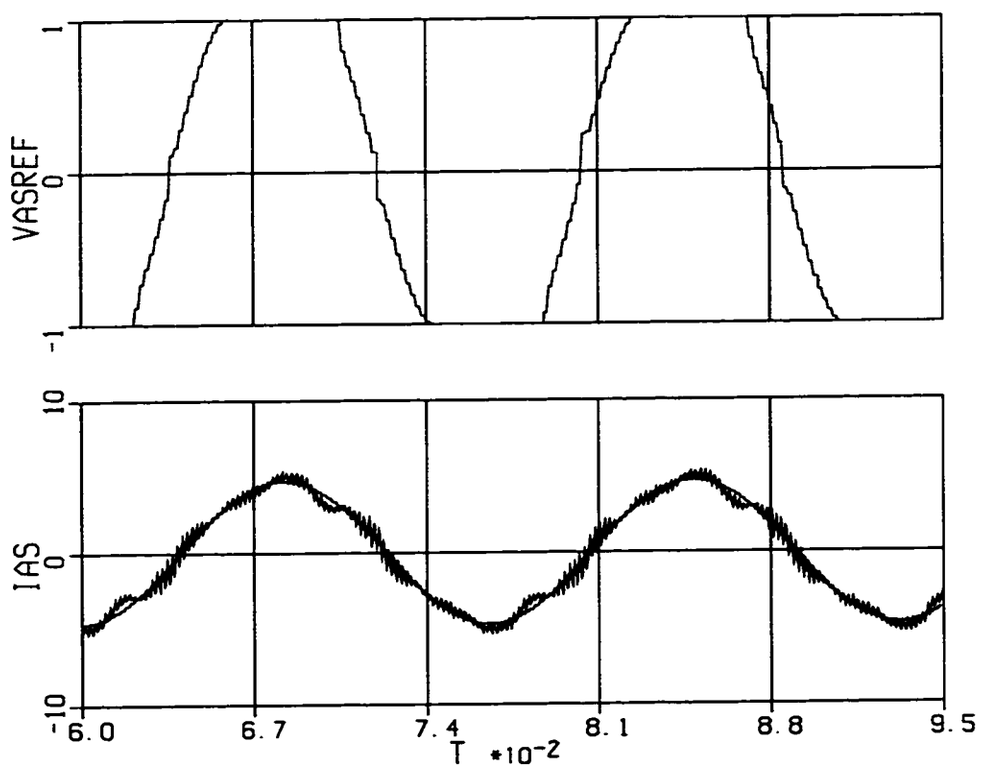

Figure 5.46: Zooming into the phase current and modulation wave at M_i = 0.933. Traces (bottom to top): reference and actual phase currents, and DPWM1 modulation wave.

In this work, a reference model based harmonic estimation method is developed. The induction machine harmonic behavior can be modeled by its transient impedance circuit [108, 145]. Figure 5.47 shows the induction machine constant flux model, and harmonic equivalent circuit. The motor harmonic equivalent circuit model can be represented in any reference frame. For this application, the synchronous frame equivalent circuit is suitable. If the AC motor harmonic voltages are known, then the corresponding d and q axis harmonic currents can be estimated from the harmonic equivalent circuit as follows.

$$i_{qeh}(t) = \int_0^t \frac{v_{qeh}(t) - r_\sigma i_{qeh}(t) - w_e L_\sigma i_{deh}(t)}{L_\sigma} dt + i_{qeh}(0) \qquad (5.18)$$

$$i_{deh}(t) = \int_0^t \frac{v_{deh}(t) - r_\sigma i_{deh}(t) + w_e L_\sigma i_{qeh}(t)}{L_\sigma} dt + i_{deh}(0) \qquad (5.19)$$

Figure 5.48 shows the harmonic estimation based system controller block diagram. Figure 5.48(a) shows the current regulator structure, including the fundamental component gain compensation scheme. The low pass filter (LPF), provides a smooth gain compensation signal and helps estimate the overmodulation harmonic voltage signal. As shown in Figure 5.48(b), the overmodulation harmonic voltages are estimated from the modulator input and output waveforms. In the overmodulation region, the modulator output signal is saturated and has a lower fundamental component magnitude than the reference. When the inverse gain compensation technique is involved, the original modulation signal and the modulator output signal have the same fundamental component.

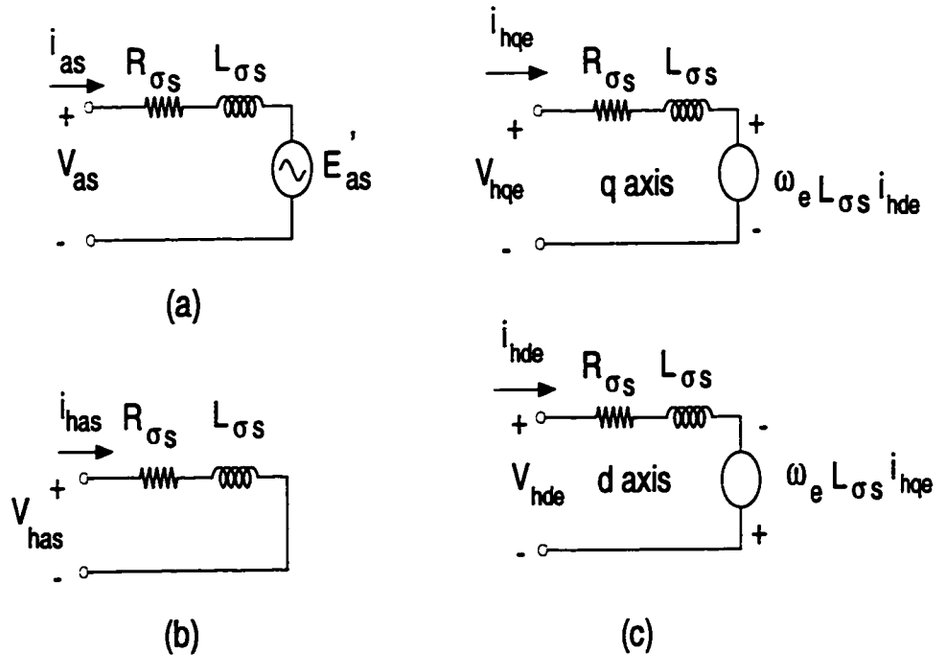

Figure 5.47: Three phase AC induction motor transient and harmonic equivalent circuits; (a): Per phase fundamental component transient model, (b): Per phase harmonic model, (c): Harmonic model in the synchronous frame.

Therefore, the difference between the original modulation signal and the output modulation signal equals the overmodulation harmonic voltage. In case of inaccurate inverse gain compensation, the estimation will include a fundamental component also. Therefore, additional filtering to block the fundamental component voltage is required for accurate harmonic voltage estimation. As will be shown in the simulations, a single frequency band pass filter (BPF) tuned to the dominant $6f_e$ component and implemented in the $6f_e$ frame provides satisfactory results. In Fig. 5.48 (c), the overmodulation harmonic current, and fundamental component current estimation block diagrams are illustrated. Employing the synchronous frame harmonic equivalent circuit and the estimated synchronous frame harmonic voltages, the overmodulation harmonic currents can be easily computed. Subtracting the estimated harmonic currents from the synchronously sampled and d-q transformed currents, the synchronous frame fundamental component currents can be found. The accuracy of the discussed harmonic current estimation scheme depends on the knowledge of machine parameters. Parameter inaccuracy, computational accuracy, etc. factors can strongly affect the overmodulation harmonic current prediction accuracy. However, at this stage the accuracy and implementation issues of the overmodulation harmonic current prediction algorithm will be omitted.

The overmodulation harmonic feedback current reduced current controller scheme has been simulated to illustrate its superior steady state overmodulation performance. The same load, inverter, and controller parameters as the previous case are assumed. The overmodulation harmonic estimator computes

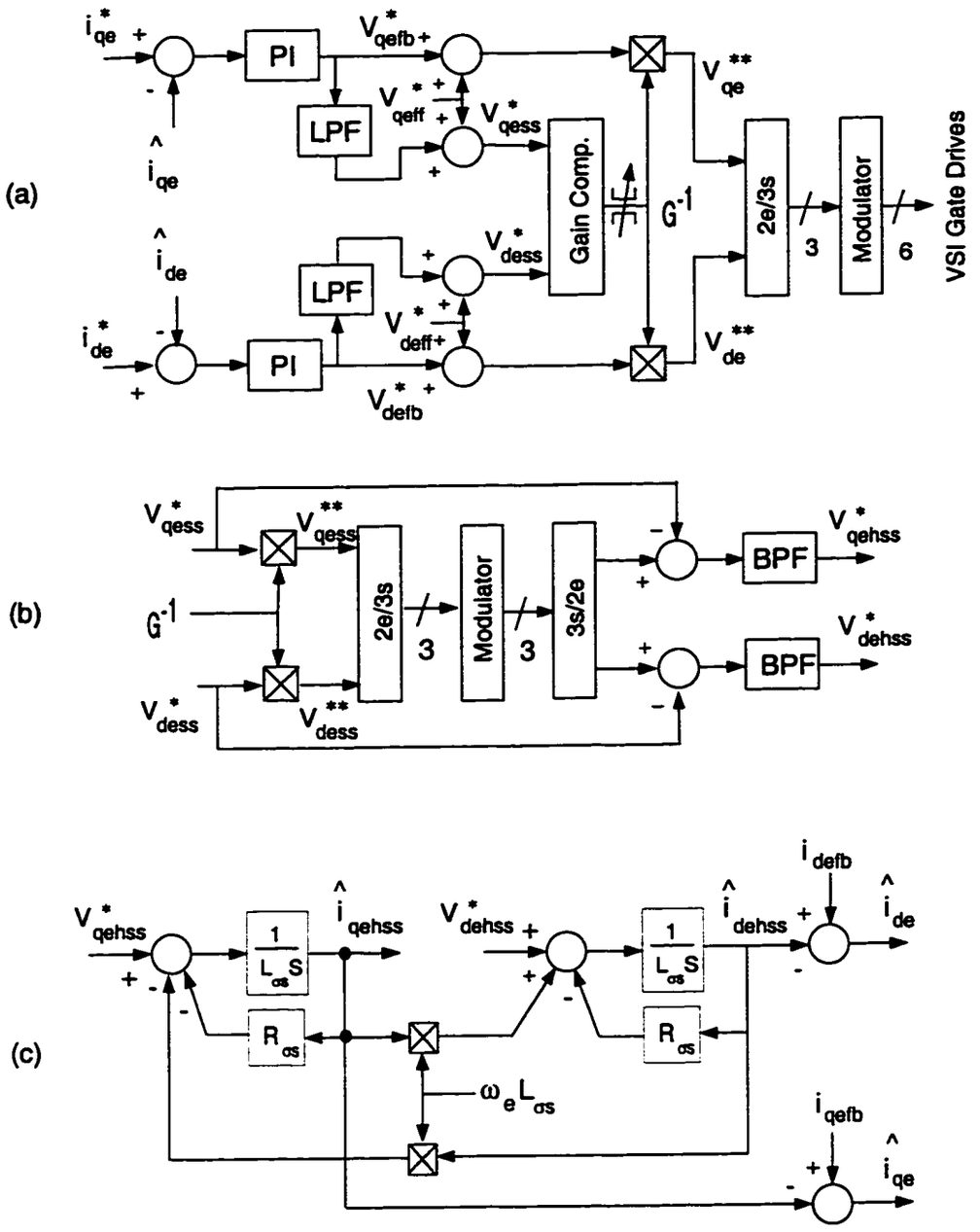

Figure 5.48: The SFCR drive with overmodulation harmonic estimation algorithm. (a): Current regulation algorithm including the gain compensation block, (b): Overmodulation harmonic voltage estimation block diagram, and (c): Overmodulation harmonic current estimation block diagram.

the signals once per carrier cycle. Once the reference voltage signal is computed (at the beginning of the cycle), the estimator predicts the harmonic current value at the end of the associated carrier cycle. Figure 5.49 shows the simulation waveforms of the harmonic reduced system. The system is operated at 0.933 modulation index(at $t = 0$ all the currents are zero) for 0.1 s. Then the d axis current reference is stepped to a value corresponding to 0.965 modulation index. As the figure indicates the current regulator provides improved steady state current waveform. With the absence of the dominant overmodulation harmonics from the feedback, the PI controller output signals are less oscillatory and the operation is less oscillatory. Zooming into the figure, it can be seen in Figure 5.50, the synchronous frame d-q axis discretized currents are not as oscillatory as the previous case (Fig. 5.45). Including more detail, the waveforms in Fig. 5.51 indicate the steady state performance superiority of this controller. The modulation waveform has quarter-wave symmetry and the phase currents are more sinusoidal than the previous case.

This section illustrated high performance SFCR based drives have significant performance issues in the overmodulation region. Without PI controller antiwindups, current controllers exhibit poor steady state and dynamic performance in the overmodulation region. Employing antiwindups on the PI current controllers aids manipulating dynamic overmodulation conditions without significant current oscillations. Steady state operation of an SFCR based drive with or without antiwindups in the overmodulation region results in higher

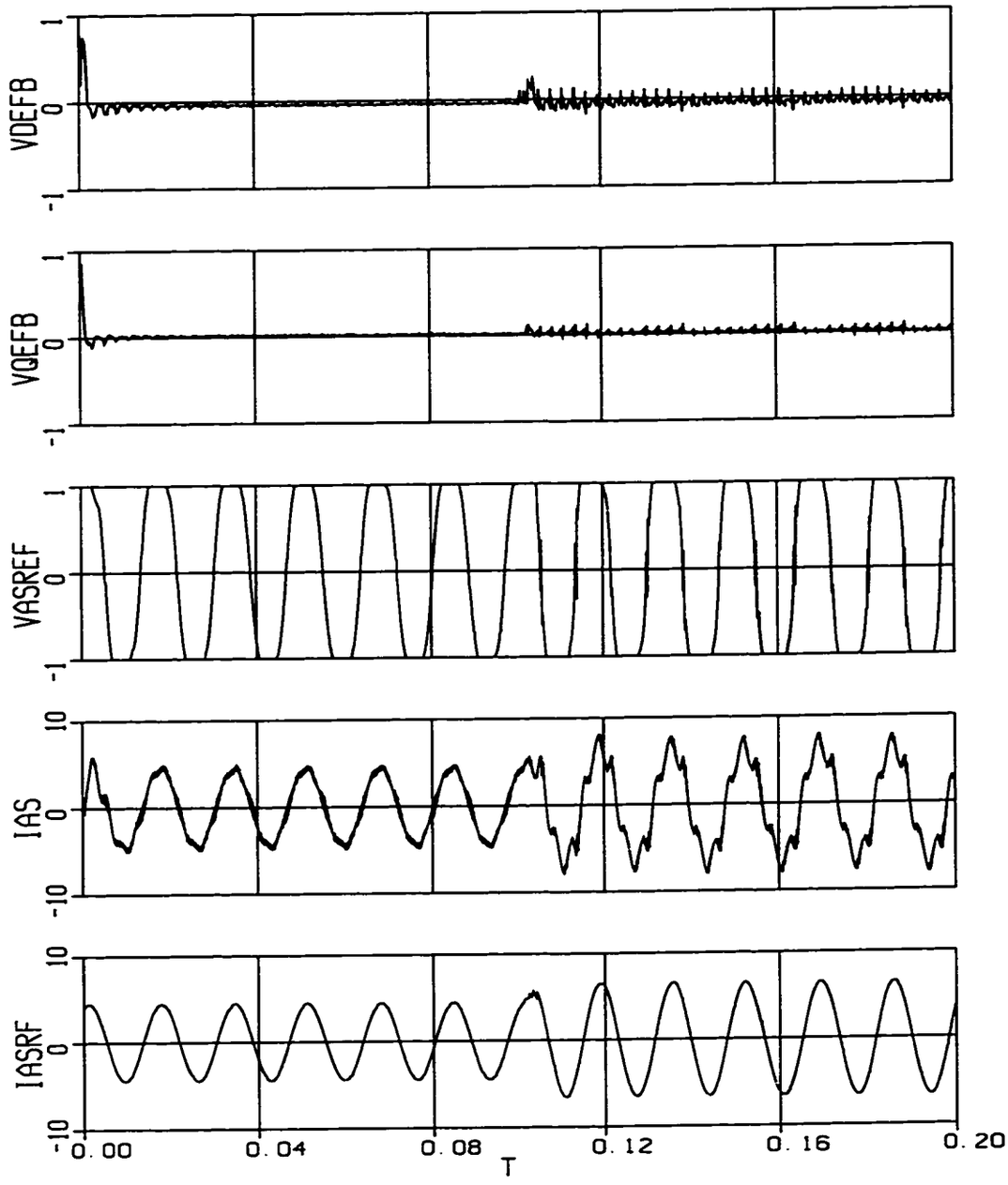

Figure 5.49: Harmonic feedback reduced, SFCR based drive simulation waveforms in the overmodulation range. Traces (bottom to top): reference phase current, actual phase current, modulation wave, q and d axis PI controller outputs. At $t = 0.1s$, the modulation index is increased from $M_i = 0.933$ to $M_i = 0.965$.

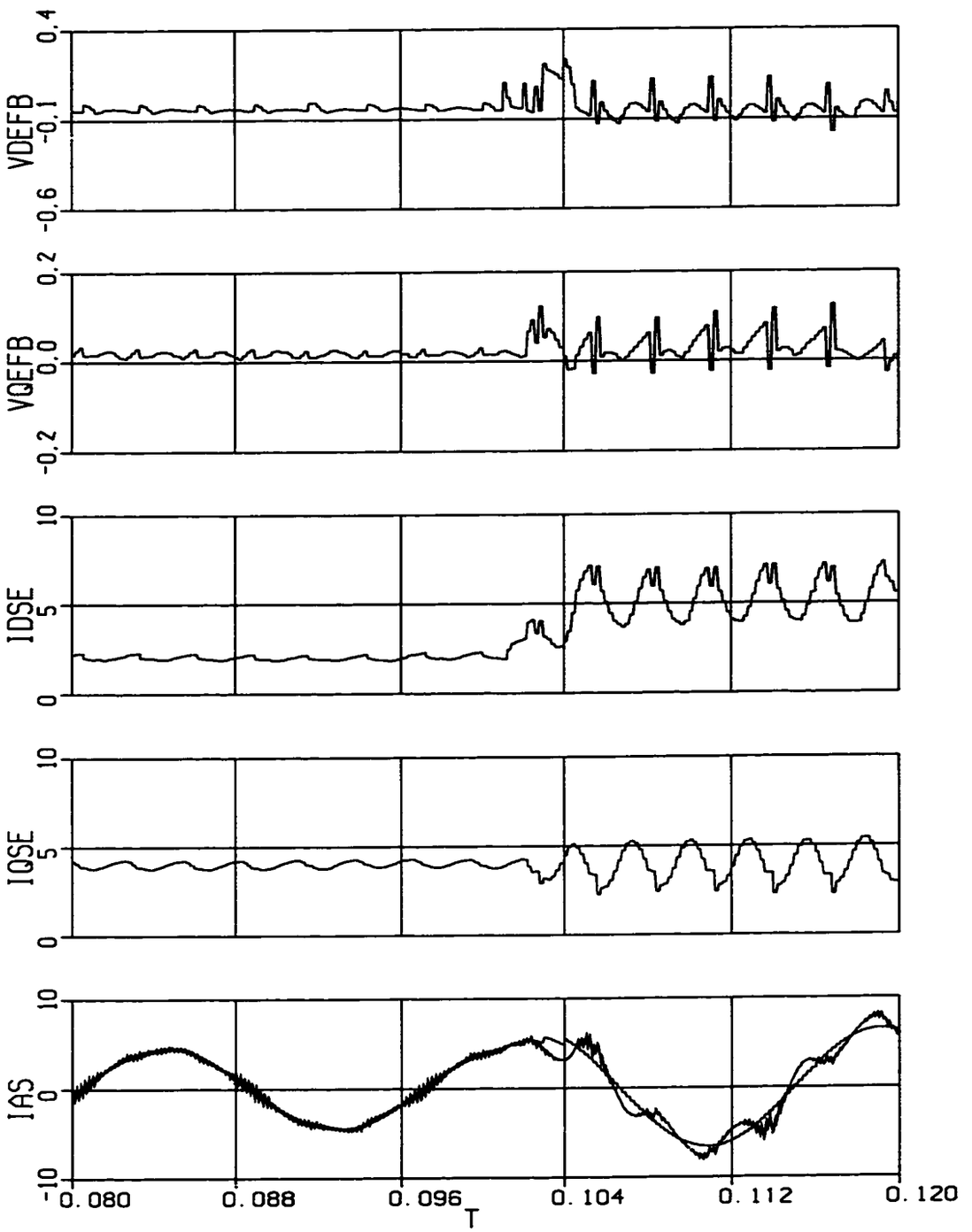

Figure 5.50: Detailed view of the system characteristic waveforms in the over-modulation range. Traces (bottom to top): reference and actual phase currents, discretized q and d axis currents, q and d axis PI controller outputs.

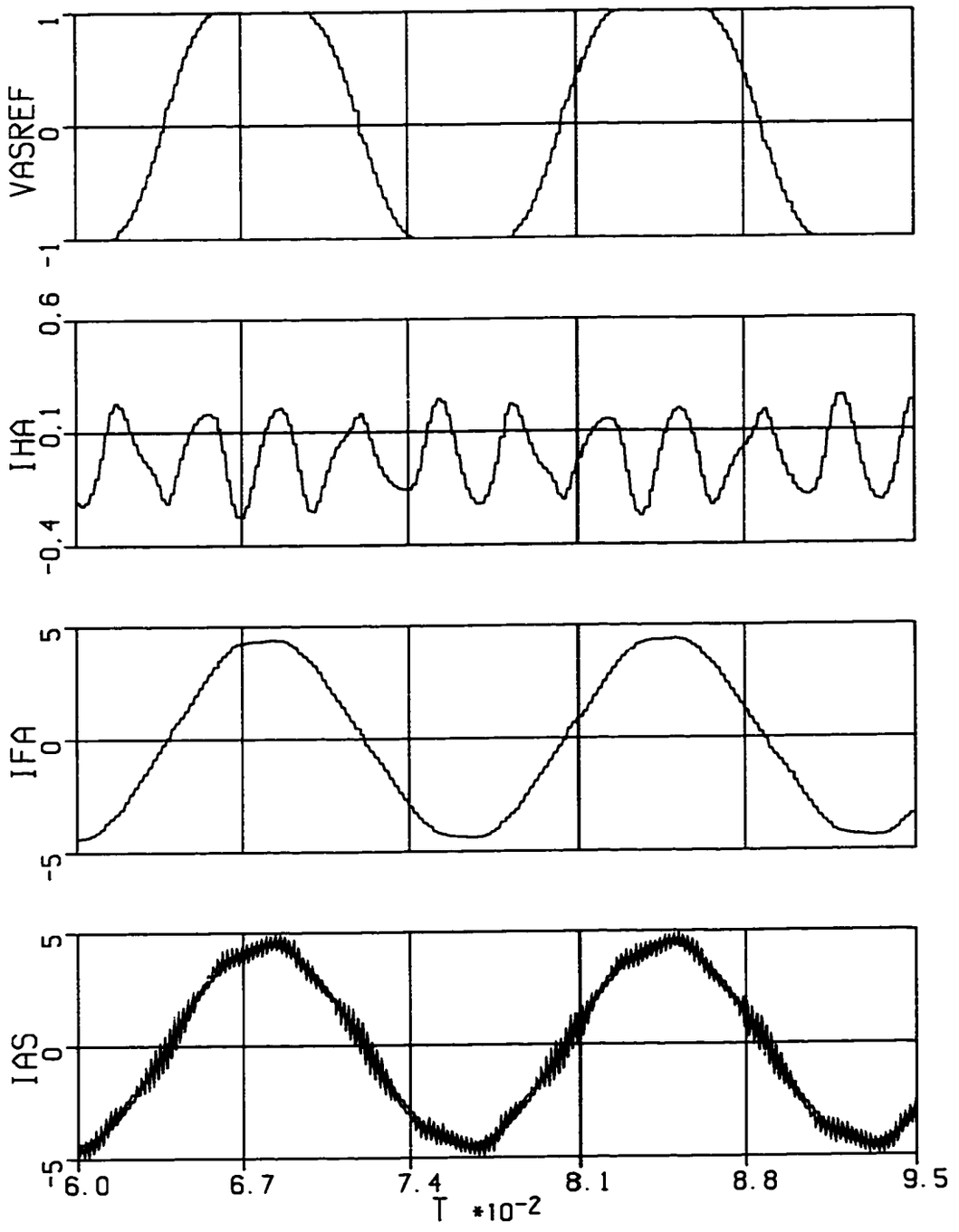

Figure 5.51: Zoomed view of the phase current and modulation wave at $M_i = 0.933$. Traces (bottom to top): reference and actual phase currents, estimated fundamental component and harmonic currents, and DPWM1 modulation wave.

overmodulation harmonics than voltage feedforward drives for the same operating point. The steady state performance of an SFCR based drive can be enhanced by removing the overmodulation harmonic feedbacks from the controller. However, this approach requires filtering and the dynamic performance reduction due to the introduction of such filters is generally prohibitive. Although the implementation difficulties can be overcome with high performance digital signal processors, the inherent delay of the filters is prohibitive from the performance perspective. As a result, most drives only employ antiwindup controllers and the dynamic performance is retained. Although their presence limits the voltage utilization and steady state operating range of a drive, antiwindups are invaluable for they manipulate the dynamics safely. The simulation study of this section illustrated the poor steady state overmodulation performance characteristics of current controllers and aided in understanding the problem. Therefore, it becomes clear, the overall overmodulation region performance of current controlled drives is limited.

Perhaps, the steady state modulation limit of an SFCR based drive with antiwindup and with a high performance modulator could be estimated by calculating the modulation index corresponding to an operating condition which forces the inverter output vector follow the hexagon sides. This condition corresponds to the minimum (zero) phase error method developed for direct digital PWM overmodulation [58] and illustrated in Fig. 5.6 with the tip point "a" in detail. Projecting the reference voltage vector on the "q" axis of the complex

plane, the q axis AC voltage signal can be found and the fundamental component voltage magnitude can be closed form calculated. Expressed in terms of modulation index, the resulting maximum steady state voltage utilization is as follows.

$$M_{imaxa} = (\frac{\sqrt{3}}{2})ln(3) \approx 0.9514 \tag{5.20}$$

This operating point also corresponds to the practical breakthrough point for the rapid increase of the overmodulation harmonics. Although some applications may require smaller or wider operating range, the authors experience indicates the 0.95 modulation index limit generally represents the rapid performance degradation point and it is the typical performance boundary for many industrial current controlled drives with moderate performance requirements.

5.9 Summary

Dynamic overmodulation and steady state overmodulation issues are different and the modulator fundamental gain characteristics are not a sufficient performance measure to evaluate the dynamic overmodulation performance. An elegant approach is the characterization of the reference and modulator output voltage vector angle and magnitude relations. A simple technique provides analytical tools to obtain these characteristics. Each triangle intersection PWM method is shown to have a unique dynamic overmodulation characteristic. The

investigation reveals the minimum voltage magnitude error dynamic overmodulation attribute (one-step-optimal) of SVPWM method, indicating a significant implementation advantage compared to the two methods reported to achieve such performance. In a motor drive, motion quality is more important than rapid current control and the high performance phase error regulation approach is superior to the inherent overmodulation characteristics of the modern PWM methods. For intermediate dynamic overmodulation performance SVPWM provides satisfactory performance and for high dynamic overmodulation performance a phase error regulation method is adapted from the direct digital PWM technique to enhance the dynamic overmodulation characteristics of the triangle intersection PWM methods. In both methods the antiwindup limiters play an important role in keeping the phase error small and maintaining high dynamic performance. The theoretical modulator dynamic overmodulation characteristics were verified by detailed computer simulations and laboratory experiments.

This chapter also illustrated the steady state overmodulation performance deficiency of current controlled drives. Detailed computer simulation studies illustrated the overmodulation harmonic currents affect the current controller through the feedback channels and the performance degrades. As a result the steady state overmodulation performance of current controlled drives is inferior to voltage feedforward drives. Current controlled drives with antiwindups provide approximately a maximum steady state operating point of 0.95. Although their operating range is narrower than the voltage feedforward drives, current controlled drives manipulate dynamic conditions more rapidly and safer.

Chapter 6

Conclusions and Future Work

This thesis has involved a detailed study of high performance PWM methods for three phase voltage source inverters and it was developed in two stages.

The first stage of the thesis involved a detailed analysis of linear modulation range waveform quality and semiconductor device switching loss characteristics of modern PWM methods. The rigorous analysis and detailed graphical illustrations of multivariable modulator functions provided improved insight to modulator behavior. The study provided simple analytical methods and tools for modulator design. Simple techniques for generating the modulation waves of the high performance PWM methods were described. Most importantly, the study aided the development of the high performance GDPWM method with on-line performance optimization capability. In addition, the thorough analysis established the basic knowledge for the second and dominant portion of this thesis.

The second stage of the thesis involved the overmodulation region performance study of AC drives employing the modern PWM methods. First the

voltage linearity limits were investigated and then the overmodulation characteristics were studied. The overmodulation region fundamental component voltage gain characteristics, and the per carrier cycle modulator phase and magnitude error characteristics were rigorously analyzed. As the overmodulation characteristics of modern modulators were clearly understood, the following step involved the study of AC drive behavior employing such modulators. The overmodulation region steady state and dynamic performance of AC motor drives and utility interfaces was thoroughly investigated. Both voltage feedforward drives and closed loop current controlled drives were considered. Strong correlation between theory, computer simulations, and laboratory tests was obtained. The overmodulation studies of this thesis illustrated the steady state and dynamic performance issues of various modulators and aided the modulator selection and design procedure. Furthermore, control algorithms with superior overmodulation region performance were developed and verified. As a result, it was shown improved inverter utilization and superior overmodulation region performance could be obtained by only moderate software modifications to the state of the art PWM-VSI drives.

6.1 Conclusions

The most significant contributions and conclusions of this thesis can be itemized in the following paragraphs.

Modern modulation methods were separated into two groups; the continuous PWM and discontinuous PWM methods. A thorough investigation indicated the equivalency of various modulation methods, and an attempt to unify the modern modulation methods successfully reduced their count to less than a handful. Employing the magnitude rules, modulation signals of all the modern modulators could be easily generated by means of software/hardware. The difficulties encountered in learning the behavior of large number of modulation methods, and selecting and implementing one among them, are greatly overcome with these classifications and generalizations.

The analytical modulator waveform quality and switching loss formulas, and the graphic illustration of these multivariable functions significantly simplify the modulator design stage of drives employing modern PWM methods. These formulas and graphics provide substantial amount of information on the modulator behavior. Therefore, they are invaluable PWM learning tools.

The waveform quality and switching loss comparisons indicated near zero modulation index region CPWM methods are superior to DPWM methods. However, in the remainder of the voltage linearity region the opposite is true.

A high performance GDPWM method with on-line controllable characteristics was developed and its characteristics analytically investigated. Simple to implement, GDPWM could be closed loop controlled to maintain high drive performance as opposed to the conventional modulators with predefined and operating point dependent performance characteristics. With GDPWM, reduced

switching losses, wide voltage linearity range, and high waveform quality could be obtained in a wide operating range. Since the near zero modulation index range performance of SVPWM/SPWM is superior to GDPWM, a simple modulation algorithm which selects SPWM or SVPWM in the lower modulation index range, and GDPWM in the remainder of the voltage linearity region, was established and tested in the laboratory. As the GDPWM control variable, the modulator phase angle was controlled in a manner to minimize the switching losses.

When combining several modulation methods in a modulation algorithm, the modulation indices at which the transitions occur could be accurately calculated (based on a selected performance criteria) by employing the analytical HDF and SLF functions.

The overmodulation region fundamental component voltage gain characteristics of modern PWM methods were analytically investigated. Comparisons indicated DPWM1 has significantly higher gain than the remainder of the modulators. The overmodulation region waveform quality investigation indicated DPWM methods are superior to CPWM methods until approximately 0.95 modulation index. Beyond this limit, the waveform distortion rapidly increases with both modulator groups. With the voltage feedforward drives requiring high fundamental component voltage gain, and high waveform quality, the DPWM1 method was illustrated to be the most appropriate modulation method for such drives. Employing DPWM1 (as an operating point of GDPWM), and including

a voltage gain compensator (inverse gain compensation by means of polynomial approximation) and a DC bus voltage disturbance rejection controller (by on-line scaling the modulation index with the inverse of the normalized DC bus voltage), the overmodulation region performance of a voltage feedforward drive could be substantially enhanced. The laboratory experiments illustrated the superiority of this approach.

The influence of inverter blanking time and minimum pulse width control on the modulator linearity was studied in detail. It was shown that both have substantial effect on the waveform quality and voltage linearity. It was illustrated DPWM methods perform poorly near zero modulation index and both effects exacerbate the performance substantially. However, the maximum linear modulation index of DPWM methods is higher than the CPWM methods and it is less influenced by the blanking time and MPW.

When current controlled PWM-VSI drives operate in the overmodulation region, the modulator and current controller exhibit strong interactions and oscillatory drive performance may result. The degree of instability was shown to strongly depend on the modulator phase error characteristics. The phase error characteristics of all modern PWM methods were calculated and their influence on the dynamic overmodulation performance of AC a drive was studied.

The investigation revealed the minimum voltage magnitude error dynamic overmodulation attribute (one-step-optimal) of SVPWM method, indicating a significant implementation advantage compared to the two methods reported to

achieve rapid current regulation.

Due to its lagging phase error characteristics, the DPWM2 method forces strong current regulator dynamics, and leads to poor drive dynamic performance. Therefore, its utilization in the dynamic overmodulation range is prohibitive.

In a motor drive, motion quality is more important than rapid current control. For intermediate dynamic overmodulation performance SVPWM provides satisfactory performance. For high dynamic overmodulation performance a modulator phase error regulation method was adapted from the direct digital PWM technique to enhance the performance of the triangle intersection PWM methods.

Current controller antiwindup limiters maintain the modulator phase error at a small value such that the dynamic overmodulation oscillations are suppressed and overcurrent fault conditions are avoided. However, they limit the voltage utilization and delay the controller response. The practical voltage utilization limit with antiwindups is 0.95 modulation index.

Higher current controller gains result in larger phase errors, and larger oscillations. Therefore, the dynamic overmodulation performance issues of high bandwidth current controllers are significant. When designing a modulator for such drives, the dynamic overmodulation performance must be taken into account.

The steady state overmodulation performance of current controlled drives is inferior to voltage feedforward drives due to the influence of the feedback current harmonic components. Current controlled drives with antiwindups provide approximately a maximum steady state voltage utilization of 0.95. Although their operating range is narrower than the voltage feedforward drives, current controlled drives manipulate dynamic conditions more rapidly and safer.

Current controlled drives can employ SPWM/SVPWM near zero modulation index, and GDPWM until the maximum linear modulation index. In the overmodulation region, SVPWM or the phase error regulation methods may be selected for superior performance. Implementing such an algorithm on a modern digital control platform is a viable task.

The theoretical current controller dynamic overmodulation studies were supported by computer simulations and laboratory experiments and a strong correlation was obtained.

As a result, this thesis increases our knowledge about the PWM-VSI drives, and develops high performance modulation and control algorithms for superior drive performance. As the heart of the drive, the pulse width modulator was thoroughly studied, and well understood. The study aided the development of control methods yielding improved inverter utilization, lower waveform distortion, higher energy efficiency, and superior dynamic performance. To be discussed in the next section, however, several important performance issues of PWM-VSI drives remain to be addressed.

6.2 Future Work

There exists a large variety of PWM-VSI drive types and applications. This thesis could only focus on several of the many fundamental drive performance issues and resulted in several contributions to the field. However, substantial amount of effort is needed to overcome the remaining difficulties and perfect the PWM-VSI drives. Several issues relating to the subject of this thesis and PWM-VSI drives which need immediate attention can be summarized in the following.

The linear and overmodulation region performance of three-level and higher level PWM-VSI drives require a detailed analysis and performance enhancement. The approach followed in this thesis for analyzing the modern modulation methods developed for the conventional two level inverter can be extended to three and higher level inverters in a straightforward manner. The steady state and dynamic overmodulation performance of multilevel inverters with various modulators can also be investigated with the same approach.

The modulation methods described and/or reviewed in this thesis are a few intelligently programmed modulators and many more can be developed. One such modulator could have a periodically varying carrier frequency. For example, the carrier frequency can be a linear function of the zero sequence signal of the SVPWM method ($f_c = a \times V_0 + b$). In the proposed method, the carrier frequency variation increases with the modulation index because the zero sequence signal V_0 is proportional to the modulation index. Thus, at high modulation

index the carrier frequency significantly varies in space and at low modulation index it is practically fixed. Since at high modulation index the SVPWM harmonics become large and significantly vary in space (see Figures 3.15 and 3.16), employing the proposed scheme with SVPWM is advantageous. Varying the carrier frequency in this manner could reduce the harmonic distortion and spread the harmonic spectrum in a relatively wide frequency range. As a result, the audible noise could be reduced and/or the EMI performance could be enhanced. Although similar methods were reported in the literature [72], the proposed method has substantially simpler structure and can be easily implemented. Note that the method in [72] employs a large two dimensional table ($f_c = f(M_i, \theta)$), while the proposed method effectively employs a simple inverse model of the SVPWM harmonic distortion function. In the proposed method, selecting the two coefficients (a and b) appropriately is sufficient. Performance analysis and design of the proposed modulator requires appreciable effort.

The overmodulation performance of voltage feedforward controlled open loop drives could be substantially improved with a proper modulator choice and control method. This thesis established the fundamental design guideline for such drives. In this thesis current controlled drives have been investigated with greater effort. However, the current controlled system exhibits a highly nonlinear structure (due to voltage limits, antiwindup, motor dynamics etc.) and the results obtained in this thesis suggest further study is required in order to establish very high performance current controlled drives.

The current controlled drive overmodulation study of this thesis assumed the flux producing current reference (I^*_{de}) is constant. This assumption is valid within the base speed range of most drives, and only drives with field weakening capability reduce I^*_{de} with increasing speed. With this assumption, this thesis investigated the capability of the modulator and current controller regardless of the reference signals. However, with the induction machine rotor electrical time constant being large, the dynamic overmodulation performance could be further enhanced by modifying the flux current reference during a dynamic overmodulation transient. Assuming the rotor flux remains constant during the current controller transients, the flux producing current can be temporarily reduced (dynamic field weakening). With the flux current reference reduced, more voltage becomes available for torque current and the dynamics can be more rapidly manipulated. The method reported in [35] reduces I^*_{de} in proportion to the torque producing current error ($I^*_{deNEW} = I^*_{de} - K * (I^*_{qe} - I_{qe})$). However, a direct calculation of I^*_{de} based on the dynamic requirements may be possible. Therefore, a detailed study is required in order to determine the profile of I^*_{de} during dynamic overmodulation transients.

The GDPWM modulator phase angle also may be utilized as a control parameter to create the required dynamic field weakening condition. However, relations between the modulator phase angle and the field weakening level must be established. Alternatively a heuristically designed closed loop PI controller may regulate the phase angle. This subject also requires investigation and controller development and design.

The d and q channel antiwindups of the SFCR limit the current controller overshoot and delays. This performance is obtained at the expense of reduced voltage utilization. As a result relatively slow, however, controlled performance is obtained. On the other hand, during abrupt and long lasting transients (longer than the fundamental period associated with the electrical angular speed/frequency of the drive) it may be beneficial to operate the drive near or at the six-step operating mode so that the dynamics can be manipulated rapidly. Since the conventional SFCR structure with antiwindups does strongly limit the voltage utilization (to at most 95 %) and significantly high (prohibitive) controller gains are necessary to obtain full voltage utilization, a controller modification or a different controller type may be required for superior dynamic response. Perhaps, during dynamic overmodulation transients, a predictive controller with an accurate motor model could be utilized to calculate the feasible voltage vectors and guide the motor through the commanded motion trajectory with minimum disturbance and safely. Since the six-step mode yields 5 % higher voltage utilization than the SFCR with antiwindup, during long lasting transients this voltage margin may be sufficient to manipulate the transients in a substantially shorter time. A hybrid controller employing SFCR inside the inverter hexagon and a predictive controller in the overmodulation region could be designed to provide an overall superior drive performance. Designing such a control system requires a substantial effort.

A novel approach to enhance the overmodulation performance of high dynamic performance drives is to change the controller structure as the overmodulation region is approached. SFCR can be operated until roughly 90 % of the six-step voltage and a seamless transition to the DTC method [43, 190, 195] (in particular [43, 195]) enables the drive to perform satisfactorily until the six-step mode. The DTC method has been widely employed in high power traction drives which require performance in a wide operating range from zero voltage level to the six-step mode. Such drives employ field weakening above the drive base speed and fully utilize the inverter voltage by transitioning to the six-step operating mode and rapidly accelerate to very high speed levels. With an accurate motor model, the DTC method predicts the phase and magnitude of the motor EMF and precisely controls the stator flux to rapidly accelerate/decelerate the motor (utilizing all the available voltage) without unwanted overcurrent transients. Graceful transition to the six-step mode and back is easily achieved with DTC. Therefore, the high modulation region performance of DTC is superior to SFCR. Combining these two methods, a high performance variable structure control algorithm can be obtained. Seamless transition from SFCR to DTC and back can be easily achieved provided that the state variables of both controllers are precisely computed and updated. Since both controllers employ the same motor model (motor fundamental model), updating the inactive controller variables should not involve substantial computations. Therefore, this approach appears to be viable and the design and implementation of such a controller is an emerging research/development subject.

Additional issues involving SFCR or DTC controlled drives operating in the overmodulation range are the DC power source stability issues as well as the motor torque oscillations at/near six-step. Widening the overmodulation range of a drive implies increasing the loading of the DC power source. In particular, in soft DC bus applications (a diode rectifier with small capacitors forms a soft DC power supply), the DC bus can have negative impedance instability and increasing the voltage utilization may result in a DC bus overvoltage/undervoltage fault condition, rendering the drive unreliable. Therefore, in such applications voltage utilization must be intentionally limited. In certain applications the six-step operating mode may result in unacceptably large torque ripple (the dominant harmonic occurs at six-times the inverter output frequency). In such applications voltage utilization must also be limited to an acceptable value.

Most overmodulation studies assume an inverter model with fixed or relatively stiff DC voltage source. Detailed system level studies which involve the DC power source and load (motor) dynamics are required in order to design reliable inverter drives.

Since the soft switching resonant converter technology is rapidly developing and becoming an alternative to the conventional hard switching PWM-VSI drives, the modulation methods and modulator performance limits of such drives are gaining importance [45]. Since modulation methods involving such converters may employ fundamentally different approaches than PWM, and the modulator nonlinearities may be more significant than PWM-VSI drives,

the performance study of such drives is more involved and requires significant attention.

Finally, the question remains on whether a high performance current regulated drive with wide steady state and dynamic performance (from zero modulation index until the six-step mode) could be developed. With the steady state and dynamic performance requirements contradicting (as illustrated in the previous chapter), an intelligent method with superior performance must be developed. This issue remains to be one of the most challenging tasks regarding SFCR controlled PWM-VSI drives.

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