Output Voltage Control of A Four-Leg Inverter Based Three-Phase UPS by Means of Stationary Frame Resonant Filter Banks

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***Abstract*—A method for high performance output voltage control of a four-leg inverter (FLI) based three-phase UPS is proposed. Stationary frame resonant filter bank based output voltage control loop, which is complemented by capacitor current feedback based active damping loop, is employed. Utilizing the zero-state partitioning variable, a generalized form of scalar PWM for the FLI is developed and the minimum loss discontinuous PWM method is derived. The controller and modulator design and implementation details for the FLI-UPS are given. Linear and nonlinear loads for balanced and unbalanced load operating conditions are considered. The scalar control and PWM methods are proven by means of theory, simulations, and experiments.**

***Index Terms*—Four-leg, inverter, UPS, voltage regulation, unbalance, zero-sequence, harmonic, THD, crest factor, resonant filter, active damping, scalar PWM, zero-state partitioning, switching loss, efficiency.**

I. INTRODUCTION

The four-leg inverter (FLI) is utilized in three-phase four-wire power converter and UPS applications due to its superior performance characteristics such as relatively low DC bus voltage and switching loss, and capability to handle unbalanced load currents [1]. Shown in Fig.1, the four-leg Voltage Source Inverter (VSI) topology involves an additional leg compared to the conventional three-leg inverter such that the fourth leg provides a path for the zero-sequence currents for nonlinear and unbalanced loads. Since there is no DC bus mid-point connection to the load, and the load current unbalances are partially circulated in the inverter through the fourth leg, the DC bus capacitor size and the DC bus voltage oscillations can be made small [2]. Since it involves three independent load phases and four inverter legs (2 additional switches and 2^4=16 switch states), the FLI is more complex structure than the classical three-leg inverter. Both the control and PWM methods are complex for the FLI. As a result the FLI topology has found limited applications until recently.

Control of the FLI based three-phase UPS (FLI-UPS) may involve classical linear regulators (stationary/synchronous frame PID) [3], modern control methods such as deadbeat and predictive control. In the classical stationary/synchronous frame control methods, the three-phase variables are coordinate transformed to the control coordinates (αβ0 and/or dq0), the controller operates on the error and the manipulation signals are obtained. Then an inverse transformation is employed and the inverter applies the PWM signals. In the synchronous frame approach, the dq variables are controlled with linear PI regulators while the zero-sequence component is separately controlled with a different type controller [4]. As a result a complex controller structure becomes inevitable.

Similar to the control difficulties, the PWM pulse pattern determination process of the FLI is involved. The 3-dimensional space vector PWM (3D-SVPWM) approach involves a complex procedure (defining a region among 24, the sequence for 5 vectors, and converting vector duty cycles to switch duty cycles) that is time consuming and non-intuitive [2]. Although with proper algorithms the 3D-SVPWM can be utilized to generate high performance pulse patterns, due to its complexity the method is not favorable. The scalar PWM method which has been developed for the FLI is easier to implement, however it is not complete and general in mathematical sense [5]. Low switching loss PWM algorithms are not reported either.

In this paper, the FLI is considered for UPS applications. Simple and easy to implement control and PWM algorithms are developed and implemented. The UPS output voltages are controlled by employing stationary frame resonant filter banks [6], [7] accompanied with proportional control, capacitor current based active damping control [8], and command voltage feedforward. Scalar PWM is employed and with the zero-state partitioning function, the scalar PWM methods for FLI are unified under one umbrella [7]. A low switching loss discontinuous PWM algorithm which provides minimum switching losses (MLDPWM) under all operating conditions (including unbalanced operation) suitable for FLI-UPS systems is developed. The theoretical control and modulation method studies will be complemented with detailed computer simulations and laboratory experiments.

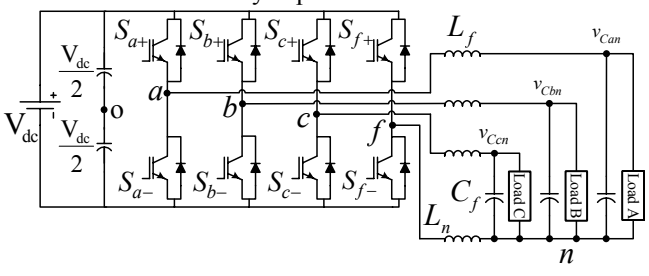

Fig. 1. Three-phase FLI-UPS system basic circuit configuration.

II. CONTROL OF FLI-UPS OUTPUT VOLTAGES

In this work, resonant filter controllers [7] will be employed for the purpose of regulating the output voltages of the FLI-UPS. In the FLI, due to the fourth leg, each phase voltage can be controlled independently (as if there were three independent inverters). For each phase of the UPS, one identical resonant filter bank controller is utilized and acts on the output voltage error of the associated UPS phase. Each resonant filter bank includes a fundamental frequency resonant filter controller and a set of harmonic frequency resonant filter controllers. In addition to the resonant filter bank, each phase involves a proportional controller acting on the output voltage error for the purpose of improving the output voltage dynamic response. Thus, the total controller is termed as P+Resonant controller and its structure is shown in Fig. 2.

In practice the application of the resonant filter controllers involves phase advancing (ϕ_m) that is required for the compensation of the measurement, computation, and PWM delays of the system. Furthermore, a damping term (ζ_m) is added to the resonant filter controller structure so that the fixed point DSP implementations have improved resolution and the wide frequency operating range applications have sufficiently wide control bandwidth. With the two additional parameters, the P+Resonant controller bank can be mathematically expressed in (1) where ($m\omega_e$) is the harmonic component to be controlled and M is the highest order to be controlled. K_{pv} represents the proportional controller gain and K_{im} represents the integral gain of associated resonant frequency. For $m=1$, the fundamental frequency controller provides voltage regulation. The resonant filter bank harmonic frequency controllers of the FLI-UPS are selected such that the current harmonics of the nonlinear load (as the worst case) are manipulated by the resonant filter bank and the output voltage is free of these harmonics. Thus, the resonant filter bank harmonic controllers are set to be the 3rd, 5th, etc. (Fig. 2).

$$G_C(s) = K_{pv} + \sum_{\substack{m=1 \\ m\ odd}}^{M} \frac{2K_{im}\cdot\zeta_m m\omega_e \left(s\cos(\phi_m) - m\omega_e \sin(\phi_m)\right)}{s^2 + 2\zeta_m m\omega_e s + \left(m\omega_e\right)^2} \quad (1)$$

The phase advance term can be calculated in (2), where τ_T is the total system delay (typically two PWM cycles). As (2) indicates, ϕ_m increases with the frequency. Additional phase advancing may be required as the resonant frequency of the LC filter of the UPS is approached. The damping term is given in (3), where $\Delta\omega$ represents the bandwidth of the resonant filter at the frequency to be controlled. In order to provide appropriate resolution for the resonant filter coefficients (in the fixed point processor applications) or to provide sufficient bandwidth, $\Delta\omega$ should be properly increased with the harmonic order [7].

$$\phi_m = \tau_T \cdot m\omega_e \quad (2)$$

$$\zeta_m = \Delta\omega/(2m\omega_e) \quad (3)$$

The resonant filter bank controller provides superior steady-state performance. However its dynamic response is limited and proportional gain alone can not improve the dynamic response of the controller. In order to obtain high dynamic performance, the output capacitor current feedback loop (with a K_{ad} gain) which provides active damping and improves the load disturbance rejection characteristic [8] is added to the resonant filter. Also voltage feedforward is added to the controller for the purpose of good command tracking. Thus the multi-loop controller structure in Fig. 3 is obtained. For each phase the controller operates on the output voltage error and the inverter phase voltage references v_{af}^*, v_{bf}^*, v_{cf}^* are obtained.

The stationary frame resonant filter bank control approach provides an easy design and implementation task with respect to the synchronous frame based controller or other complex control algorithms. There is no need for involved αβ0 and/or dq0 transformations, positive/negative/zero sequence decomposition and complex control structures. Thus, it is favored over other controller structures in this work.

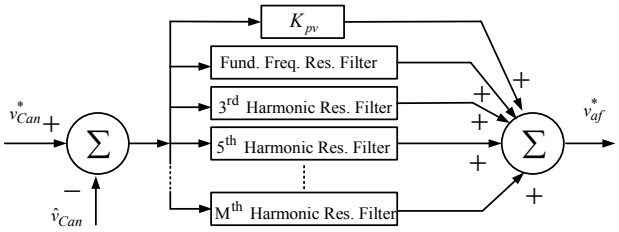

Fig. 2. Per phase P+Resonant filter bank controller structure.

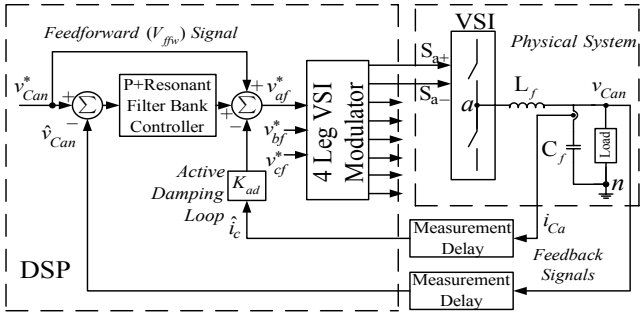

Fig. 3. The control system block diagram of the FLI-UPS system.

III. SCALAR PWM FOR FLI-UPS

In the FLI-UPS, the output voltage controller generates the voltage references v_{af}^*, v_{bf}^*, v_{cf}^* for the three phases, all with respect to "*f*," the center point of the fourth leg. It is required to define the fourth leg reference voltage v_{fo}^*. Then, all the inverter phase output terminal reference voltages (v_{ao}^{**}, v_{bo}^{**}, v_{co}^{**}) with respect to the virtual DC bus midpoint are defined in (4). The next step is to generate the PWM output signals as in the three-leg inverter case [9]. Comparing the modulation signals with the triangular carrier wave, the intersections define the switching instants. Figures 4 and 5 aid illustrating the pulse pattern generation method. Since the center point of the DC bus voltage is isolated and there is no path for current flow from the "*f*" point to the "o" point (see Fig. 1), there exists a degree of freedom in the choice of v_{fo}^* value. Thus, this degree of freedom can be utilized to the advantage of the inverter in terms of performance optimization. As it is added to the v_{af}^*, v_{bf}^*, v_{cf}^* to obtain the inverter leg modulation signals, this signal is called the offset or injection signal (Fig. 4). Output current ripple minimization, voltage linearity range maximization, switching loss minimization, etc. criteria can be utilized for optimization of the offset signal. To retain modulator voltage linearity, the reference voltages v_{ao}^{**}, v_{bo}^{**}, v_{co}^{**}, v_{fo}^* should be bounded with $\pm V_{dc}/2$. As a result, the potential difference between any two inverter output terminals is bounded by $\pm V_{dc}$.

$$v_{xo}^{**} = v_{xf}^* + v_{fo}^* \qquad x \in \{a,b,c\} \quad (4)$$

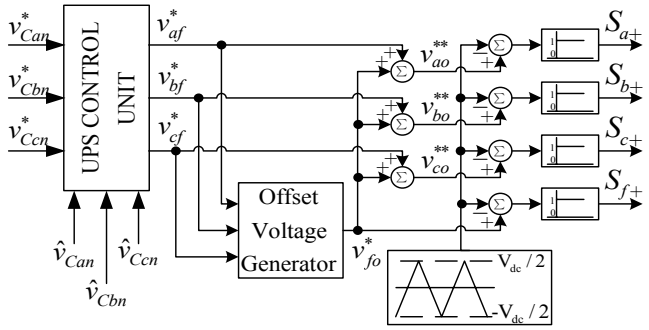

Fig. 4. Block diagram of the scalar modulation in the FLI.

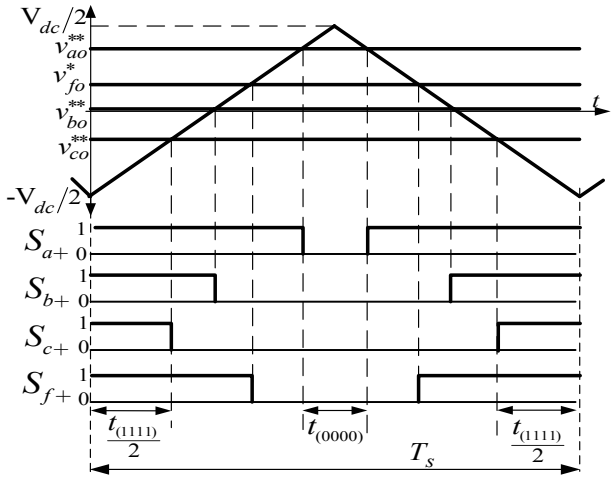

Fig. 5. Modulation and carrier signals and switching diagram of the FLI with $v_{fo}^*>0$ illustrating the influence on the width of the two zero-states.

There is a further constraint on v_{fo}^*, which will be discussed in the following. Of the three reference signals v_{af}^*, v_{bf}^*, v_{cf}^*, let's assume that the two extreme signals are v_{max}^* and v_{min}^* as defined in (5) and (6), respectively. The largest possible v_{fo}^* that retains the system linearity is a function of the absolute value of $v_{max}^* - v_{min}^*$. If $v_{max}^* - v_{min}^*$ is smaller than V_{dc}, there is a room for injecting a nonzero v_{fo}^*. The available range for the injection depends on the sign and magnitude of the v_{max}^* and v_{min}^*. The top and bottom limits of v_{fo}^* are given in (7) and (8). Depending on the top and bottom limit values of v_{fo}^*, a wide range may exist for the purpose of performance optimization.

$$v_{\max}^* = \max(v_{af}^*, v_{bf}^*, v_{cf}^*) \tag{5}$$

$$v_{\min}^* = \min(v_{af}^*, v_{bf}^*, v_{cf}^*) \tag{6}$$

$$v_{fo\_top}^* = \begin{cases} V_{dc}/2 & v_{\max}^* < 0 \\ V_{dc}/2 - v_{\max}^* & \text{elsewhere} \end{cases} \tag{7}$$

$$v_{fo\_bottom}^* = \begin{cases} -V_{dc}/2 & v_{\min}^* > 0 \\ -V_{dc}/2 - v_{\min}^* & \text{elsewhere} \end{cases} \tag{8}$$

If no offset signal is injected, $v_{fo}^*=0$ (the fourth leg is operated at 50 % duty cycle), then $v_{af}^*=v_{ao}^{**}$ etc. If v_{fo}^* is selected within the boundaries of (7) and (8) all the original modulation signals of Fig. 5 simultaneously shift upwards or downwards depending on the injection signal polarity. Thus, the intersection points of the carrier wave and thus the switching instants change. However, the modified signals v_{af}^{**}, v_{bf}^{**}, v_{cf}^{**} remain relatively at the same distance from each other. Thus, the widths of the rectangular line-to-line voltage pulses (and their average values) remain the same. Figure 5 shows that this vertical movement changes the duration ratio of the inverter zero-states 0000 and 1111. Defining the two zero-states as $V_{(0000)}$ and $V_{(1111)}$ and their durations as $t_{(0000)}$ and $t_{(1111)}$, respectively (Fig. 5), the zero-state partitioning function ξ can be formulated in (9). ξ has a range between 0 and 1. As v_{fo}^* increases, ξ linearly decreases. Involving (7) and (8), the relation between the ξ and v_{fo}^* can be written in (10), or as a function of v_{max}^* and v_{min}^* in (11) [7].

$$\xi = t_{(0000)} / (t_{(0000)} + t_{(1111)}) \tag{9}$$

$$v_{fo}^* = (1-\xi)(v_{fo\_top}^*) + \xi(v_{fo\_bottom}^*) \tag{10}$$

$$v_{fo}^* = \begin{cases} (1/2-\xi)V_{dc} - \xi v_{\min}^* & v_{\max}^* < 0 \\ (1/2-\xi)V_{dc} + (\xi-1)v_{\max}^* & v_{\min}^* > 0 \\ (1/2-\xi)V_{dc} + (\xi-1)v_{\max}^* - \xi v_{\min}^* & \text{elsewhere} \end{cases} \tag{11}$$

In order to illustrate the ξ and v_{fo}^* relations, operation at the modulation index (M_i) value of 0.64 is considered. M_i is defined as $M_i=0.5\pi V_{1m}/V_{dc}$, where V_{1m} is the fundamental component magnitude of the line-to-neutral inverter output voltage. As shown in Fig. 6, as ξ is incremented with 0.1 steps from 0 to 1, the offset signal v_{fo}^* decreases from $v_{fo\_top}^*$ to $v_{fo\_bottom}^*$. As M_i increases, the two boundaries approach each other and the range for v_{fo}^* expires. Between the two boundaries, the range of v_{fo}^* (or ξ) can be utilized to optimize a specific performance of the modulator. As a result, various PWM schemes arise. The ξ based modulation signal definition approach of (11) allows the unification of all the scalar PWM methods for FLI under one umbrella as previously established for the three-leg inverter [5]. The PWM methods discussed in the following are defined by the ξ function. Since SVPWM assumes equal zero-state partitioning, by definition $\xi_{SVPWM}=0.5$, which is the same as in the three-leg inverter case. The DPWM1 method, which is widely utilized in the three-leg inverter and specifically at high M_i due to its low output voltage ripple and reduced switching losses, involves locking the phase with the largest magnitude to the same side of the DC bus of the inverter. This method can be applied to FLI and for this inverter the ξ of DPWM1 is given in (12). Although the DPWM1 method and in a more generalized form GPDPWM provide switching loss reduction within a specific power factor range, they are inadequate for the FLI under load unbalance. For this purpose, the following new method is proposed for the UPS applications. In the Minimum Loss DPWM (MLDPWM) method, the offset signal is determined by considering both the largest phase magnitude voltages and the currents associated with these phases. Of v_{max}^* and v_{min}^*, the one that carries larger current is selected. This leg is clamped to the closer DC rail side while all other legs are shifted by the same amount in the same direction. For MLDPWM, ξ is given in (13), where I_{vmax} and I_{vmin} are the phase current magnitudes of v_{max}^* and v_{min}^*, respectively. Similar to other DPWM methods, MLDPWM exhibits low PWM ripple at high M_i and is suitable for UPS applications.

$$\xi_{DPWM1} = \begin{cases} 0 & |v_{fo\_top}^*| > |v_{fo\_bottom}^*| \\ 1 & |v_{fo\_top}^*| < |v_{fo\_bottom}^*| \end{cases} \tag{12}$$

$$\xi_{MLDPWM} = \begin{cases} 0 & |I_{v\max}| > |I_{v\min}| \\ 1 & |I_{v\max}| < |I_{v\min}| \end{cases} \tag{13}$$

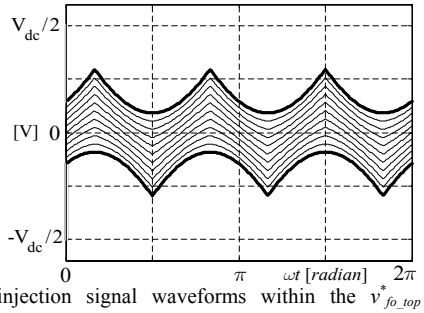

Fig. 6. The injection signal waveforms within the $v^*_{fo\_top}$ and $v^*_{fo\_bottom}$ boundaries as a function of ξ for M_i=0.64 (ξ incremented from 0 to 1 by 0.1).

The practical implementation of the discussed scalar PWM methods involves simple comparisons and computations. ξ is only utilized to formulate the modulation methods. However, the implementation does not involve calculation of ξ. Instead, v_{af}^*, v_{bf}^*, v_{cf}^* and if necessary the inverter currents are evaluated by simple comparisons. Based on the results, the modulation signals are obtained by simple computations. For example, for SVPWM, $v_{fo}^* = -0.5\,(v^*_{max} + v^*_{min})$, and then employing (4) the final modulation signals are obtained.

IV. Computer Simulations

In this section, the performances of the proposed control and PWM methods for the FLI-UPS are investigated by means of computer simulations using Ansoft-Simplorer where the inverter is fully modeled and the control system is implemented in discrete time. A 5-kVA, 120-V_{rms}/phase, 50-Hz, FLI-UPS is considered. The filter parameters, DC bus voltage, and switching/sampling frequency are given in Table I. For the balanced load tests, resistive load (Y-connected, 8.4 Ω/phase) and nonlinear three-phase diode rectifier with RC load (24 Ω, 1.1 mF) are considered.

TABLE I. System Parameters

Inverter	DC bus voltage (V_{dc})	540 V
	Switching frequency (f_{sw})	20 kHz
	Sampling frequency (f_s)	20 kHz
Filter	Inductor (L_f)	1.5 mH
	Capacitor (C_f)	30 μF
	Fourth leg inductor (L_n)	500 μH

First the controller gains of the proposed control algorithm (Fig. 3) are sequentially tuned based on trial and error method. This procedure is done at steady-state for the nonlinear rated-load (as the worst case). In the tuning procedure, the UPS output voltage quality measures, the output voltage regulation (VR), output voltage total harmonic distortion (THD_v), and load current crest factor (CF) are observed. Throughout, SVPWM is utilized. Since each controller is decoupled from the rest, the tuning procedure is sequentially conducted starting from the fundamental frequency and going up (3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}). The phase delay compensation given in (2) is taken $2m\omega_e T_s$ up to 7^{th} and $3m\omega_e T_s$ for the rest. The filter damping given in (3) is $1/(100\pi \cdot m)$ up to the 9^{th} harmonic and $1/(100\pi)$ for the rest. In the simulation, following the resonant filter controller gain tuning, the active damping and the proportional controller gains are set. Via this approach the degree of improvement each controller provides can be seen clearly [7]. Following the gain optimization stage, the steady-state linear/nonlinear balanced/unbalanced load tests are conducted.

Figure 7 shows the FLI-UPS performance under nonlinear, balanced, rated-load. With the closed-loop controller being active, VR, THD_V, and CF are 0.1%, 1.58%, and 2.45, respectively, compared to those of open-loop with 4.8%, 12.2%, and 1.6, respectively. The fundamental frequency controller regulates the output voltage with high accuracy and the harmonic controllers lower the UPS output impedance significantly such that THD_V is quite low. With the UPS acting as an ideal voltage source, the nonlinear load current crest factor becomes large compared to the open-loop controlled case.

The dynamic performance of the UPS is tested under balanced resistive rated-load. The load is turned on at the peak of the UPS phase output voltage and a sag condition is generated. The voltage dip, settling time, and the lost volt-seconds are measured. Both open-loop and closed-loop tests are conducted and those of the latter are shown in Fig. 8. The closed-loop controlled FLI-UPS output voltage dip is 67 V, the settling time is 0.55 ms and the lost volt-seconds are 19 mVs, compared to those of open-loop, which are 85 V, 1.2 ms, and 55 mVs, respectively. The active damping loop improves the dynamic response significantly as the figure shows. The total delay time is approximately $2T_s$ which is the total system delay time.

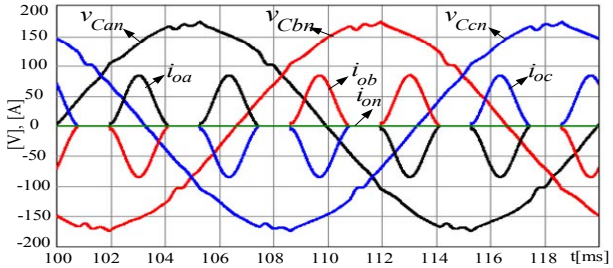

Fig. 7. Three-phase output voltages and load currents (scale: 2.5x) for closed-loop operation under balanced, nonlinear, rated-load.

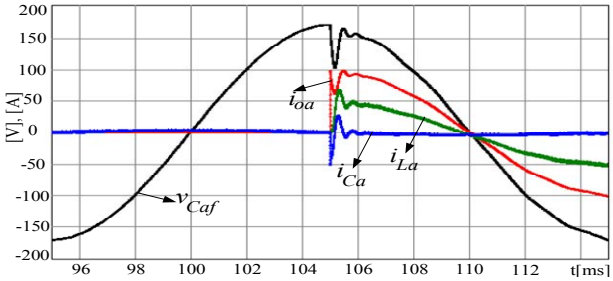

Fig. 8. Output phase voltage, load current (scale:x5), inductor current (scale:x2.5), and capacitor current (scale:x2.5) waveforms of the closed-loop controlled UPS during loading transient.

For balanced, resistive rated-load, closed-loop, steady-state operation, the inverter and load current, output voltage and modulation/switch logic signal waveforms are given in Fig. 9 for SVPWM and MLDPWM (same as DPWM1). Both PWM methods operate at 20 kHz. As in the three-leg inverter, smaller PWM current ripple favors SVPWM and lower switching count (better than 33% less switching losses) favors MLDPWM. SVPWM characteristics are independent of the load. Although MLDPWM and DPWM1 exhibit the same performance for balanced linear load, their performances under nonlinear and/or unbalanced load differ. For linear resistive line-to-neutral unbalanced rated-load, MLDPWM and DPWM1 method waveforms are shown in Fig. 10. For MLDPWM switchings of the loaded phase cease for longer duration than 120°. Thus, switching losses decrease compared to DPWM1 (13 % less) [7]. In this region, the loaded phase PWM current ripple of

MLDPWM is slightly higher than DPWM1. As shown in Fig. 11, the line-to-neutral unbalanced load current flows through the loaded phase and the fourth leg, while the unloaded phases carry small amount of current. As a result, MLDPWM respects the load current information (similar to GDPWM of 3-leg inverter [9]) in addition to the reference voltage magnitude information such that the switches of the phase with the largest current are selected to be locked to the DC rail for longer time intervals than the DPWM1 case yielding lower switching losses.

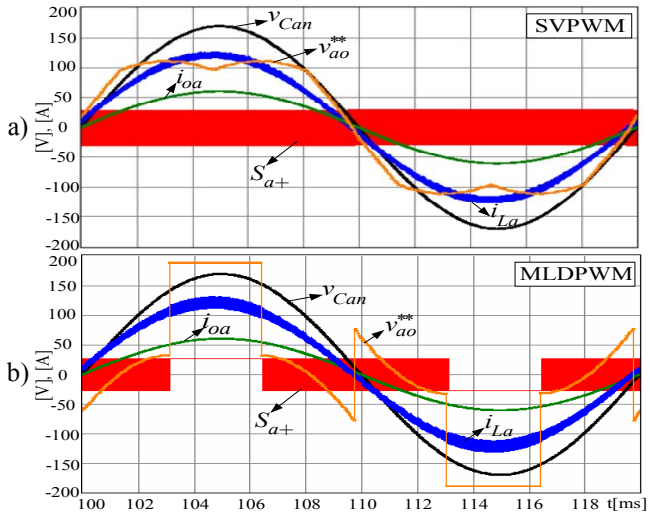

Fig. 9. Output voltage, modulation and switch logic signals, load current (scale: x3), and inductor current (scale: x6) under linear balanced load.

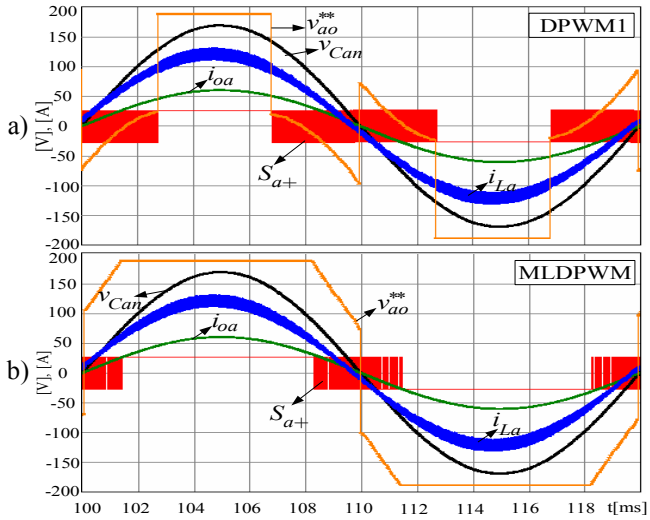

Fig. 10. Output voltage, modulation/switch logic signals, load current (scale: x3), and inductor current (scale: x6), under linear line-neutral unbalanced load.

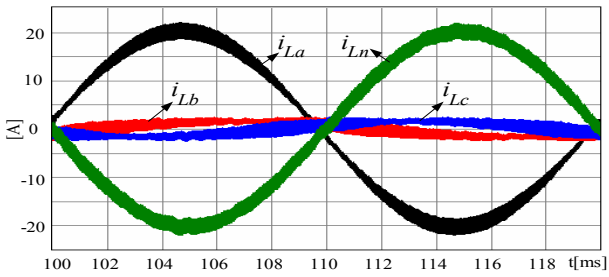

Fig. 11. Steady-state inverter output currents of MLDPWM under resistive line-to-neutral unbalanced load.

V. Experimental Results

In this section, the performances of the proposed control and PWM methods for the FLI-UPS are investigated by laboratory experiments. An FLI-UPS with the same ratings as the simulated system has been built and tested in the laboratory. The UPS is controlled by a DSP (TMS320F2812). The experimental system parameters are the same as those in Table I. The same controller design, tuning and UPS performance test steps as those of the simulations are followed in the laboratory.

Figure 12 shows the closed-loop controlled FLI-UPS performance under nonlinear, balanced rated-load. For this case, FLI-UPS produces output voltages with THD_v of 1.8% and VR of 0.33% with load current CF of 2.6. Thus, experimental results verify the computer simulations, and as predicted in the computer simulations, the experimental performance of the UPS is superior to the commercial state-of-the-art. Detailed steady-state performance results for various (particularly unbalanced) loading conditions are given in Table II. According to the table, for extreme load current imbalances, the output voltages remain well balanced (for all load conditions V_{neg}<1% and V_{zero}<1%) and THD_v remains low (for linear load THD_v<1%, for nonlinear load THD_v<3%). For all cases VR is less than 1% illustrating the superior performance of the proposed control method.

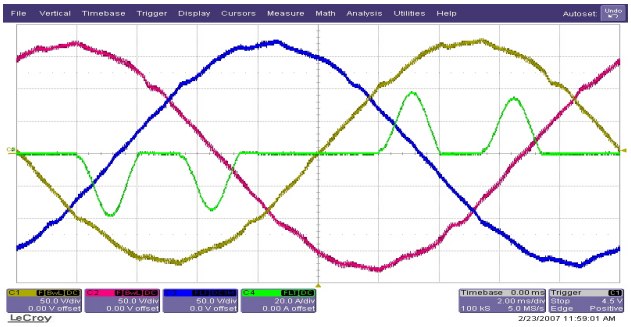

Fig. 12. Output voltages and one phase load current for closed-loop operation under balanced nonlinear rated-load (Scales: 50V/div, 20A/div, 2ms/div).

TABLE II. The Steady-State Performance at Various Load Conditions

		Linear load		Nonlinear load	
		Open-loop	*Closed-loop*	*Open-loop*	*Closed-loop*
Balanced load	CF	1.43	1.44	1.65	2.60
	VR (%)	14.95	0.33~0.45	13.63	0.16~0.33
	THD_V (%)	4.6	0.7	10.6	1.8
	V_{neg} (%)	0.2	0.3	0.2	0.3
	V_{zero} (%)	0.2	0.4	0.3	0.5
	I_{neg} (%)	0.3	0.6	1.1	4.5
	I_{zero} (%)	0.2	0.4	0.3	0.2
Line-neutral unbalanced load	CF	1.54	1.43	2.21	3.43
	VR (%)	12.6~30.8	0.41~0.83	7.43~19.0	0.17~0.57
	THD_V (%)	6.3~12.0	0.7~0.9	7.4~16.2	0.9~2.6
	V_{neg} (%)	5.9	0.3	3.8	0.3
	V_{zero} (%)	24.0	0.8	15.3	0.6
	I_{neg} (%)	100	100	100	100
	I_{zero} (%)	100	100	100	100
Line-line unbalanced load	CF	1.48	1.43	2.30	3.38
	VR (%)	1.4~14.3	0.4~0.7	0.25~12.3	0.08~0.25
	THD_V (%)	3.6~6.9	0.7~0.9	3.6~11.5	0.8~1.9
	V_{neg} (%)	11.0	0.2	7.4	0.3
	V_{zero} (%)	4.9	0.4	4.5	0.4
	I_{neg} (%)	100	100	100	100
	I_{zero} (%)	0.2	0.2	0.2	0.1

The dynamic performance of the UPS is tested in the laboratory under the same resistive loading condition as the simulations. The voltage dip, settling time, and the lost volt-seconds are measured and listed in Table III. Both open-loop and closed-loop tests are conducted. The voltage dip is mainly improved by the active damping loop while all the controllers contribute to the improvement in the settling time practically equally. With all the controllers being active (the last line on Table III), the best dynamic response is obtained. The loading transient waveforms for this case are shown in Fig. 13. The waveforms are in high correlation with the simulation results indicating the satisfactory performance of the control system.

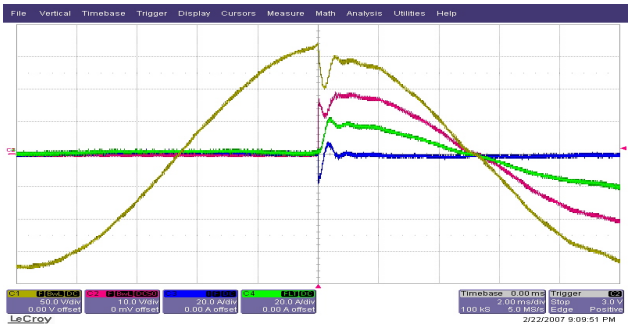

Fig. 13. Output voltage (yellow), load current (red, x2), inductor current (green), capacitor current (blue) transients (Scales: 50V/div, 20A/div, 2ms/div).

TABLE III. PERFORMANCE CHARACTERISTICS DURING THE DYNAMIC LOADING

Controller	Δt (ms)	ΔV (V)	∫vdt (V·ms)
Open-loop (only V_{ffw} active)	1.65	85	70.13
Fund. freq. res. filter added	1.58	90	71.20
Harmonics freq. res. filters added	1.05	90	47.25
Prop. cont. loop (K_{pv}) added	0.88	88	38.72
K_{ad} added and gains increased	0.63	68	21.50

As a final experiment, for balanced, resistive rated-load, closed-loop, steady-state operation, the inverter and load current, output voltage and modulation/switch logic signal waveforms are given in Fig. 14 for MLDPWM. The waveforms are in correlation with the computer simulation results of Fig.9. As shown by computer simulations, for nonlinear/unbalanced load, MLDPWM has superior performance compared to DPWM1 in terms of switching count (losses). For linear resistive line-to-neutral unbalanced rated-load, MLDPWM and DPWM1 method waveforms are shown in Fig. 15. For MLDPWM, switching of the loaded phase ceases longer than 120° while for DPWM1 it ceases for approximately 120° as expected. Also there is no significant difference between the PWM current ripple of the two cases. This shows that MLDPWM is superior to DPWM1 and GDPWM [9] in terms of switching losses.

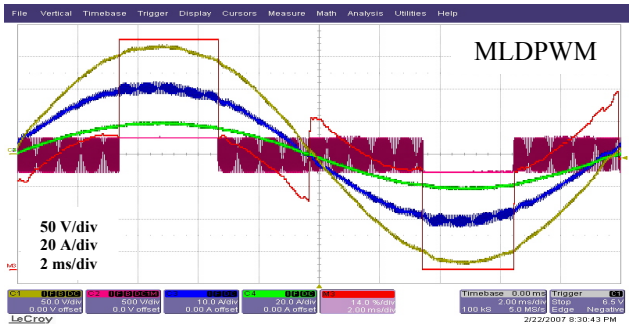

Fig. 14 Output voltage (yellow), modulation/switch logic signals, load current (green), and inductor current (blue, x2), under linear balanced load.

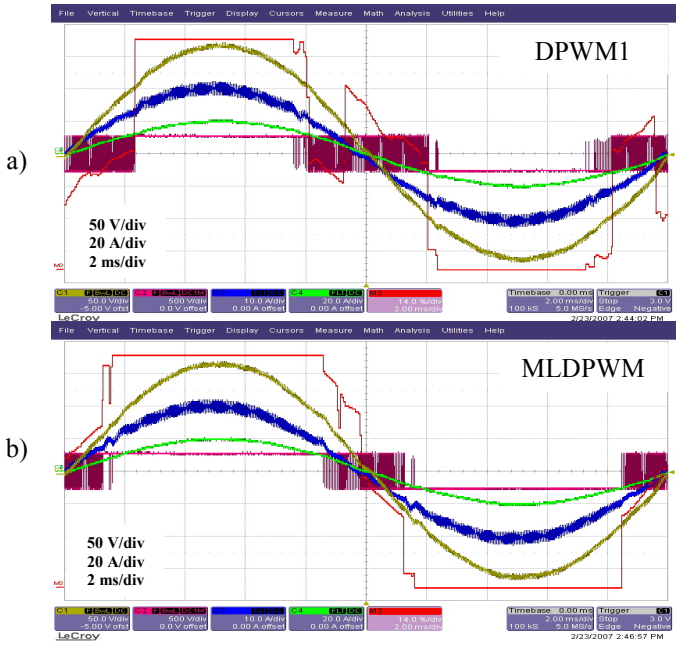

Fig. 15. Output voltage (yellow), modulation/switch logic signals, load current (green), inductor current (blue, x2), under linear line-neutral unbalanced load.

VI. CONCLUSION

Stationary frame resonant filter bank control method for output voltage control of an FLI-UPS is proposed. Utilizing the zero-state partitioning variable, a generalized form of scalar PWM is developed. MLDPWM which has equivalent performance to GDPWM for balanced load, and superior performance for line-to-neutral unbalanced load, is developed. The superior performances of both the control and PWM methods are proven by simulations and experiments.

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