EE-282 / 2010

DIGITAL ELECTRONICS

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Ceng 2010

✱ Digital Design Basics

(ex) 3 students are planning to go to a movie. Students are voting on going to a movie or not, and if the majority agrees to go to a movie, all of them'll go to that movie

Students = {G, M, S}

G	M	S	Decision
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

1: Yes 0: No

Decision:

$M \cap S = MS$ ← Mary & Sue

$M \cup S = M + S$ ← Mary OR Sue

Decision =

$$\bar{G}MS + G\bar{M}S + GM\bar{S} + GMS$$

$$GM(\bar{S}+S)$$

$$= \bar{G}MS + G\bar{M}S + GM$$

$$(G\bar{M} + GM)(S + GM)$$

$$G(\bar{M}+M)(S+GM)$$

$$G(S+GM)$$

$$= \bar{G}MS + GS + GM$$

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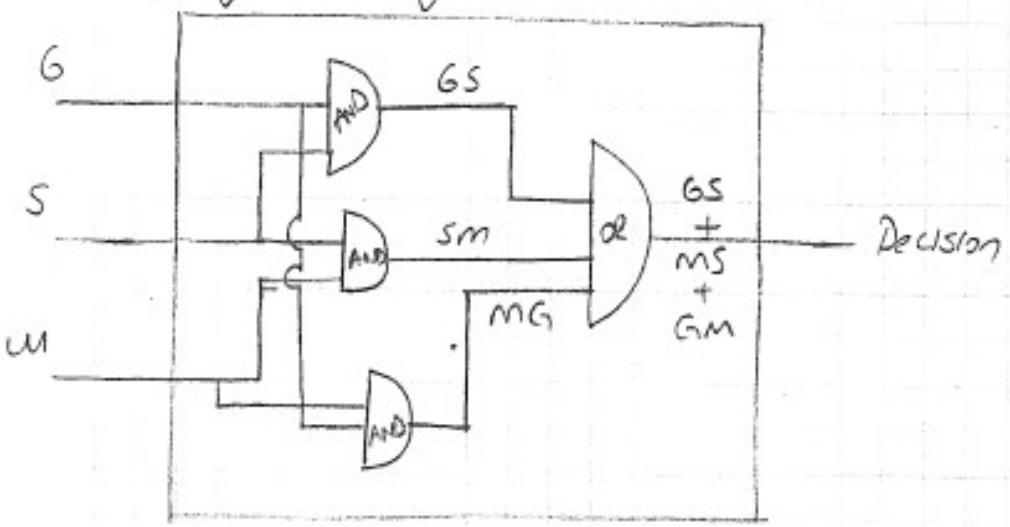
Decision : $\bar{G}MS + GS + GM$

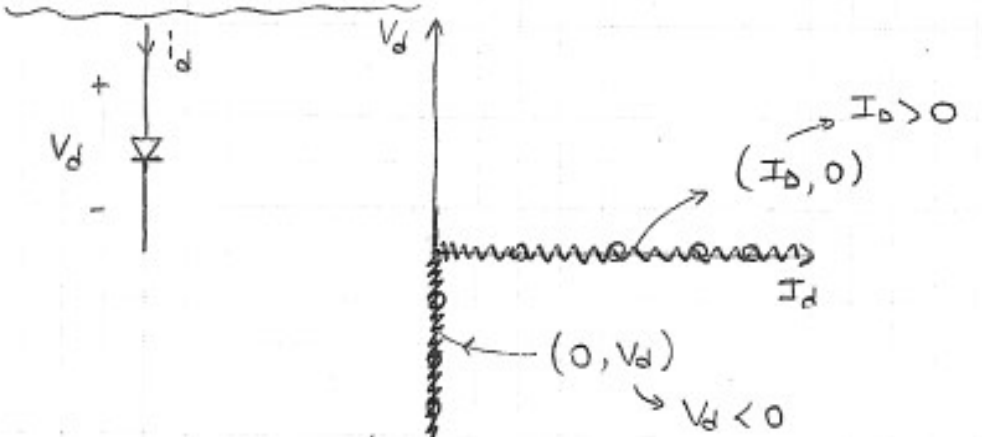
$GS + MS$

$= GS + MS + GM$

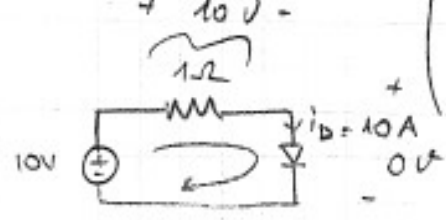
If any two says 'Yes', decision is 'Yes'.



IDEAL DIODES



(i-V characteristics of a memoryless component)



$-10 + 10 + 0 \stackrel{?}{=} 0$ ✓ (KVL)

✓ (KCL)

Ideal Diode:

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✓ Two States

↳ Conducting (Diode is ON) → $I_D > 0$

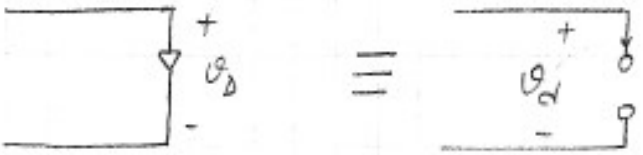
↳ Cut-off (Diode is OFF) → $I_D = 0$

ON State:

= Short Circuit

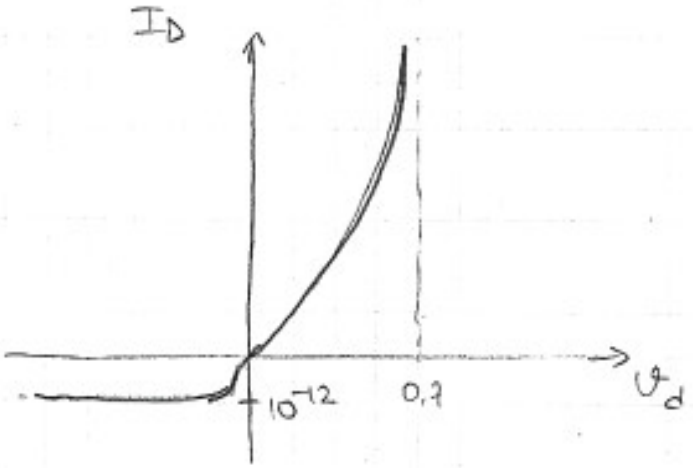
$v_D = 0$

OFF State:

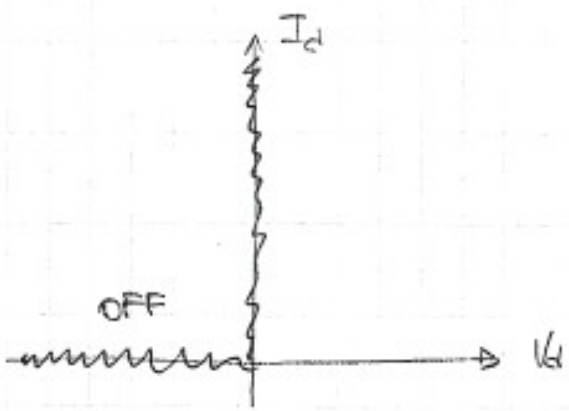


= Open Circuit

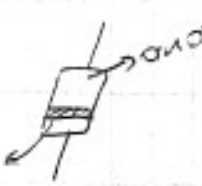
$i_D = 0$



Practical Diode



Ideal Diode



I-U characteristigi

origine göre simetrik olmadığı

için doğrusal değildir.

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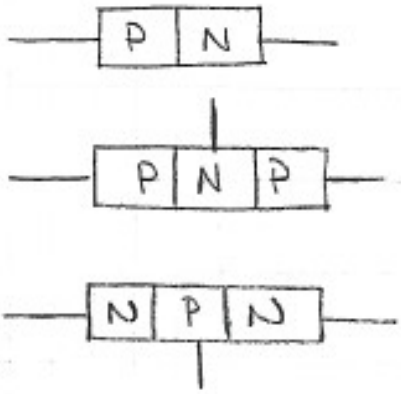


PN junction diode

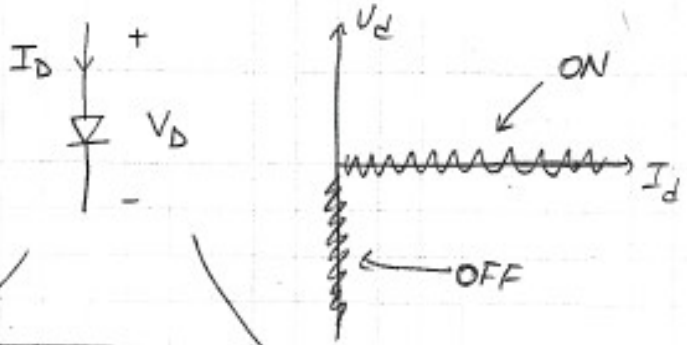
DIODE CIRCUITS

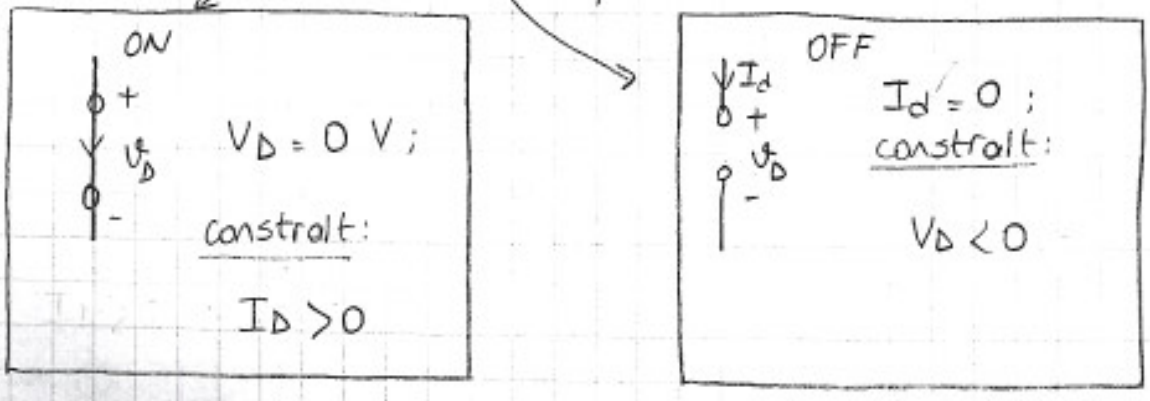
Methods of Analysis:

1. State Guessing (ON / OFF)
2. Graphical

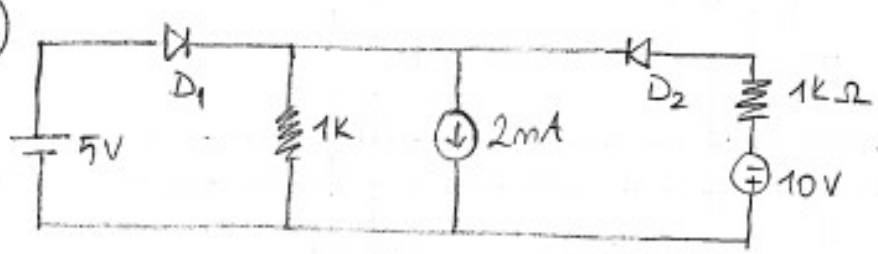
1. State Guessing

Ideal Diode Model:





(ex)



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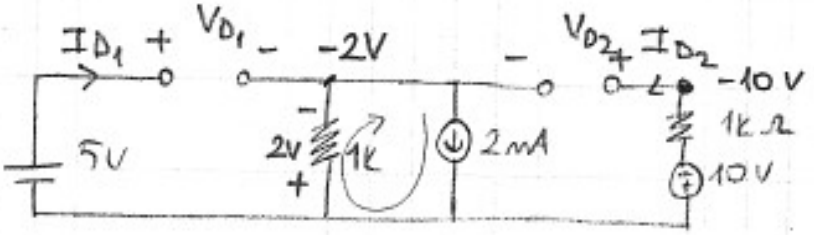
Note Guessing:

1. Make an assumption about diode states
2. Replace the model of diode according to the assumption in (1)
3. Solve resistive circuit formed at (2)
4. Check constraints / conditions for the assumption is satisfied or not.
5. If NOT satisfied → Repeat 1-5

   satisfied → Done

(1) D_1: OFF

D_2: OFF

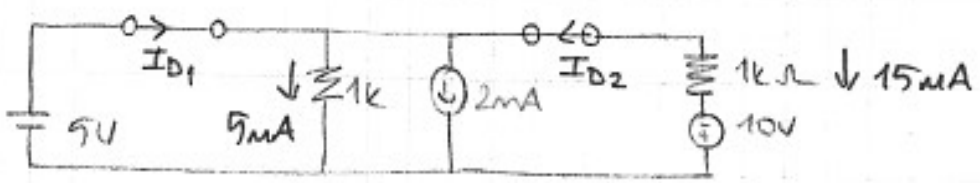


$-5 + V_{D_1} - 2V = 0$ $\quad -10 - (-2) = -8V$

$V_{D_1} = 7V$ ✗ $\quad V_{D_2} = -8V$ ✓

V_{D_1} is NOT satisfied. $\quad V_{D_2} < 0$

(2) D_1: ON



$I_{D_2} = -15\,mA$; $I_{D_1} = 22\,mA$

✗ ✓

$I_D > 0$ NOT satisfied

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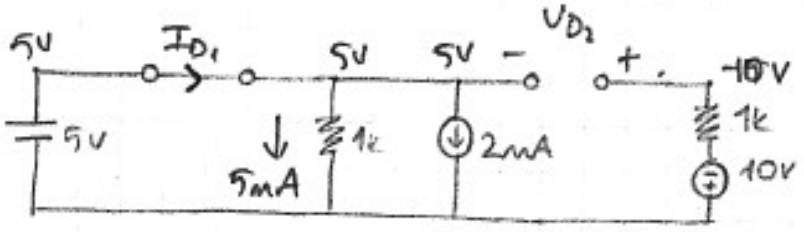
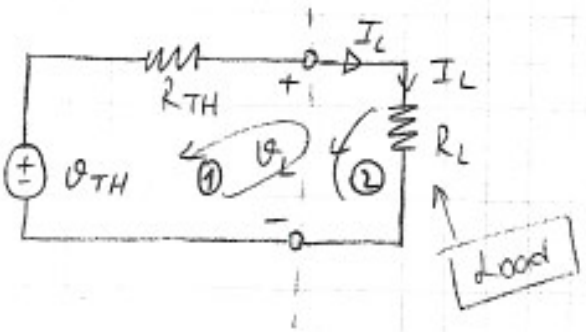
(3) D_1 : ON
D_2 : OFF



$I_{D_1} = 7mA$ ✓ ; $V_{D_2} = -10 - 5 = -15V$ ✓

Graphical Method for Analysis :



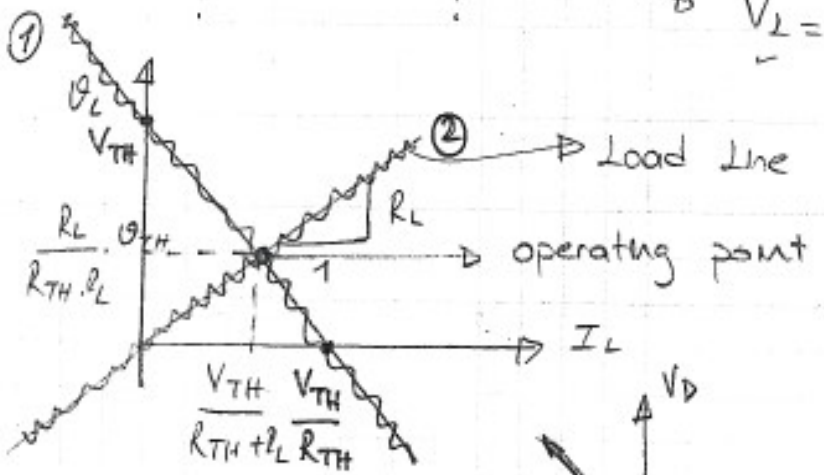
$$I_L = \frac{V_{TH}}{R_{TH} + R_L}$$

① $-V_L + R_{TH}.(-I_L) + V_{TH} = 0$ (KVL ①) $\rightarrow V_L = V_{TH} - R_{TH} I_L$

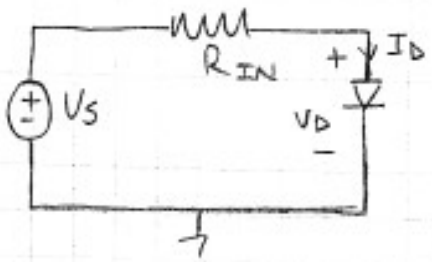
② $+V_L + R_L(-I_L) = 0$ (KVL ②)

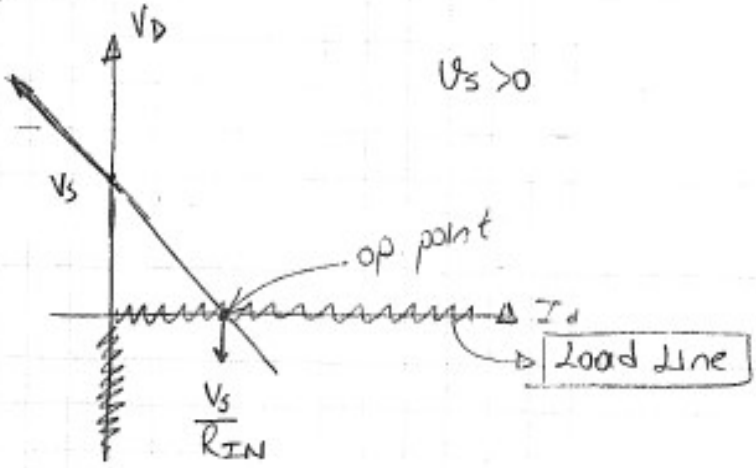
V_L ? I_L ?

$\rightarrow V_L = R_L . I_L$

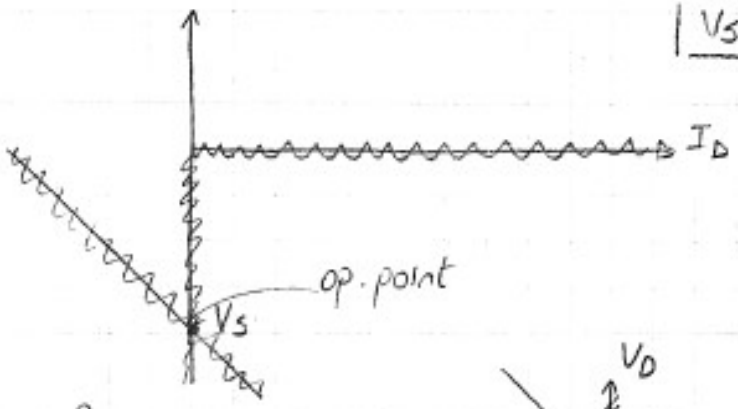


(ex)

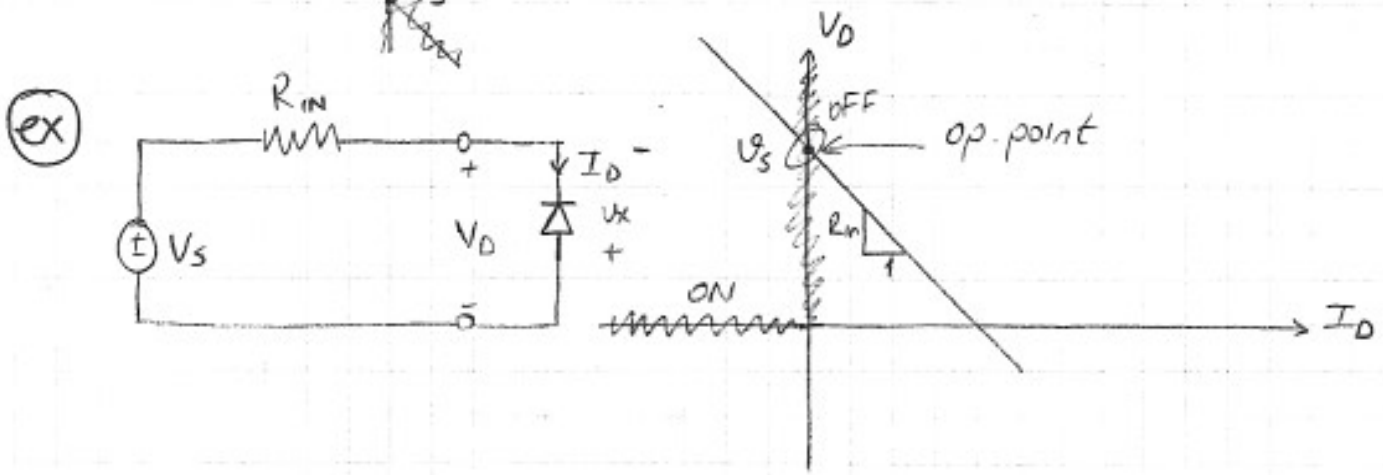




$V_S < 0$

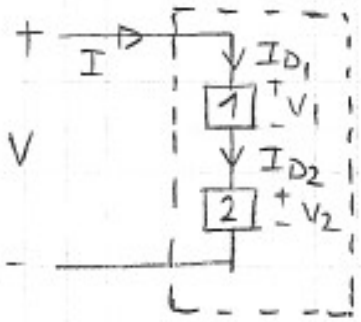


(ex)



Series & Parallel Combinations Of Circuit Components

Series:



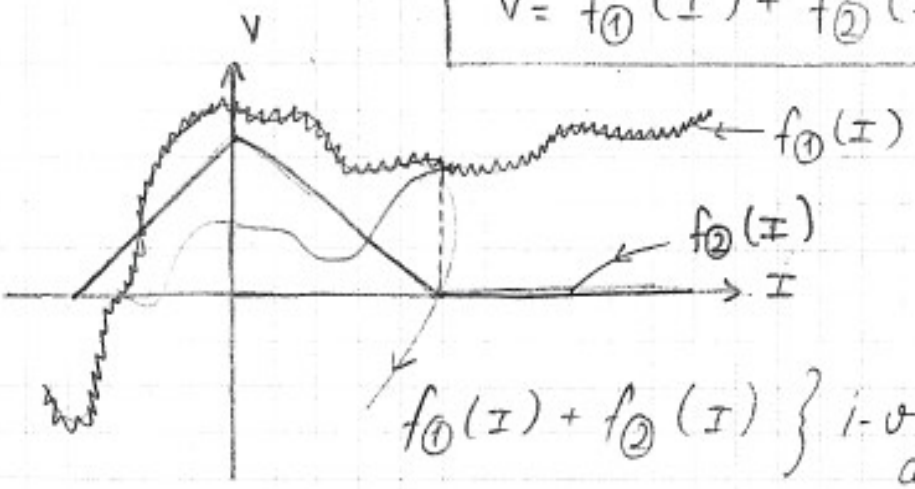
$I_1 = I_2 = I$ } Due to Series connection

$V = V_1 + V_2$

$\downarrow$

$V = f_{①}(I_1) + f_{②}(I_2)$

$\boxed{V = f_{①}(I) + f_{②}(I)}$



$f_{①}(I) + f_{②}(I)$ } i-v characteristic of combined component

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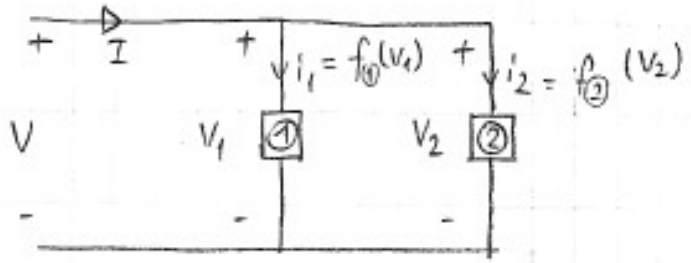
Parallel:

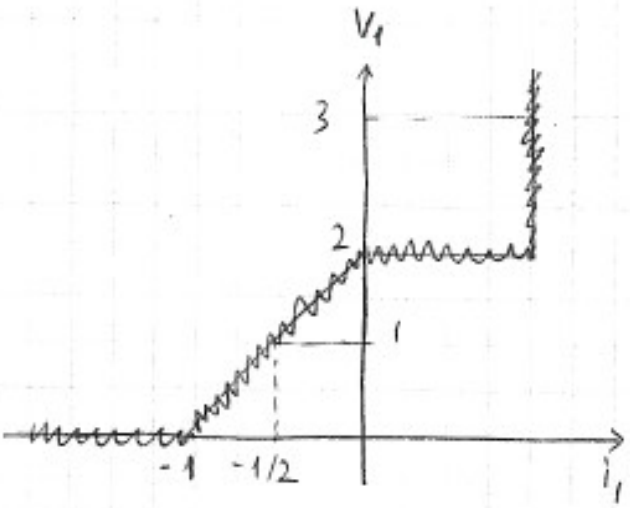


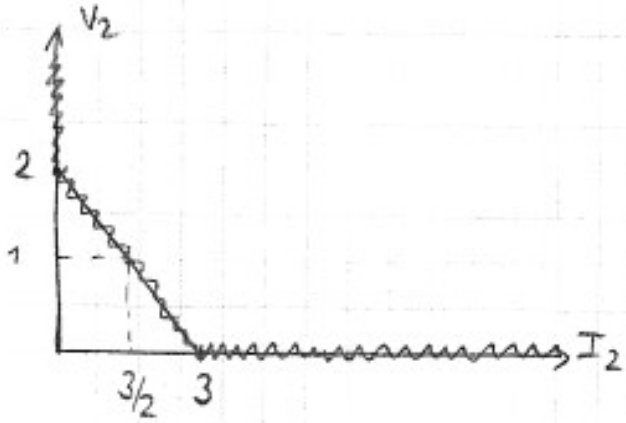
$V_1 = V_2 = V$

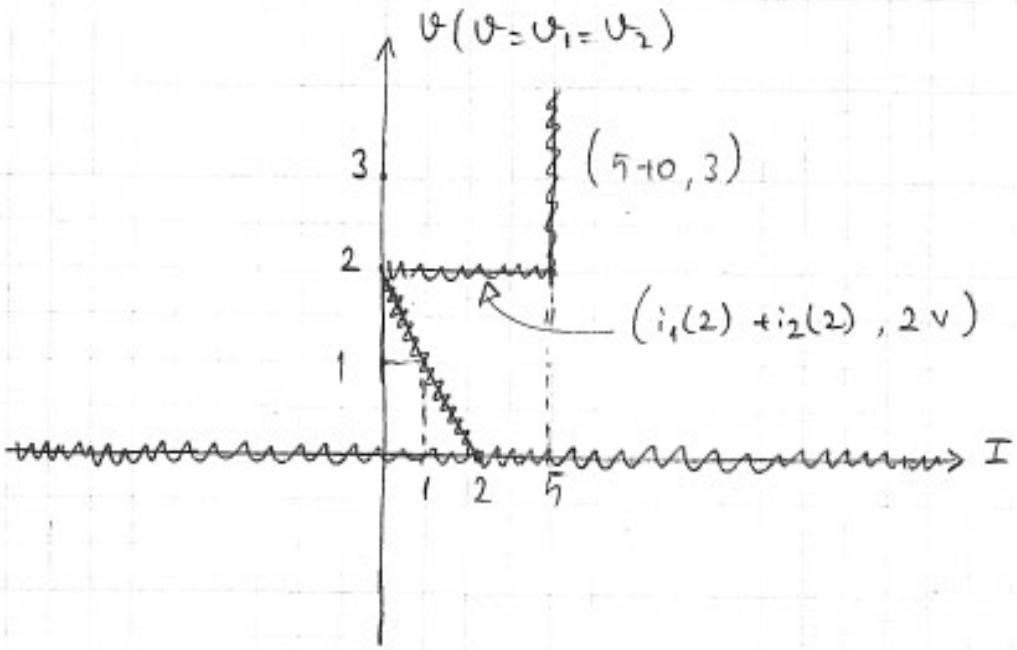
$I = i_1 + i_2$

$= f_①(V_1) + f_②(V_2)$

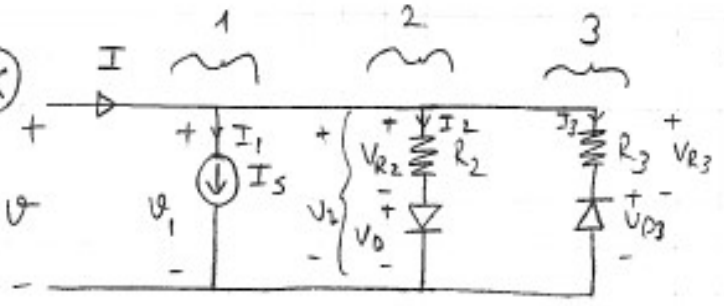
$$\boxed{I = f_①(V) + f_②(V)}$$





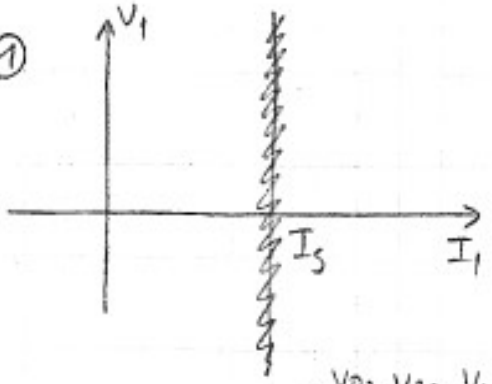


(ex)

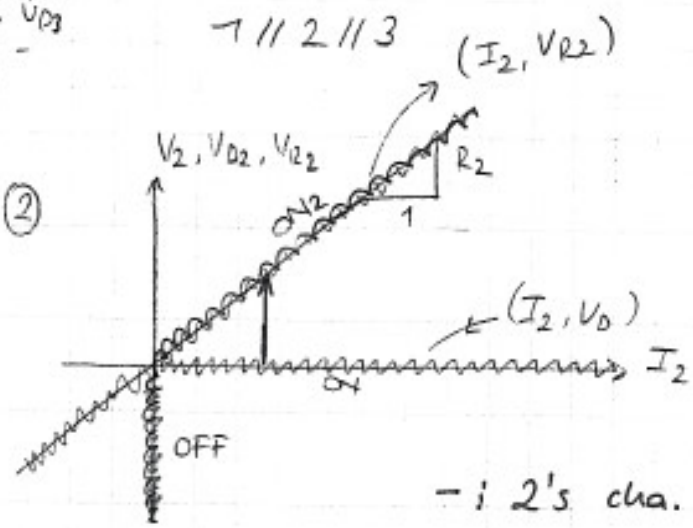


1 // 2 // 3

①

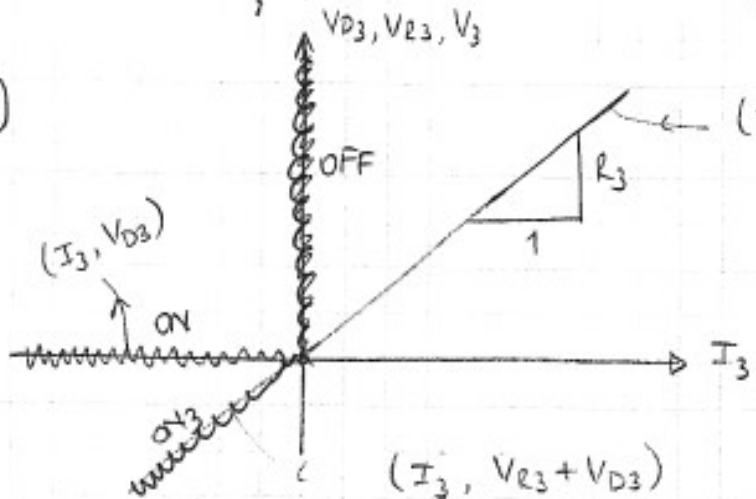


②

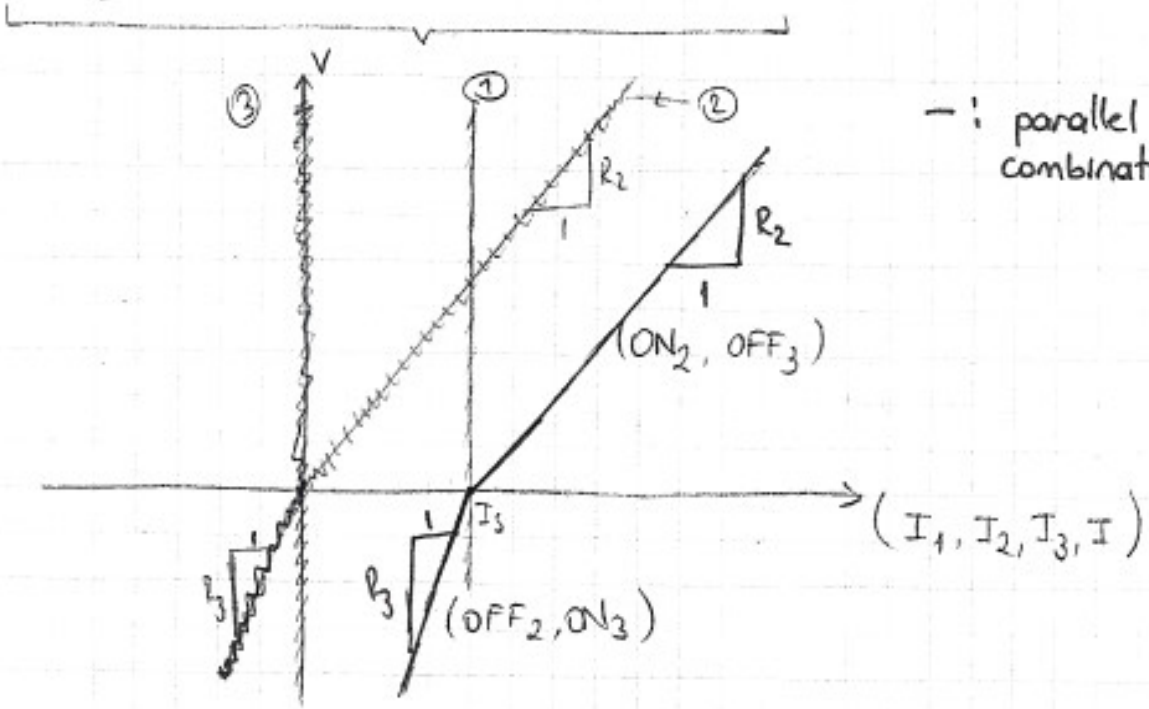


- : 2's cha.

③



- : 3'rds cha.



- : parallel combination

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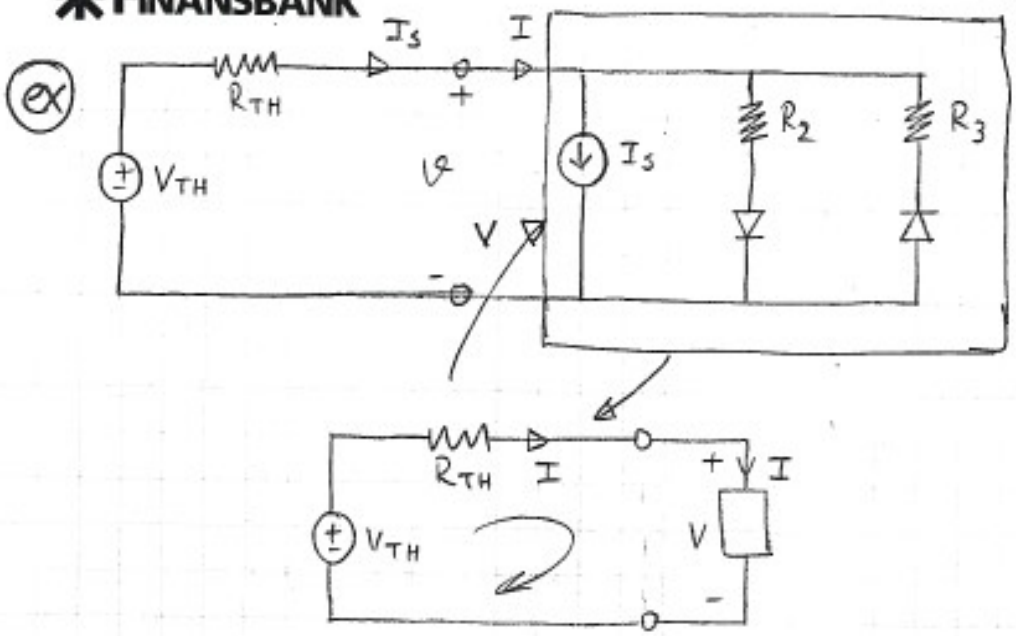
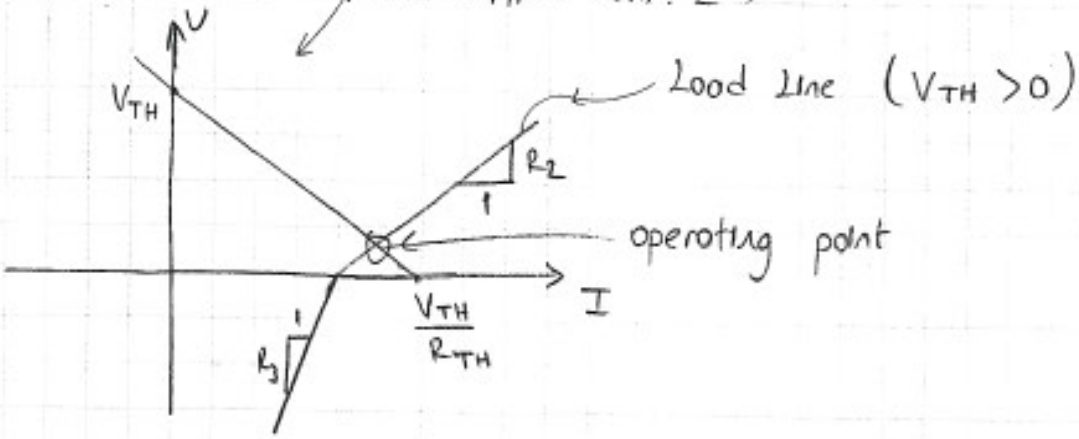
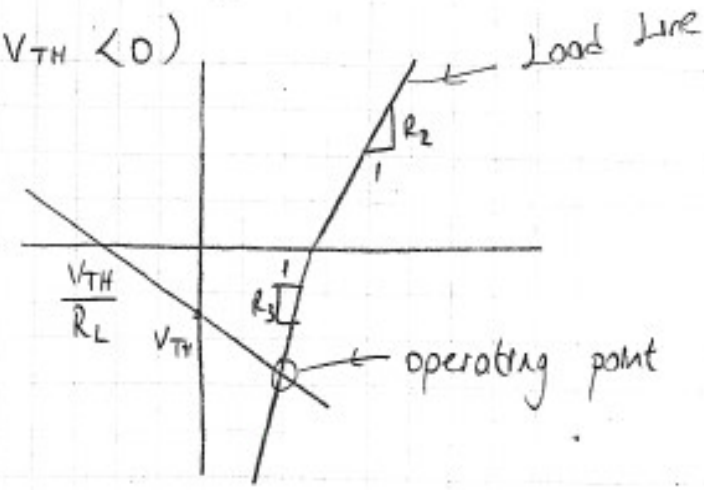


$$-V_{TH} + R_{TH}.I + V = 0$$

$$(v = V_{TH} - R_{TH}.I)$$



($V_{TH} < 0$)



3/03/2010

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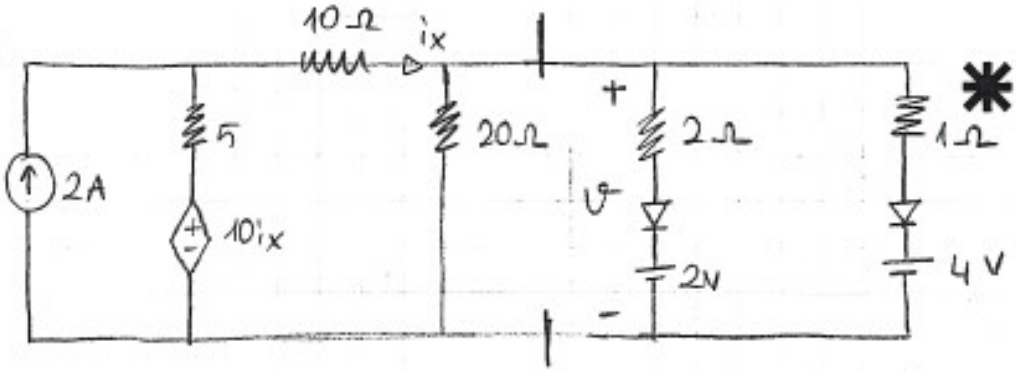
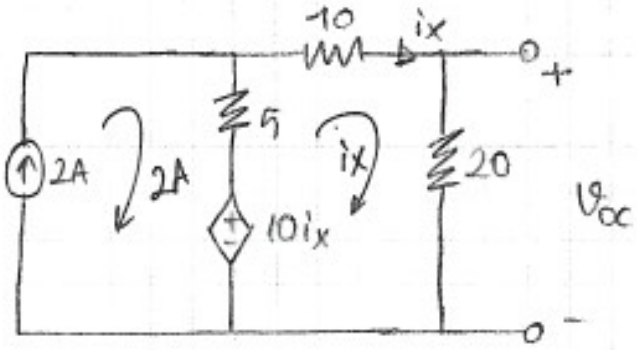
(ex)



Find v. → State Guessing
→ Graphical Method

Let's find Thev. eq of left hand side of "v" branch.



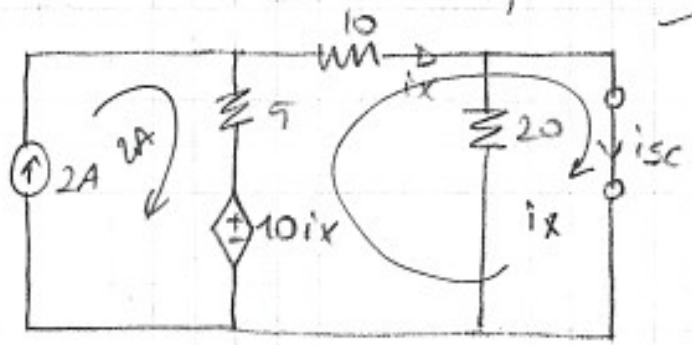
OC voltage

$$-10i_x + 5(i_x - 2) + 10i_x + 20i_x = 0$$

$$25 i_x = 10 \qquad i_x = \frac{2}{5} = 0.4\ A$$

$$v_{oc} = 20 i_x = 20 \cdot \frac{2}{5} = 8\ V$$

SC CURRENT



$$R_{TH} = \frac{V_T}{I_{sc}} = 4\Omega$$

$$-10i_x + 5(i_x - 2) + 10i_x = 0$$

$$i_x = 2\ A \qquad i_x = i_{sc} = 2A.$$

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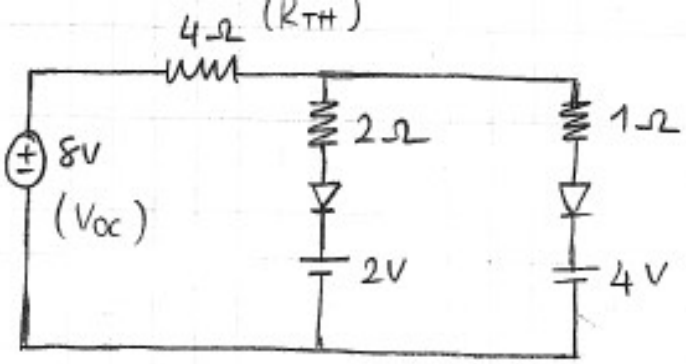
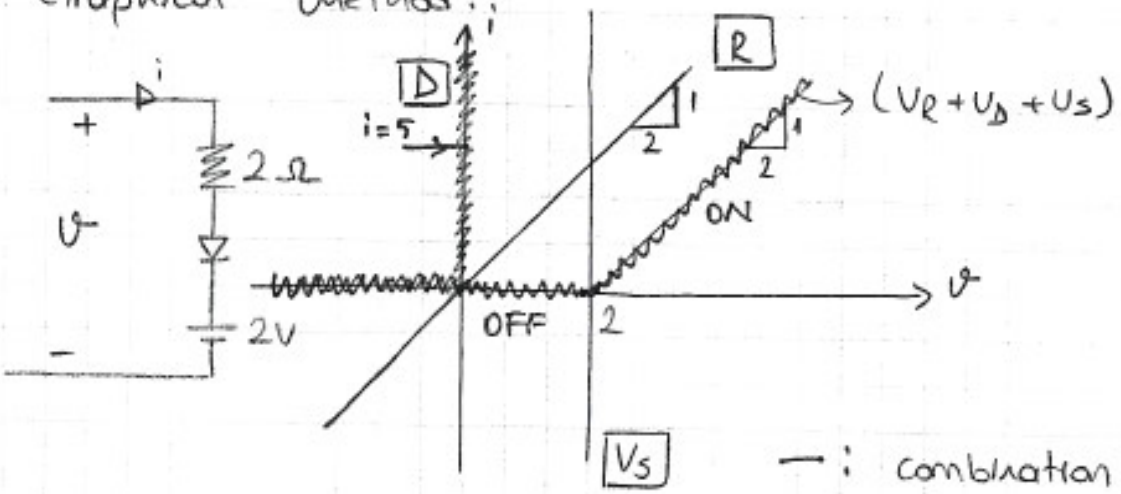
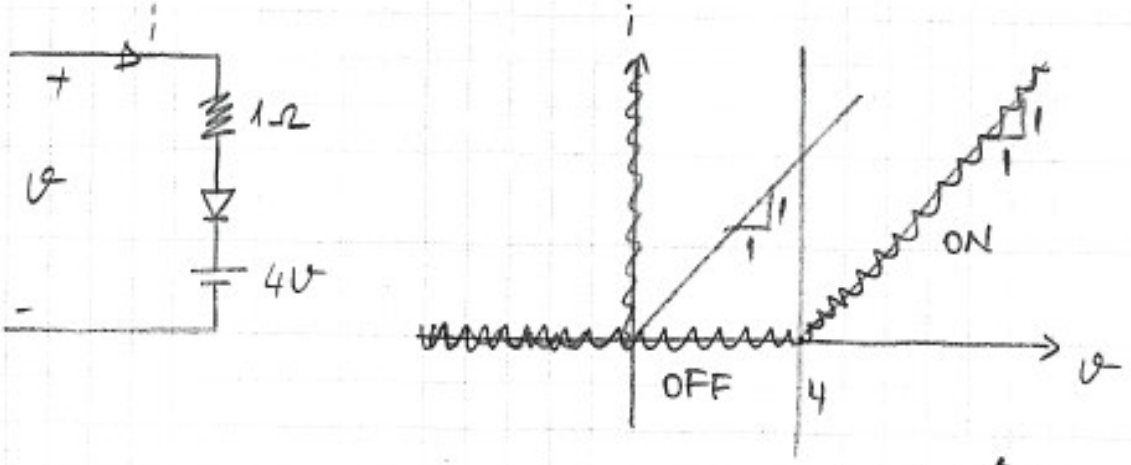


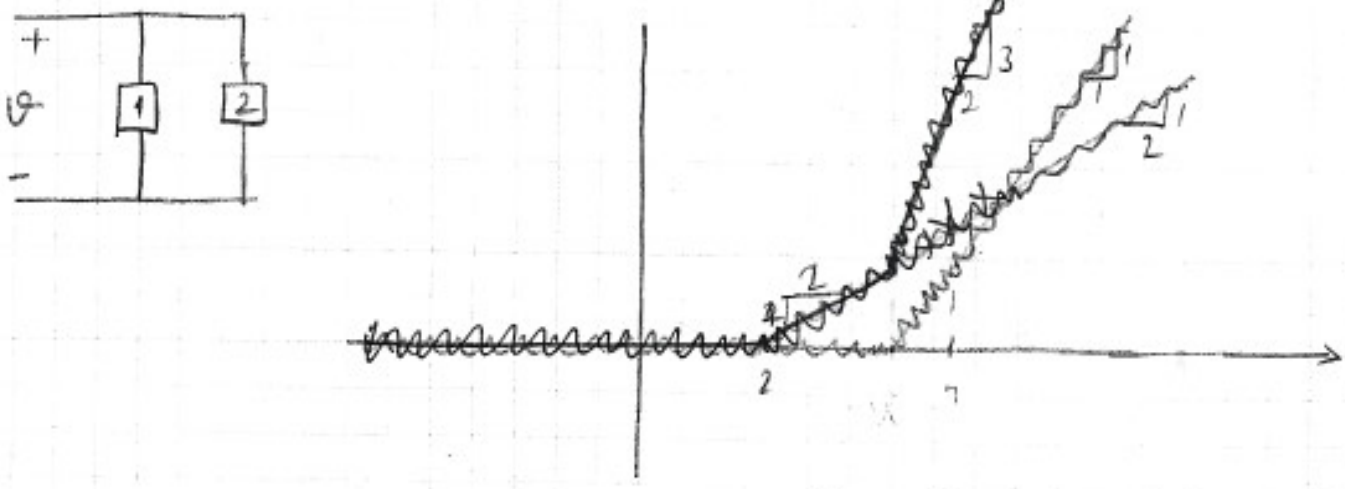
Graphical Method:



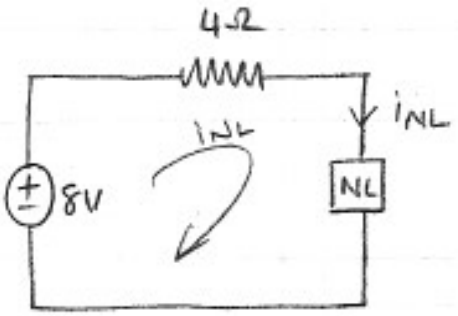
—: combination of three components

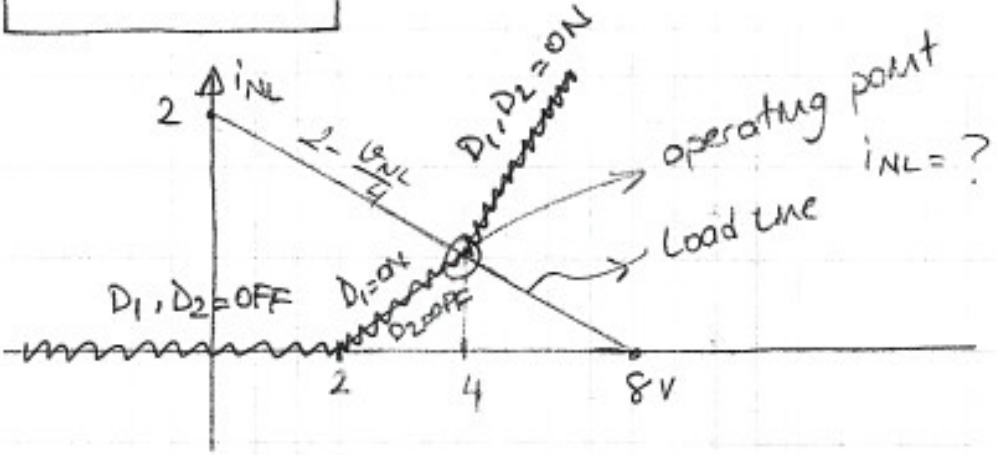
↙ Diode does not allow a negative current.





—: combination 1-2 ↙



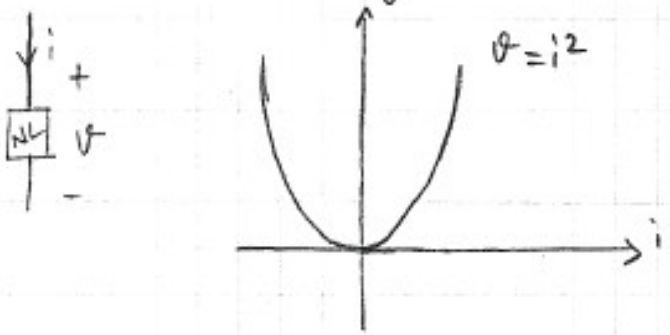


$$-8 + 4 \cdot i_{NL} + v_{NL} = 0$$

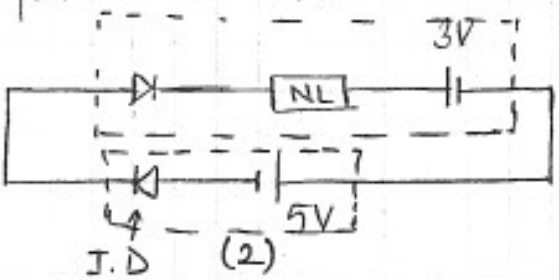
$$i_{NL} = 2 - \frac{v_{NL}}{4}$$ ← KVL constraint

5.03.2010

(ex)



Then find (1)



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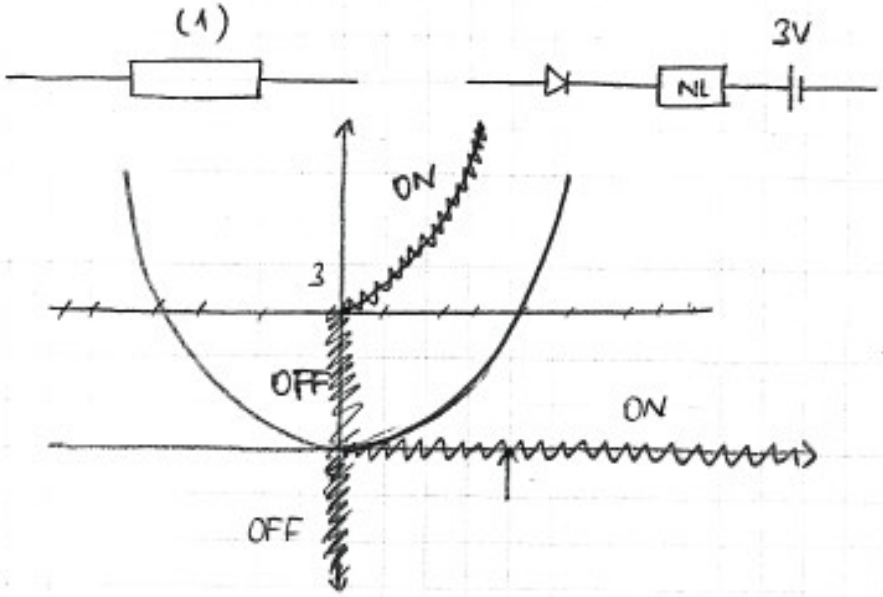
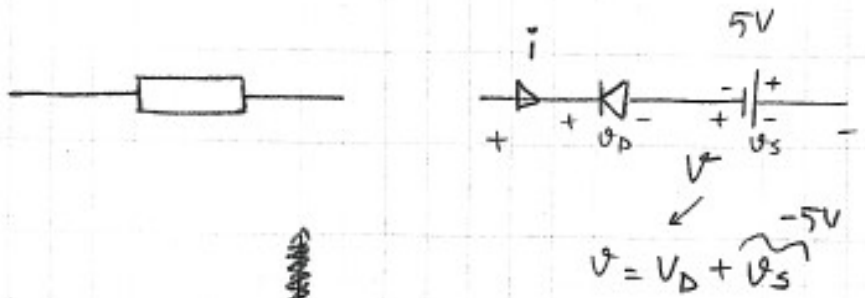
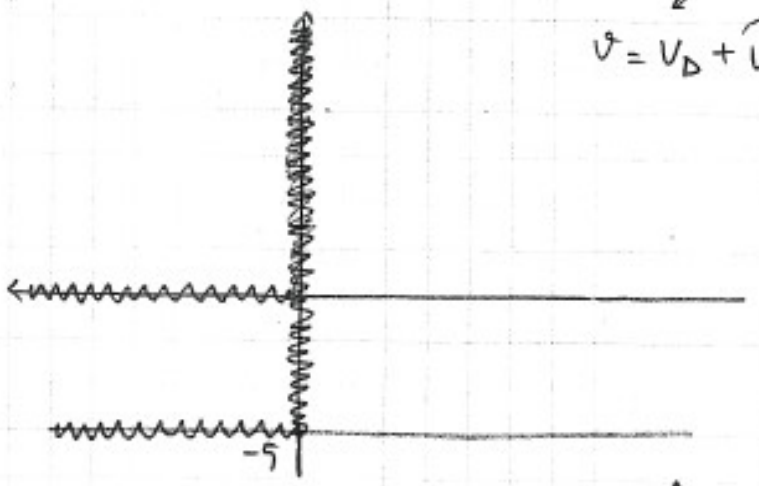
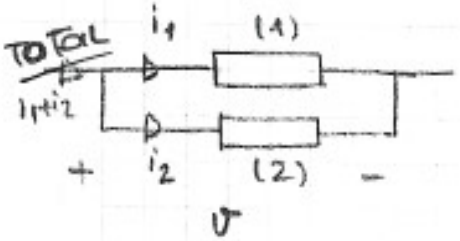
(1)

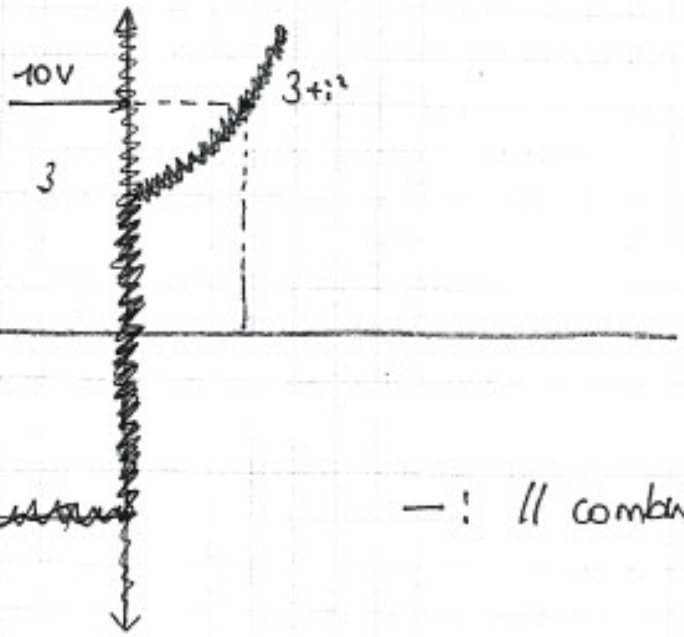


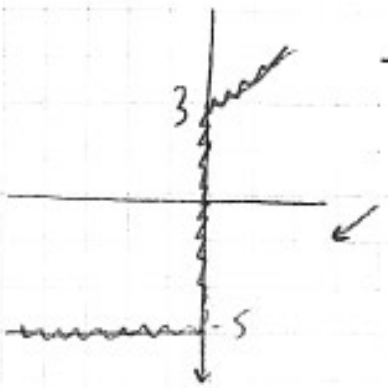
(2)







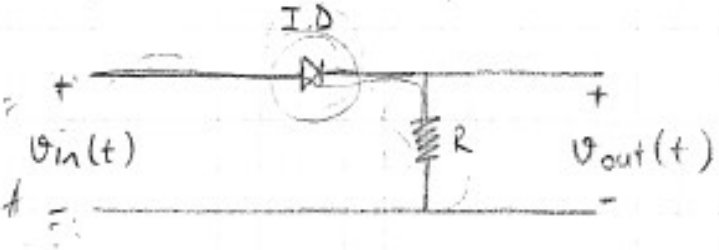




—: // combination

Diode Applications:

① Half-Wave Rectifier:

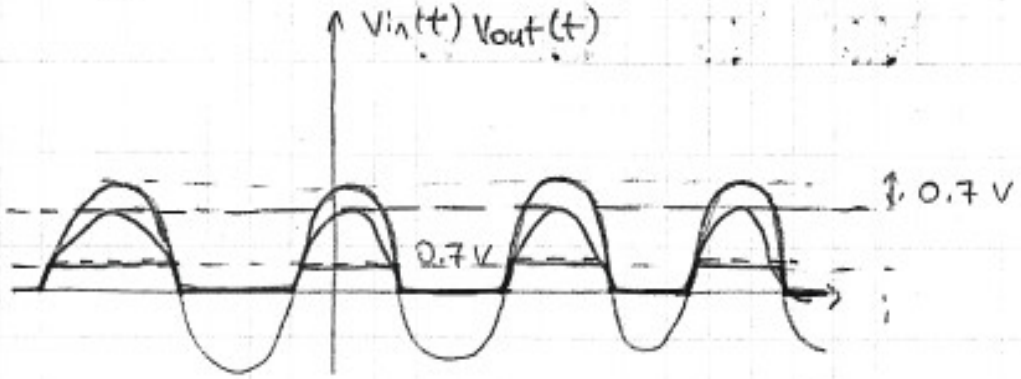


$$V_{out}(t) = \begin{cases} V_{in}(t) & V_{in}(t) > 0 \\ 0 & V_{in}(t) < 0 \end{cases}$$

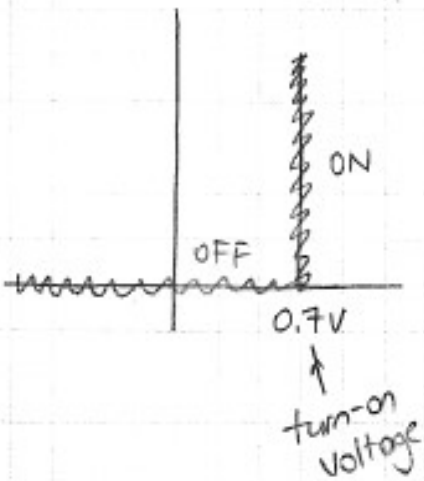
Check: $V_{in}(t) = A$

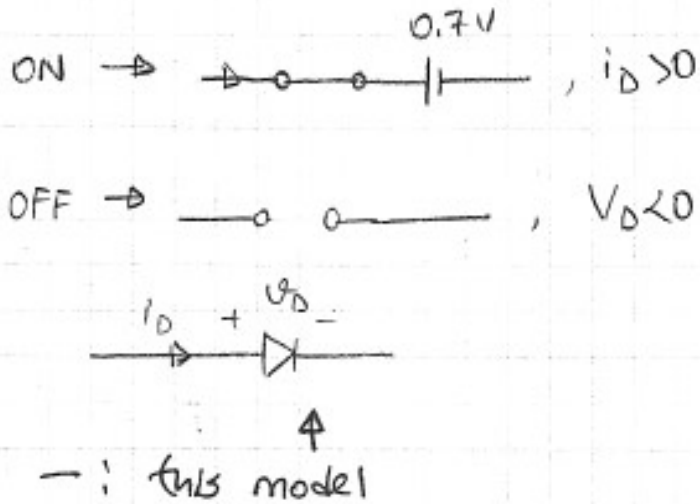
① $A > 0$, Diode ON, $V_{out}(t) = V_{in}(t)$

② $A < 0$, Diode OFF, $V_{out}(t) = 0$



Not Ideal





—: this model

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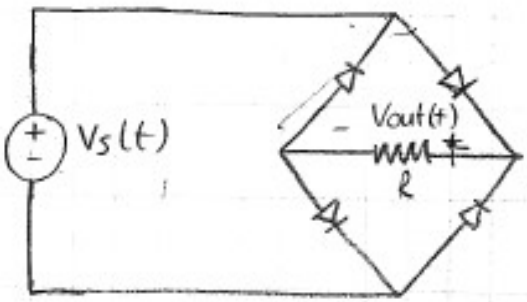
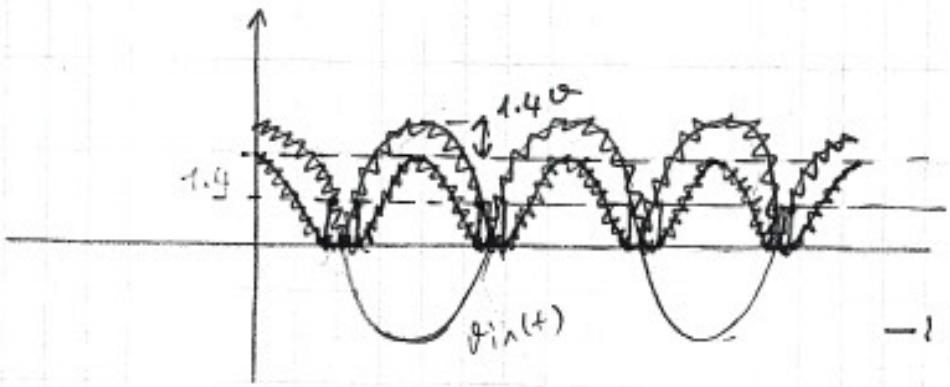
② Full - Wave Rectifier



Diodes are ideal

$V_{out}(t) = |V_{in}(t)|$



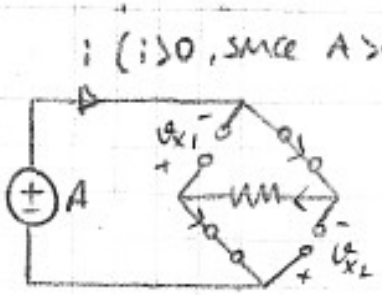
— : $v_{out}(t)$

— : not-ideal model $V_{out}(t)$

Check:

$V_S(t) = A$

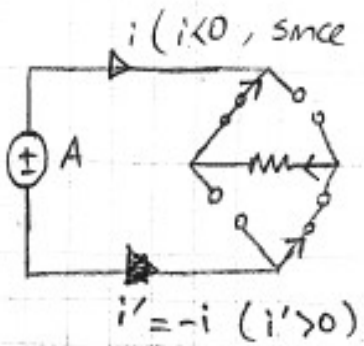
① $A > 0$



$V_{x1} = V_{x2} = -A$ OFF ✓

$v_{out}(t) = A$.

② $A < 0$



$v_{out} = i'R$

$= -A$

NOTE

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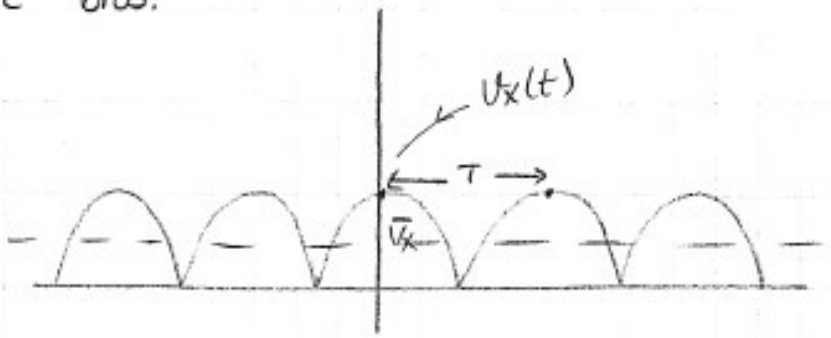
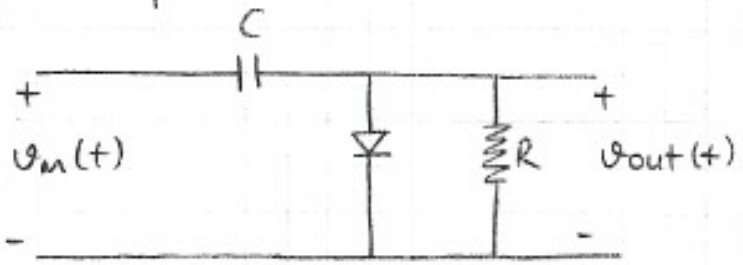
Full-wave Rectifiers are used to generate a non-zero DC bias.

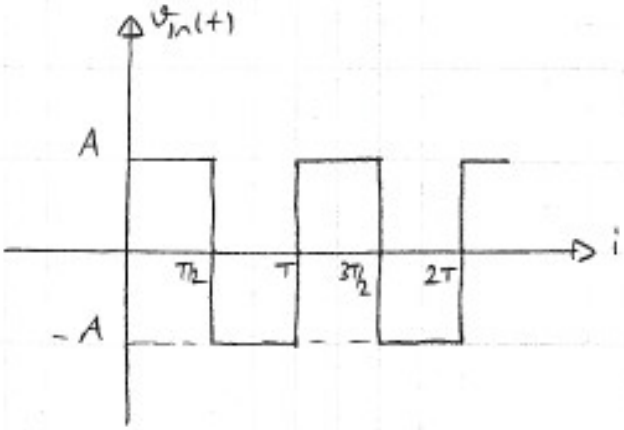


$$\frac{1}{T}\cdot\int_0^T v(t)\,dt \neq 0 = \overline{v_x}$$

(3) Clampers

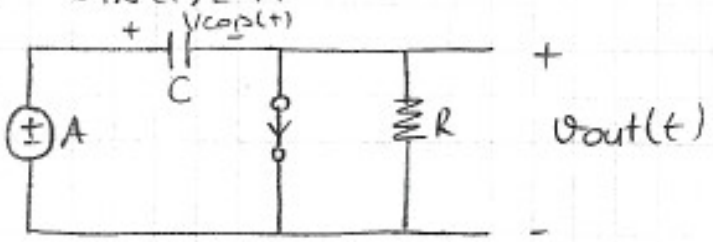


$RC >> T/2$



Period - T

Assume: $v_{IN}(t) = A$



Claim: Diode is ON., $v_{out}(t) = 0$ V;

$v_{cap}(t) = A$ V.

As soon as $v_{in}(t) = A \rightarrow$ Diode ON

$v_{out}(t) = 0$

$v_{cap}(t) = A$

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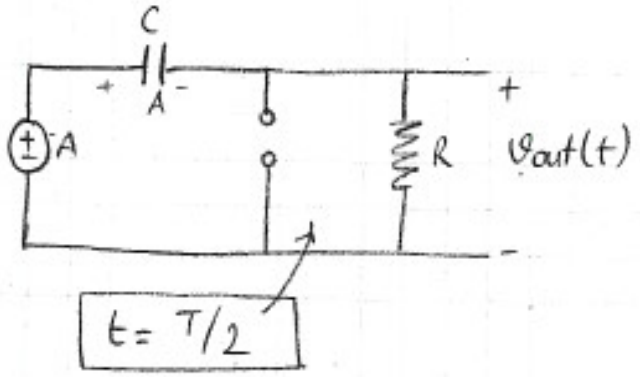
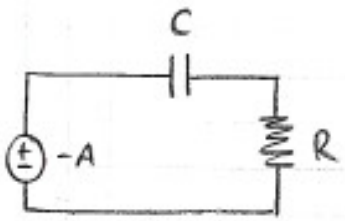
Assume : $v_{in}(t) = -A$

$t = T/2$

$v_{in}(T/2) = -A$



$v_{cap}(T/2^-) = A \rightarrow V_{cap}(T/2^+) = A$



$V_{cap}(T/2^+) = A$

$V_{cap}(t) = ?$ $\quad t \geq T/2$

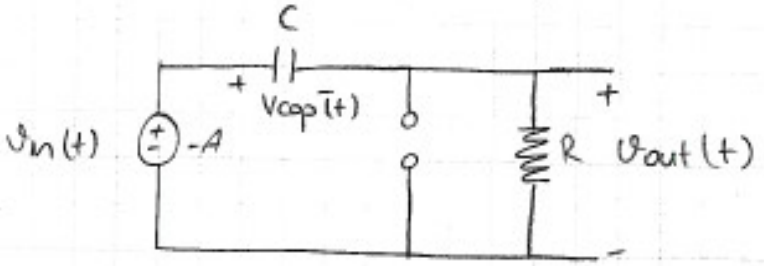
$$v_{cap}(t) = v_{final} + (v_{initial} - v_{final})\, e^{-\frac{(t-T/2)}{\tau}}, \quad t \geq T/2$$

For DC inputs

$v_{final} = -A$, $v_{initial} = A$, $\tau = -A$

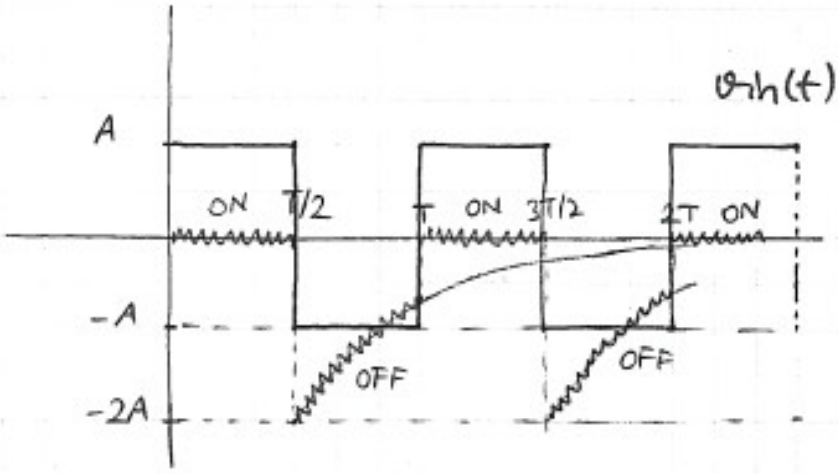
$$= -A + 2A \cdot e^{-\frac{(t-T/2)}{RC}}$$

$$= A\left(-1 + 2 \cdot e^{-\frac{(t-T/2)}{RC}}\right) \quad t \geq T/2$$



$$v_{out}(t) = v_{in}(t) - v_{cap}(t)$$

$$= -2A \cdot e^{-\frac{(t-T/2)}{RC}} \quad t > T/2$$



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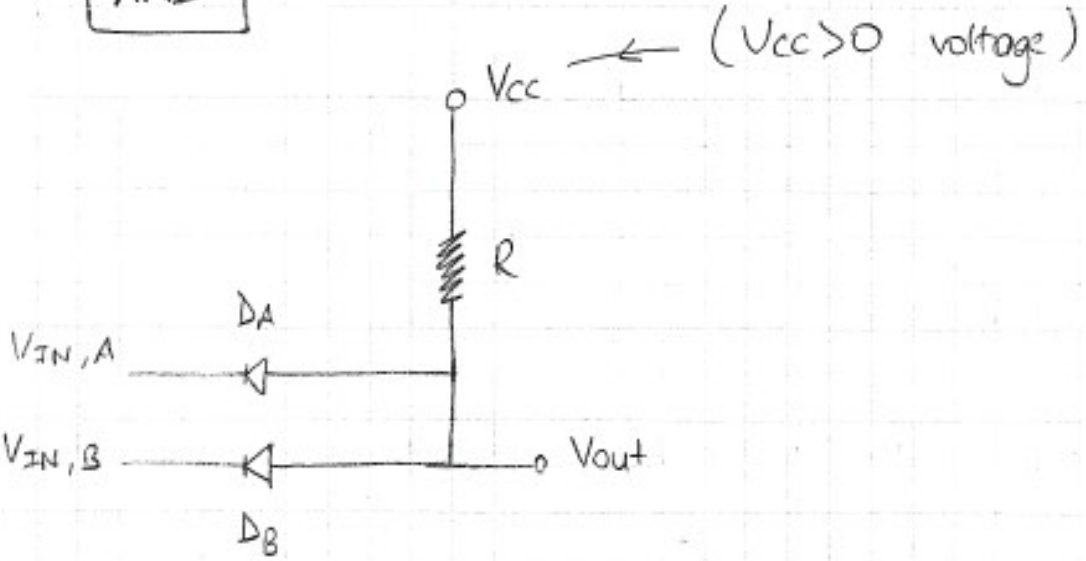
10.03.2010

Diode AND / OR Gates:

AND



A	B	D_A, D_B	Out
High	High	OFF, OFF	High (Vcc)
High	Low	OFF, ON	Low ($V_{IN} + U_{D(ON)}$)
Low	High	ON, OFF	Low
Low	Low	ON, ON	Low

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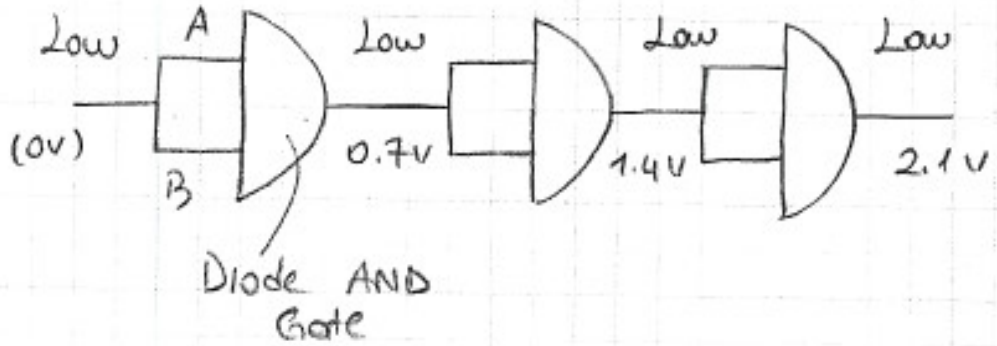
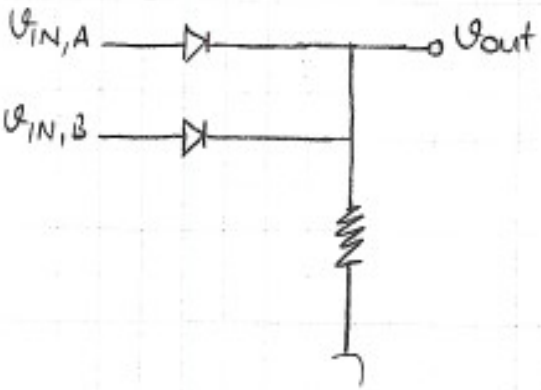
$V_{IN,A}$	$V_{IN,B}$	Vout
Vcc	Vcc	Vcc
Vcc	0	0.7
0	Vcc	0.7
0	0	0.7

$V_{D(ON)} = 0.7\ V$

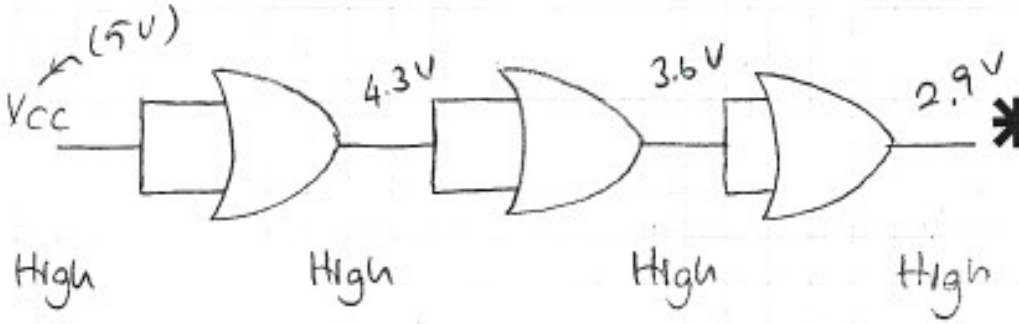


✓ Voltage level for low logic level increases as the number of cascades increases.

OR



$V_{IN,A}$	$V_{IN,B}$	Vout
0	0	0
Vcc	0	$V_{CC} - V_{D,(ON)}$
0	Vcc	$V_{CC} - V_{D(ON)}$
Vcc	Vcc	$V_{CC} - V_{D(ON)}$

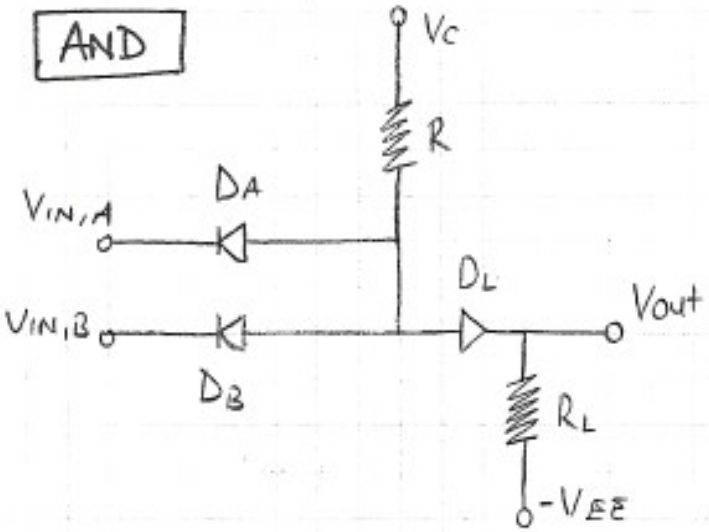


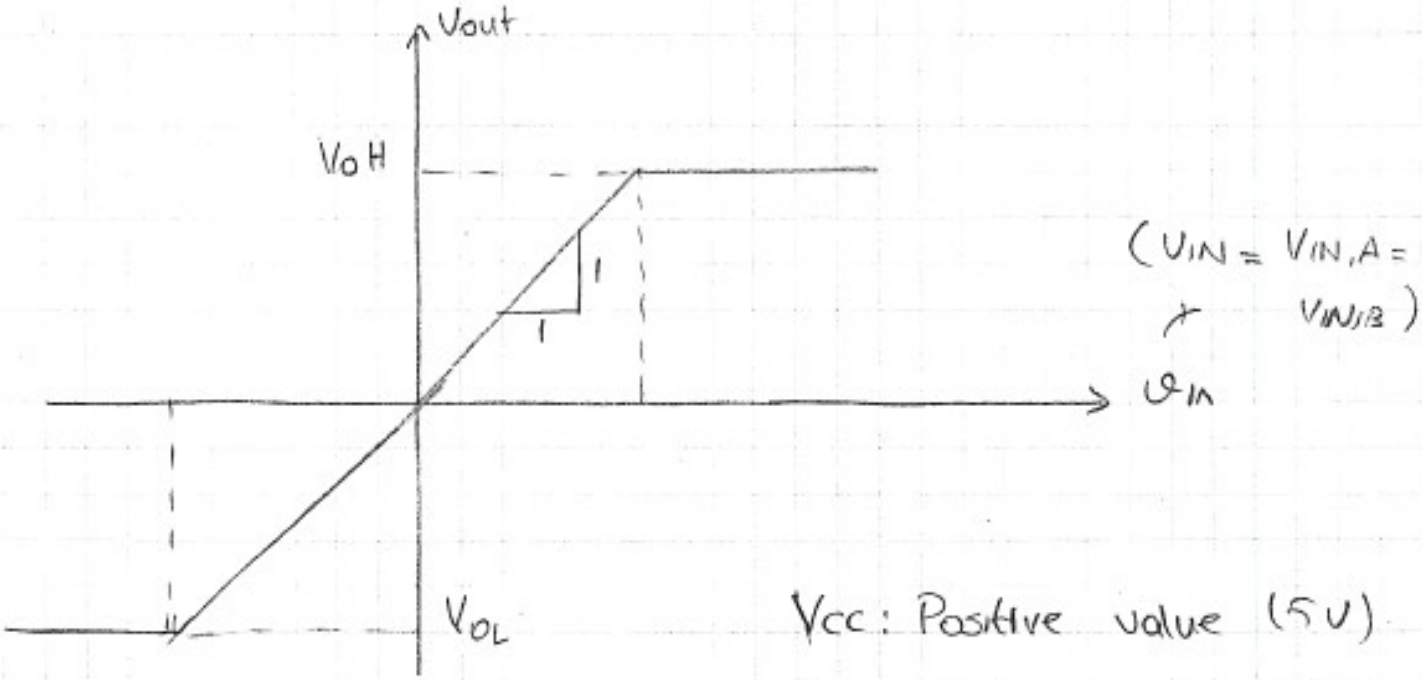
V_{CC} : Collector Voltage

↖ external power supply voltage

Level Shifted AND / OR Gates

AND





($V_{IN} = V_{IN,A} = V_{IN,B}$)

V_{CC} : Positive value (5V)

V_{EE} : Positive value (5V)

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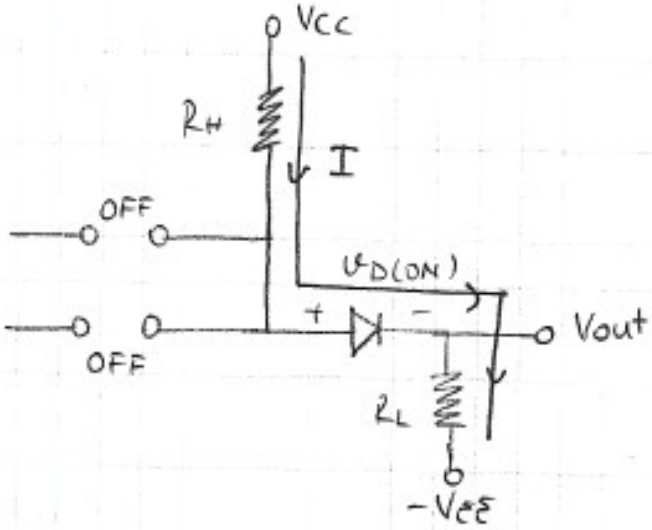
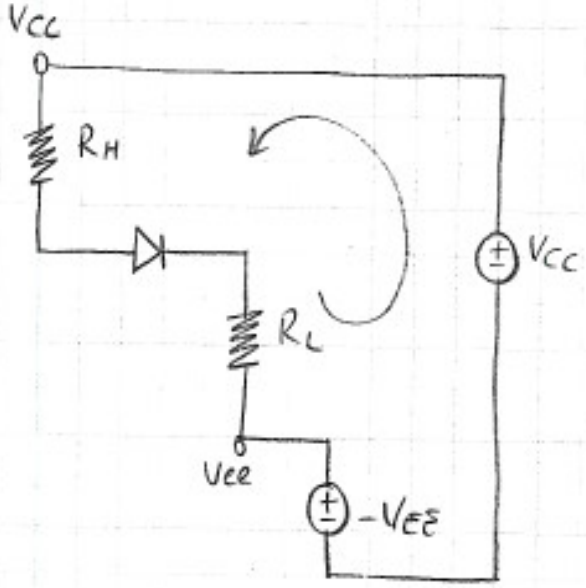
① Assume V_{IN} is sufficently high.

→ D_A, D_B : OFF



$$I = \frac{V_{CC} - (-V_{EE}) - V_{D(ON)}}{R_H + R_L}$$

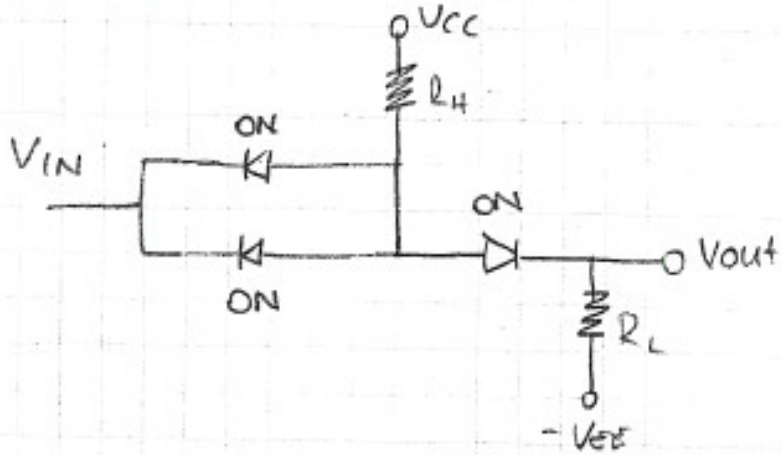


$$V_{out} = V_{CC} - R_H . I - V_{D(ON)}$$

$$V_{out} = V_{CC} - \frac{R_H}{R_H + R_L}\left(V_{CC} + V_{EE} - V_{D(ON)}\right) - V_{D(ON)}$$

$V_{out} = V_{OH}$

② When V_{IN} is low enough D_A, D_B will turn-ON and then we have



$$V_{out} = V_{IN} + V_{D(ON)} - V_{D(ON)}$$

$$V_{out} = V_{IN}$$

(3) When V_{IN} is very much low so that D_1 can not be ON.

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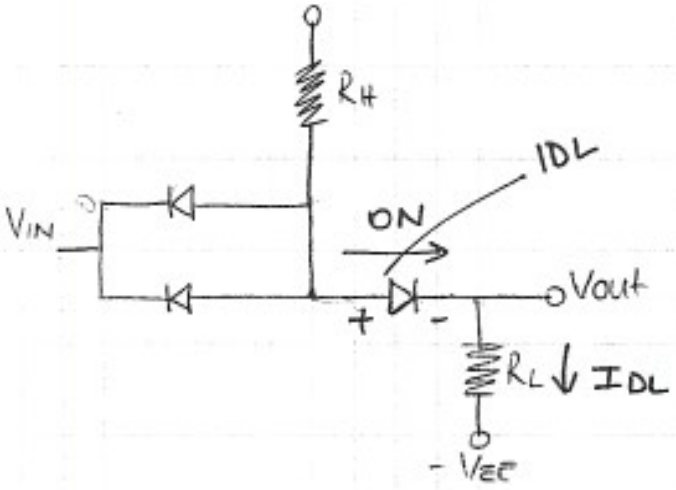
Remember for D_L to be ON, check $I_{DL} > 0$ this.

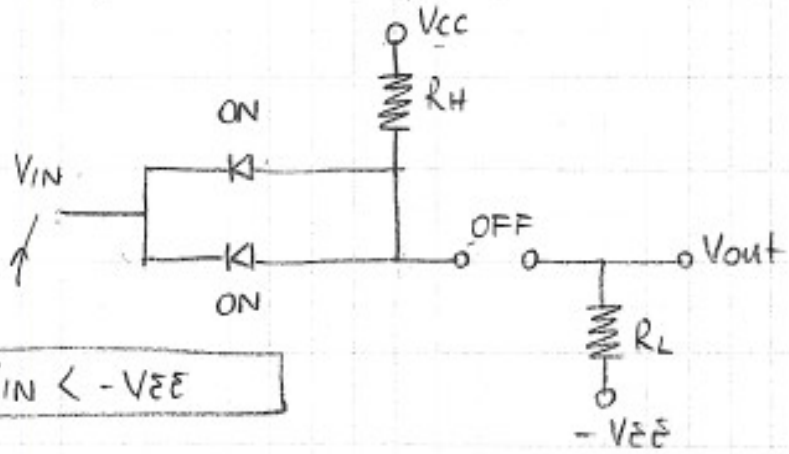


$$I_{DL} = \frac{V_{out} - (-V_{EE})}{R_L} = \frac{V_{out} + V_{EE}}{R_L}$$

✓ Then for the D_L diode to be ON $I_{DL} > 0$

$\Rightarrow V_{out} > -V_{EE}$

Then when we reduce V_{IN} below $-V_{EE}$ → D_L = OFF



$V_{IN} < -V_{EE}$

$V_{out} = -V_{EE}$

(ex)

$V_{CC} = 4V$

$-V_{EE} = -4V$

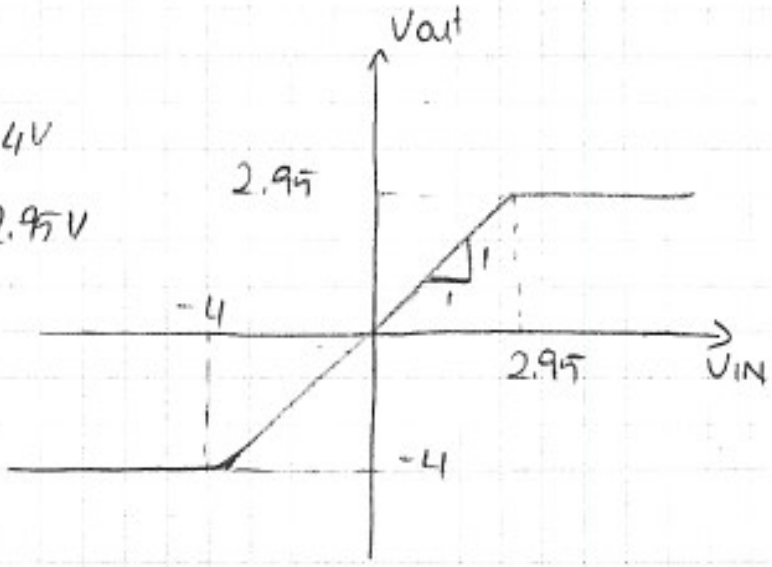
$V_{D(ON)} = 0.7\,V$

$R_H = 1\,k\Omega$

$R_L = 20\,k\Omega$

$V_{OL} = -4V$

$V_{OH} = 2.95\,V$



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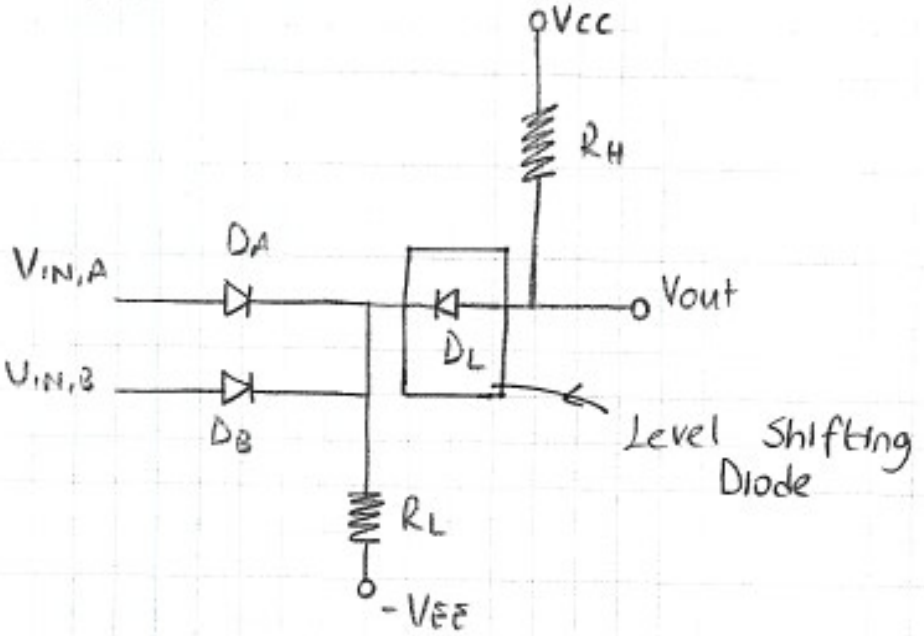
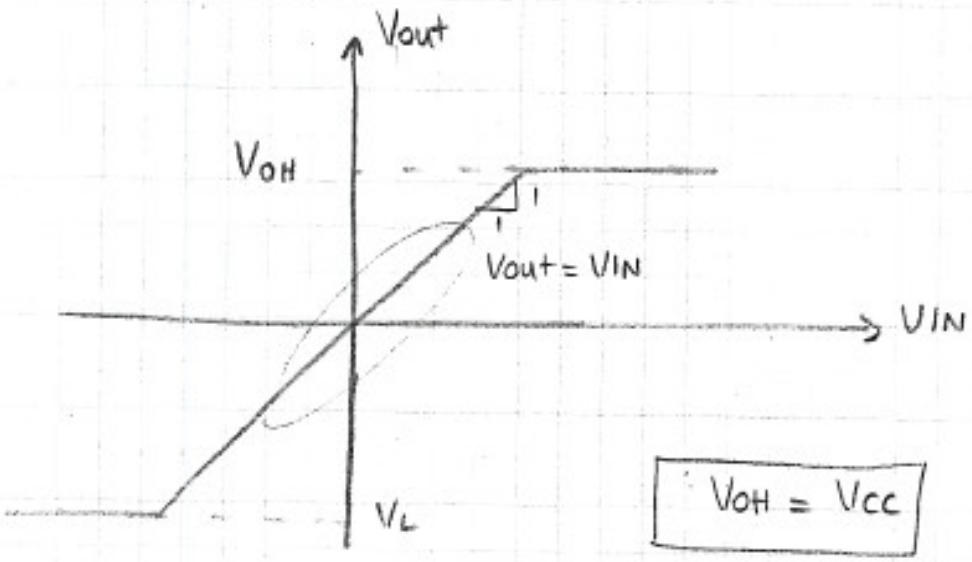
OR





$V_{OH} = V_{CC}$

$$V_{OL} = -V_{EE} + \frac{R_L}{R_H + R_L}(V_{CC} + V_{EE} - V_{D(ON)}) + V_{D(ON)}$$

12.03.2010

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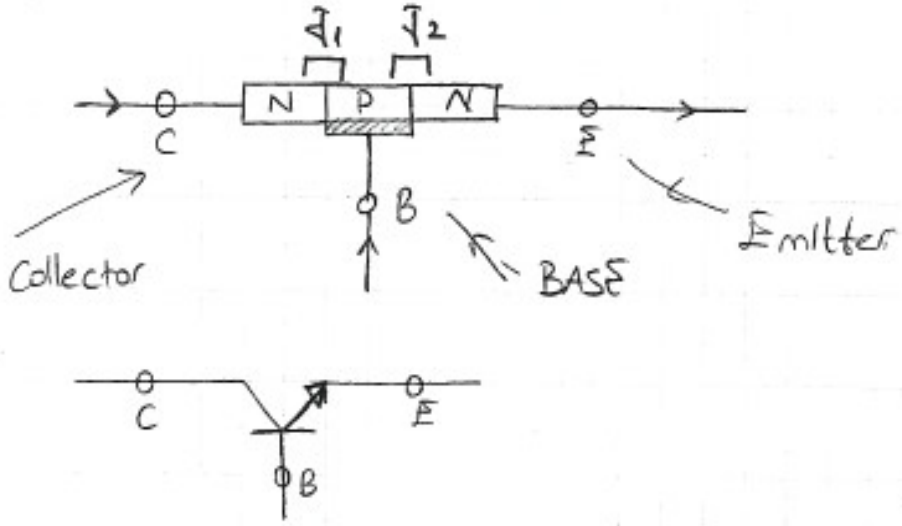
Bipolar Junction Transistors : (BJT)

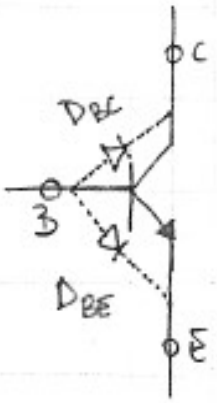


(npn - BJT)

Applications

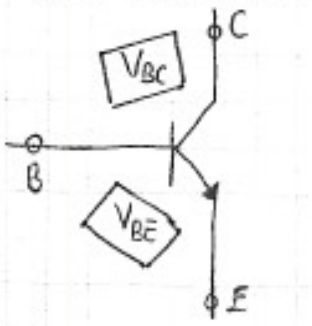
① Amplifier

② Switch

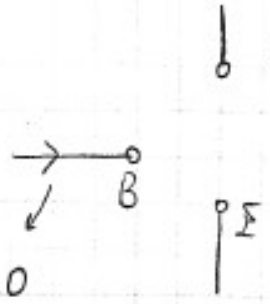


D_{BE}	D_{BC}	Transistor Diode (Mode)
OFF	OFF	OFF
ON	OFF	FA (Forward Active)
OFF	ON	RA (Reverse Active)
ON	ON	SAT (Saturation)

OFF Mode :



$\Rightarrow$ OFF



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Conditions:

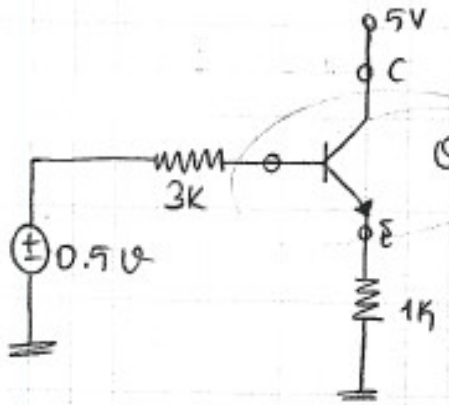
① $V_{BE} < V_{BE(ON)}$

② $V_{BC} < V_{BC(ON)}$

$V_{BE} = V_B - V_E$

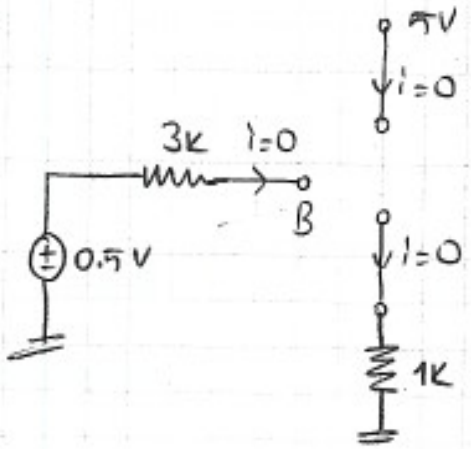
$V_{BE(ON)}$: Turn-on voltage for BE junction.

(ex)



$V_{BE(ON)} = V_{BC(ON)} = 0.7\ V$,

→ Assume OFF



▷ $V_B = 0.5 - 0 = 0.5\ V$,

$V_E = 0\ V$,

$V_C = 5\ V$,

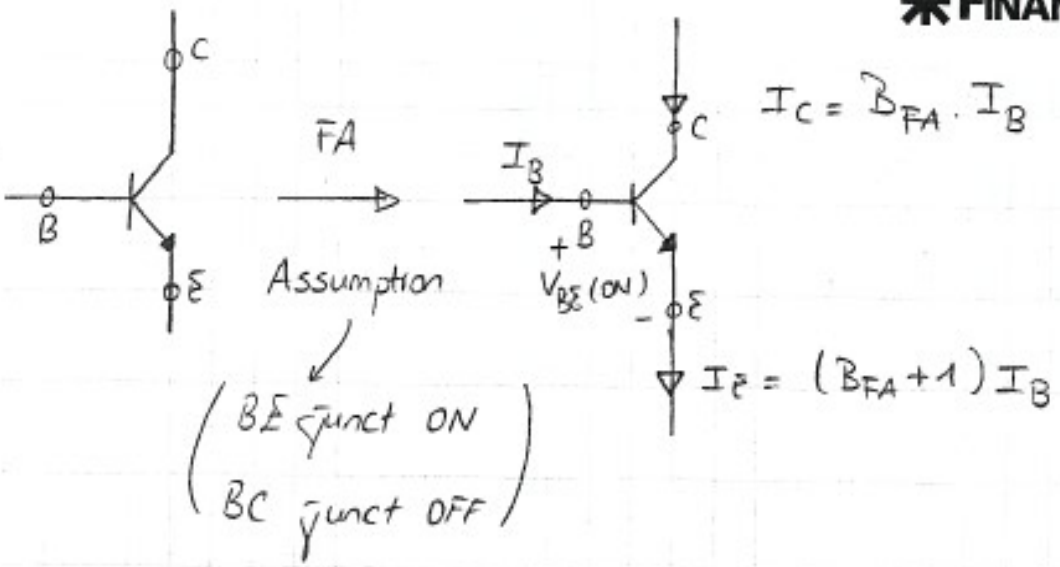
$V_{BE} = 0.5\ V < V_{BE(ON)}$ ✓

$V_{BC} = 0.5 - 5 = -4.5 < V_{BC(ON)}$ ✓

} OFF assumption is correct.

* if $0.5\ V \Rightarrow$ was $2\ V \Rightarrow V_{BE}$ would satisfied.

Forward Active:



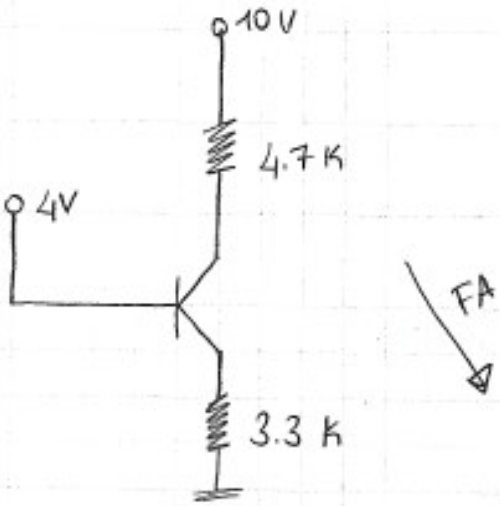
β_{FA} : current amplification factor. ($\beta_{FA} \cong 100$)

Conditions:

① $I_B > 0$

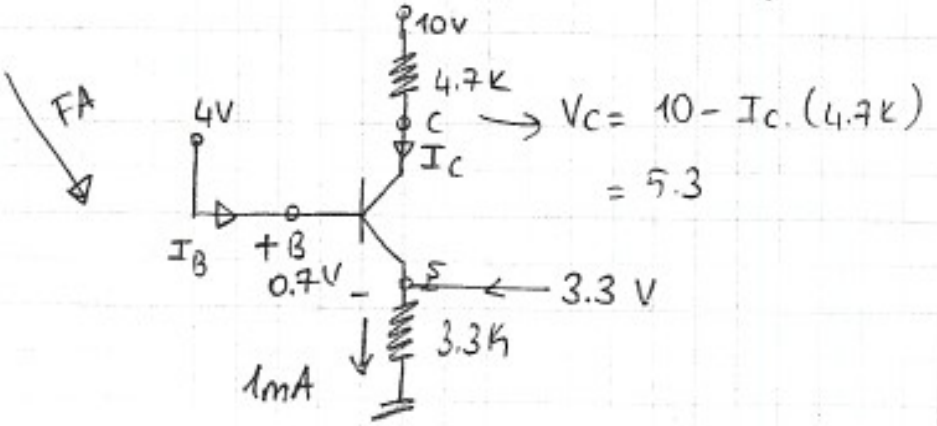
② $V_{BC} < V_{BC\,(ON)}$

ex



$\beta_{FA} = 100$;

$V_{BE\,(ON)} = V_{BC\,(ON)} = 0.7\,V$;



$I_E = 1mA$

$I_B = \dfrac{1mA}{(\beta_{FA}+1)} = \dfrac{1mA}{101}$ mA

$I_C = \beta_{FA} \cdot I_B = \dfrac{100}{101}$ mA $= 0.99$ mA

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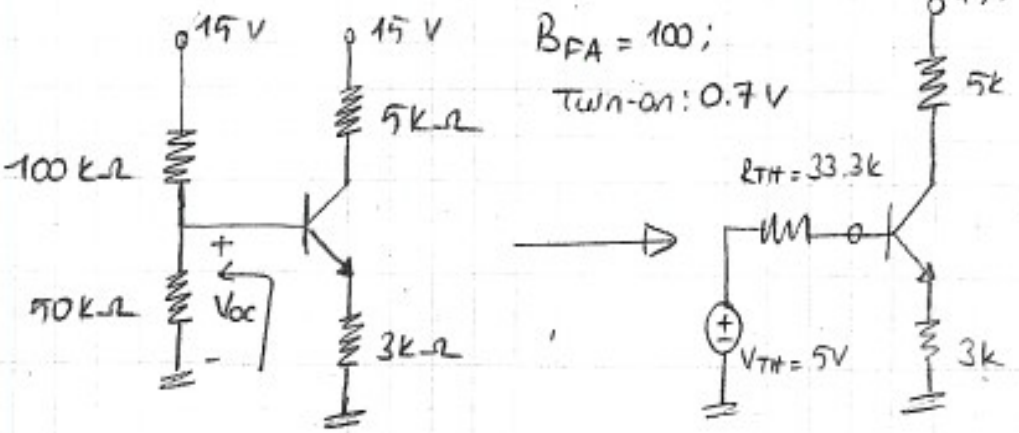
Let's Check FA conditions:

① $I_B > 0$ ✓

② $V_{BC} < V_{BC(ON)}$

$4 - 5.3 = -1.3 < 0.7$ ✓

(ex)



$\beta_{FA} = 100$;

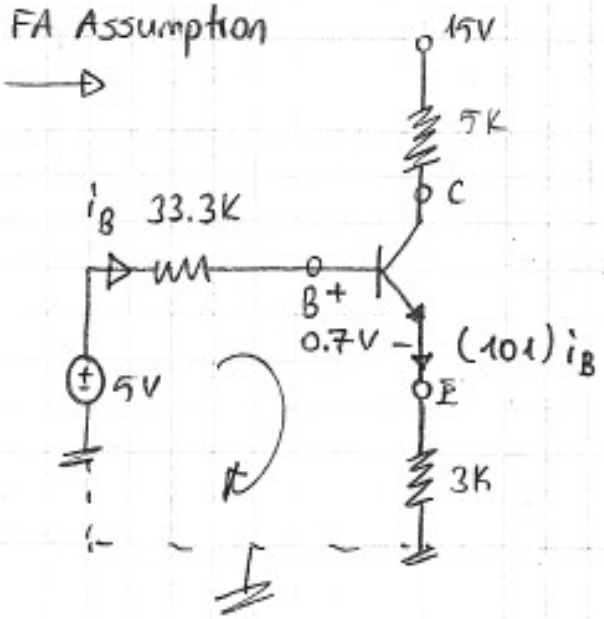
Turn-on: 0.7 V

$$V_{OC} = \frac{15}{150k} \cdot 50k = 5V$$

$$R_{TH} = 50 // 100 = 50 \cdot \frac{2}{3} = 33.3\ k\Omega$$

303
33.3

FA Assumption →



KVL:

$$-5 + (33.3)\,i_B + 0.7 + (101)3\,i_B = 0$$

(i_B in mA)

$$i_B = \frac{(336.3)}{4.3}\ mA$$

$$\boxed{i_B = 0.0128\ mA} = 12.8\ \mu A$$

Check FA conditions:

① $i_B > 0$ ✓

② $V_{BC} < V_{BC(ON)}$

→

② $V_B = 5 - (33.\bar{3})\, i_B$ (i_B in mA)

$V_B = 4.03\ V$;

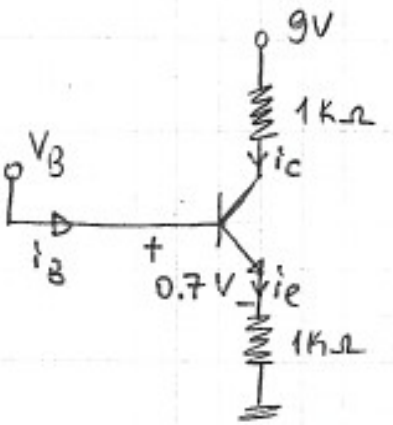
$v_C = 15 - (5).(100\, i_B)$ (i_B in mA)

$v_C = 8.6\ V$;

$V_{BC} = 4.03 - 8.6 = -4.97\ V < V_{BC(ON)}$ ✓

✓ FA assumption is TRUE.

(ex)



Transistor has a high B_{FA}. Find the max. value for V_B s.t transistor is in FA.

$I_e = \frac{V_B - 0.7}{1K} = (V_B - 0.7)\ mA$

$I_B = \frac{I_E}{B_{FA}+1} = \frac{(V_B - 0.7)}{B_{FA}+1}\ mA$ ⇝ For FA

① $i_B > 0 \rightarrow \boxed{V_B > 0.7\ V;}$

$V_{BC} = V_B - (9 - I_C \cdot 1K)$

$= V_B - 9 + B_{FA} \cdot \frac{I_E}{B_{FA}+1}$

$= V_B - 9 + V_B - 0.7$ (since B_{FA} is high)

$= 2V_B - 9.7$

$V_{BC} < V_{BC(ON)} \rightarrow \boxed{V_B < 5.2}$ (0.7)

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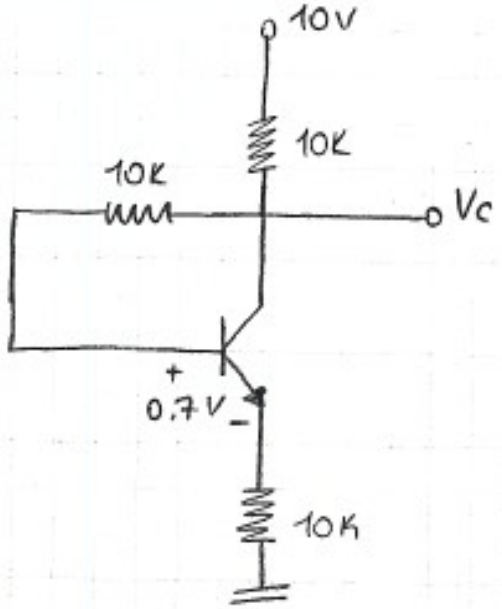
(ex)

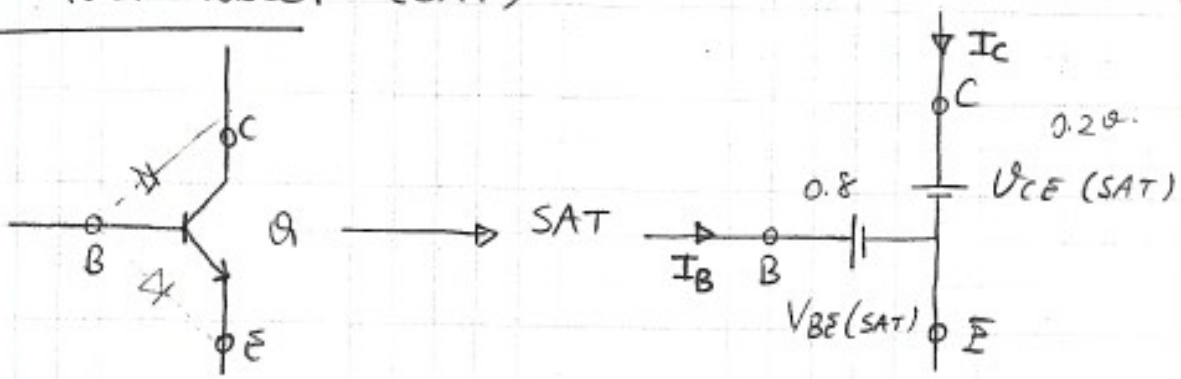


Find V_C $(B_{FA} = 100)$

Ques 5

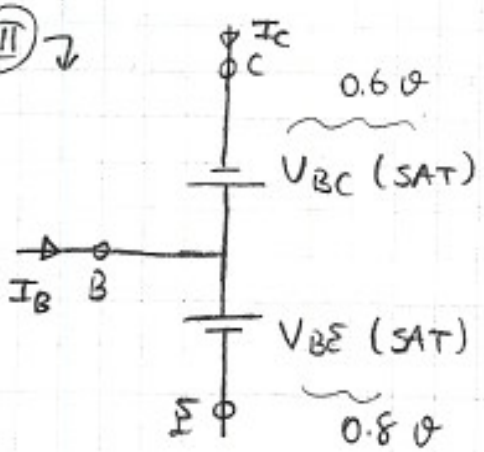
17.03.2010

Saturation Mode: (SAT)



(I)

(II)



Conditions:

(1) $B_{FA} I_B > I_C$

(2) $I_B > 0$

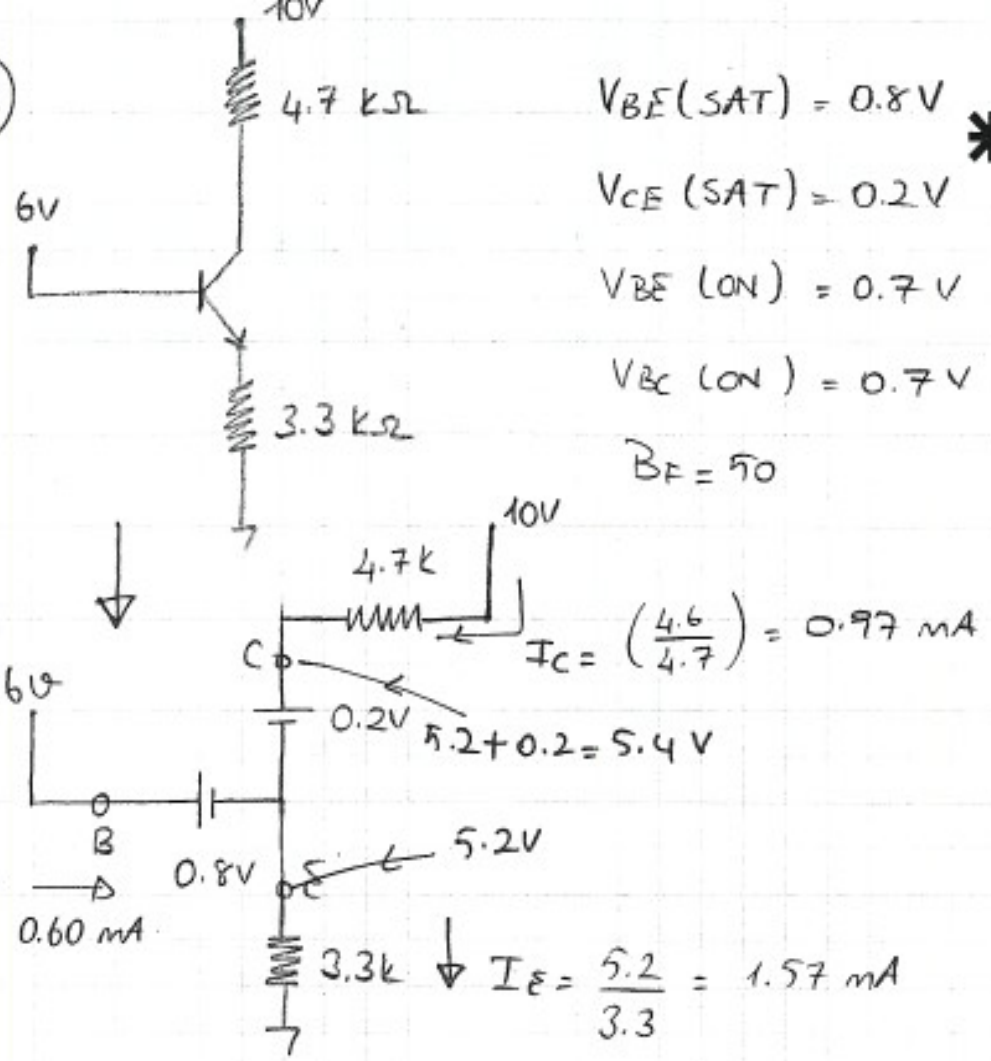
$$V_{CE(SAT)} = V_C(SAT) - V_E(SAT)$$

$$= V_{BE}(SAT) - V_{BC}(SAT)$$

$$= V_B^{SAT} - V_E^{SAT} - V_B^{SAT} + V_C^{SAT}$$

$$= V_C^{SAT} - V_E^{SAT}$$

(ex)



$V_{BE(SAT)} = 0.8\,V$

$V_{CE(SAT)} = 0.2\,V$

$V_{BE(ON)} = 0.7\,V$

$V_{BC(ON)} = 0.7\,V$

$B_F = 50$

$I_C = \left(\frac{4.6}{4.7}\right) = 0.97\ mA$

$I_E = \frac{5.2}{3.3} = 1.57\ mA$

Check conditions:

① $I_B > 0$ ✓

② $B_F A\ I_B > I_C$ ✓

$50 \quad 0.6 \quad > \quad < 0.97$

$G = \frac{B_F I_B}{I_C} > 1$ for SAT

↑ Depth of saturation $\quad G = \frac{30}{0.97} = 30$ ✓

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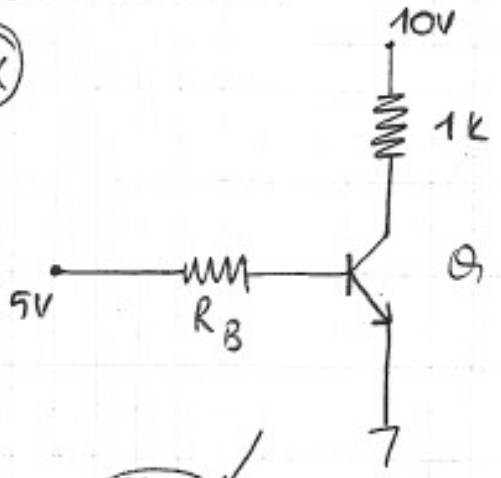
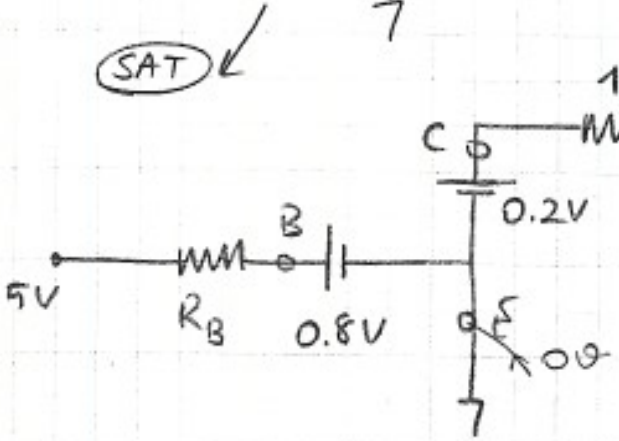
ex



Find the range for R_B such that Q is in SAT

SAT



$I_C = 0.8\ mA$

$$I_B = \frac{5 - 0.8}{R_B}$$

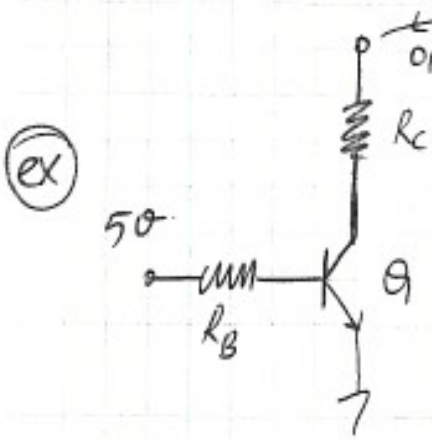
check cond.

① $I_B > 0 \longrightarrow R_B > 0$

② $\beta_F I_B > I_C \longrightarrow \dfrac{50\,(5-0.8)}{R_B} > 0.8\ mA$

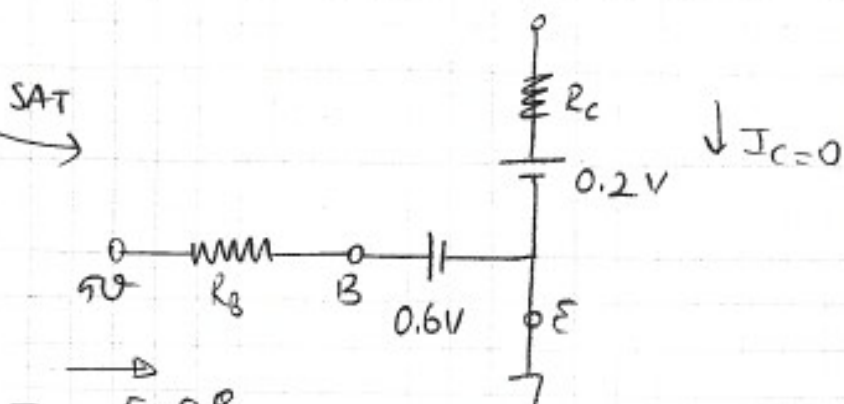
$$R_B < \frac{50\,(5-0.8)}{0.8\ mA} = 21.4\ k\Omega$$

ex



Find R_B such that Q is in SAT.

SAT



$$I_B = \frac{5 - 0.8}{R_B}$$

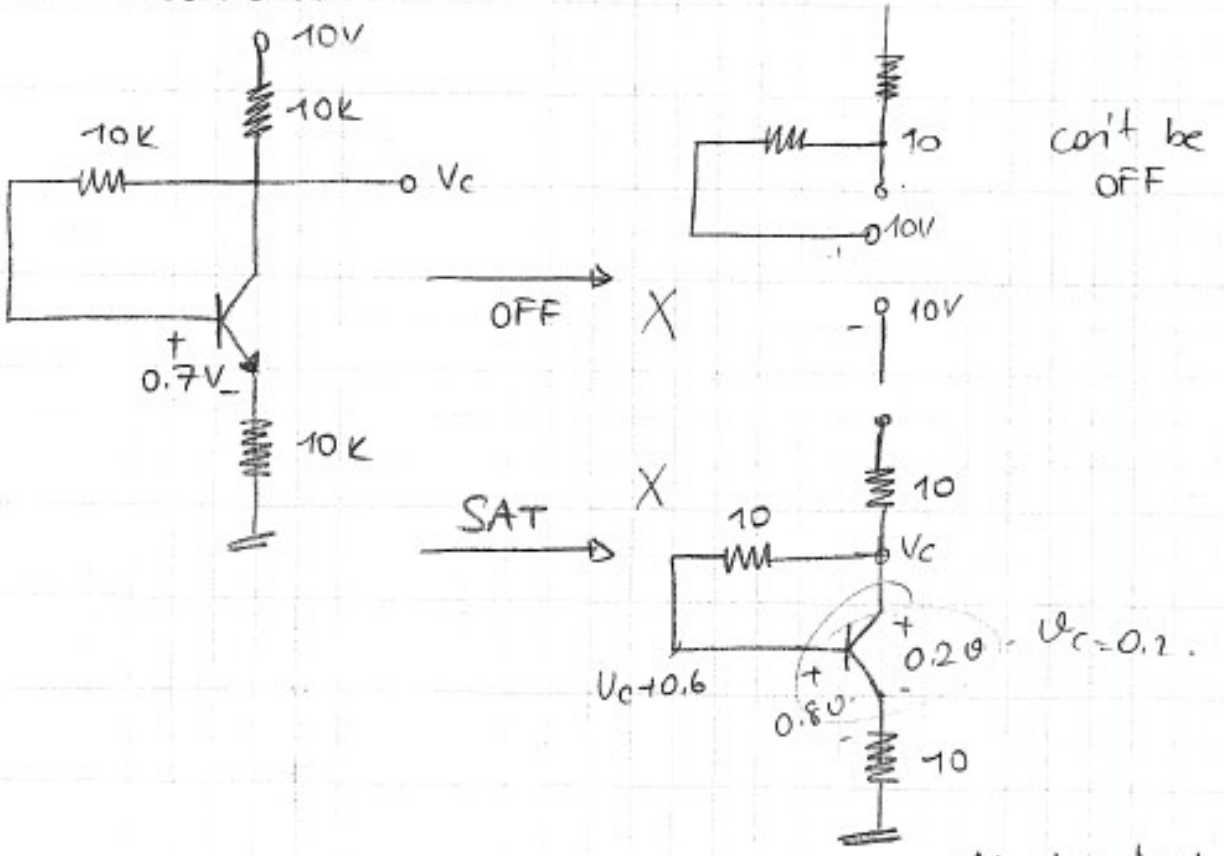
conditions

① $I_B > 0 \longrightarrow R_B > 0$

② $\beta_F I_B > I_C \longrightarrow \beta_F I_B > 0 \longrightarrow I_B > 0$

Any positive R_B (any R_B) moves the Q into SAT region.

EXERCISE SOLUTION:



Akımları bul.

$$0 = \frac{10 - V_C}{10} + \frac{V_C + 0.6}{10} + \frac{V_C}{10} - \frac{V_C + 0.6}{10}$$

$$V_C = 5.1$$

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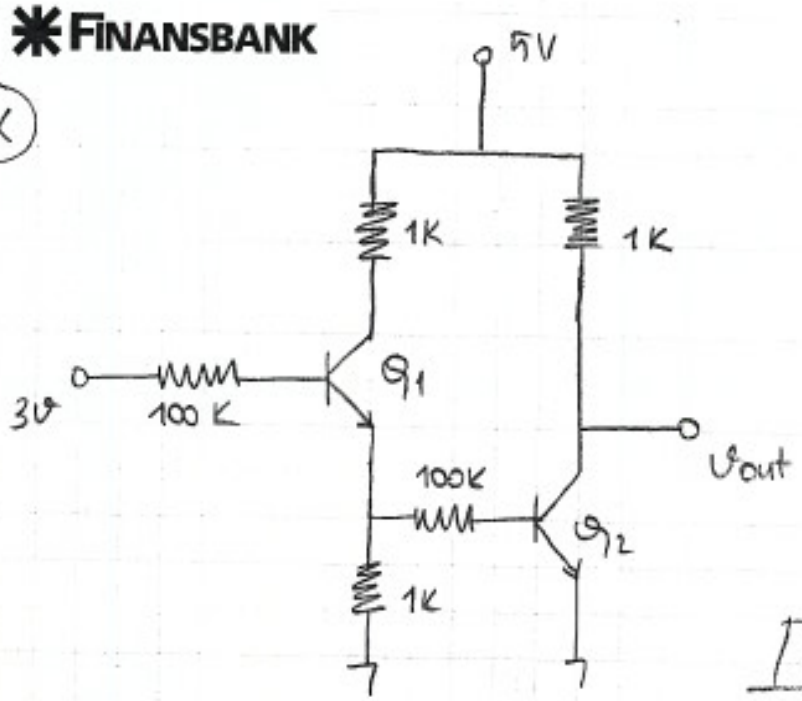
19.03.2010

(ex)



$B_F = 99$

$V_{BE}(ON) = V_{BC}(ON)$

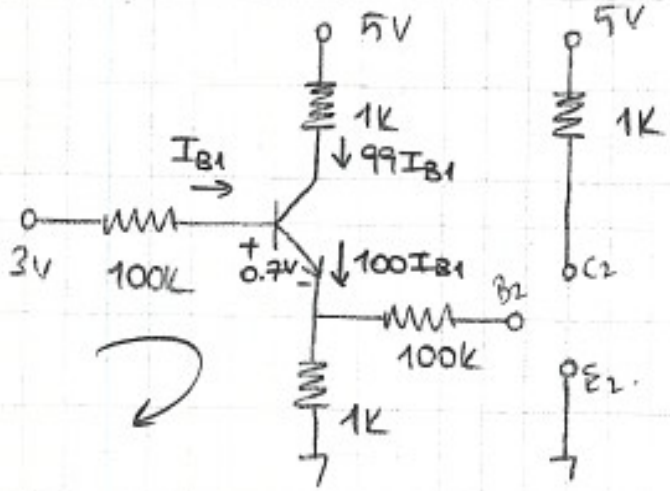
$= 0.7\ V$

$V_{CE}(SAT) = 0.2\ V$

$V_{BE}(SAT) = 0.8\ V$

$\boxed{v_{out} = v_{C_2}}$

(1) Q_1 : FA , Q_2 : OFF



KVL ↻ : $-3 + 100I_{B1} + 0.7 + 100I_{B1} \cdot 1 = 0$

$$I_{B1} = \frac{2.3}{200} = 11.5\ \mu A$$

check assumptions

Q_1 for FA :

(1) $V_{BC_1} \overset{?}{<} 0.7$

$V_{B1} = 3 - I_{B1} \cdot 100K$

$= 3 - 1.15 = 1.85\ V$

$V_{C1} = 5 - 99I_{B1} \cdot 1K$

$= 3.87\ V$

→

$V_{B1} - V_{C1} = -2.02$ ✓

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Q_2 : OFF

① $V_{BE_2} \overset{?}{<} 0.7$

② $V_{BC_2} \overset{?}{<} 0.7$

1.

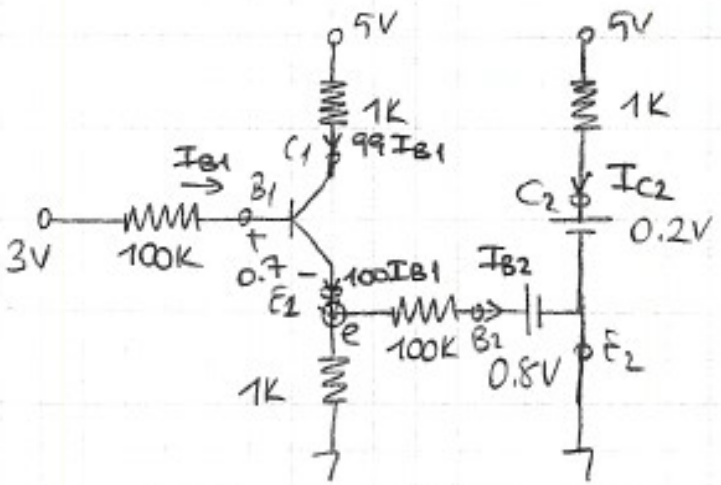
$V_{B2} = 100 I_{B1} \cdot 1K$ $\qquad V_{E_2} = 0V$

$= 1.15$ V

$V_{BE_2} = 1.15 - 0 = 1.15$ ✗ $\not< 0.7$

not satisfied ?

② Q_1 : FA , Q_2 : SAT



KCL at e : $100 I_{B1} = \frac{e}{1k} + \frac{e-0.8}{100K}$

$$I_{B1} = \frac{3-(e+0.7)}{100K}$$

$$\frac{3-(e+0.7)}{1K} = \frac{e}{1K} + \frac{e-0.8}{100K}$$

$$2.308 = 2.01e$$

$$\boxed{e = 1.148 \text{ V}}$$

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$$I_{B1} = \frac{3-(1.148+0.7)}{100}\ mA \qquad I_{E1} = (\overbrace{B_F}^{100}+1)\, I_{B1}$$

$$I_{B1} = 11.52\ \mu A \qquad = 1.152\ mA$$

$$I_{C1} = I_{E1} = I_{B1} = B_F I_{B1} = 1.14\ mA$$

$$I_{B2} = \left(\frac{e-0.8}{100}\right) mA = 3.4\ \mu A$$

$$I_{C2} = \left(\frac{5-0.2}{1}\right) mA = 4.8\ mA$$

Check conditions:

Q_1: FA.

① $V_{BC_1} \overset{?}{<} 0.7$ ✓

$V_{B1} = e + 0.7 = 1.848\ V$

$V_{C1} = 5 - 1K.99 I_{B1} = 3.86\ V$

} $V_{BC_1} = -\ldots$

Q_2 : SAT

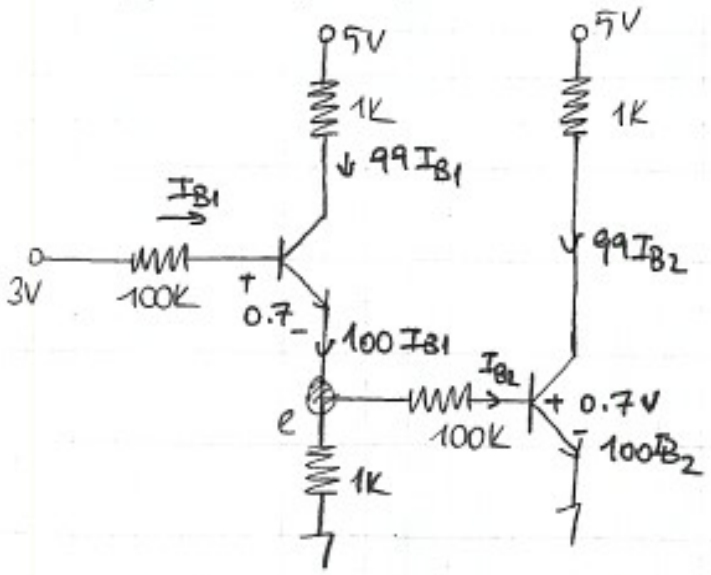
① $I_{B2} > 0$ ✓

② $B_F I_B > I_C$

$99.(3.4\ \mu A) \overset{?}{>} 4.8\ mA$ ✗ NOT SATISFIED

(FA, SAT) is not the correct state pair.

③ Q_1: FA , Q_2: FA



KCL at e:

$$\frac{e}{1} + \frac{e-0.7}{100K} - 100\,I_{B1} = 0$$

$$I_{B1} = \frac{3-(e+0.7)}{100K}$$

$$e = 1.147\ V$$

So, e is almost as in previous case

→ Then, Q_1: FA assumption still holds.

Let's check Q_2 then:

Q_2: FA

① $V_{BC_2} \overset{?}{<} 0.7\ V$

$V_{B2} = 0.7\ V$

$V_{C2} = 5 - 99 I_2 \cdot 1K$

$\overset{\wedge}{=} 5 - 0.447 = 4.553\ V$

$I_{B2} = \left(\frac{e-0.7}{100K}\right) = \frac{0.447}{100K}$ (1.147)

V_{BC_2} is negative < 0.7 ✓

23.03.2010

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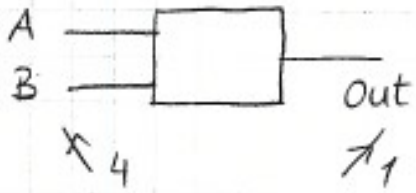
Properties & Definitions for Digital I.C's:

LOGIC GATES:

AND, OR, NAND, NOR, NOT, XOR



A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1

2^4 — 16 possible output comb.

✓ Implement any logic function using {NOT, OR} or {NOT, AND}

GATES:

✓ Sequential Gates (with memory) [State Machine]

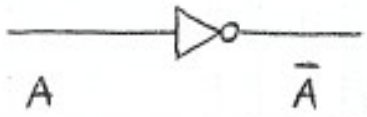
✓ Combinational Gates (without memory)

Positive Logic: → High Voltage represents "1"
→ Low Voltage represents "0"

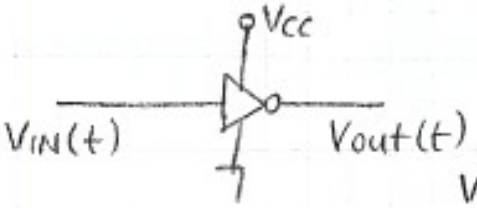
(Negative Logic: opposite Positive Logic)

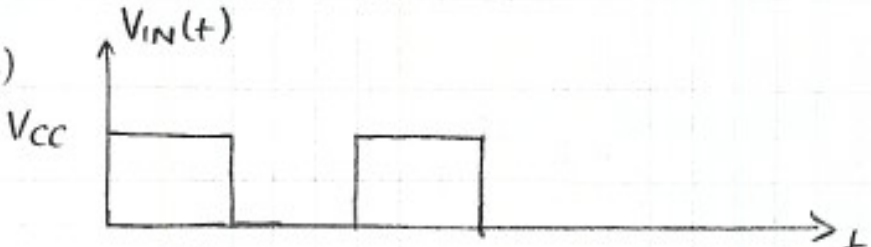
We will be using Positive Logic.

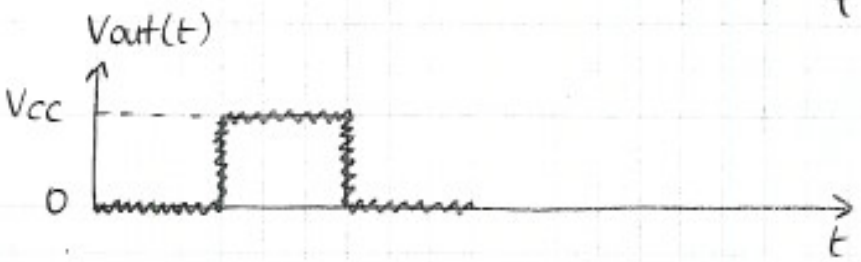
Ideal Inverter :

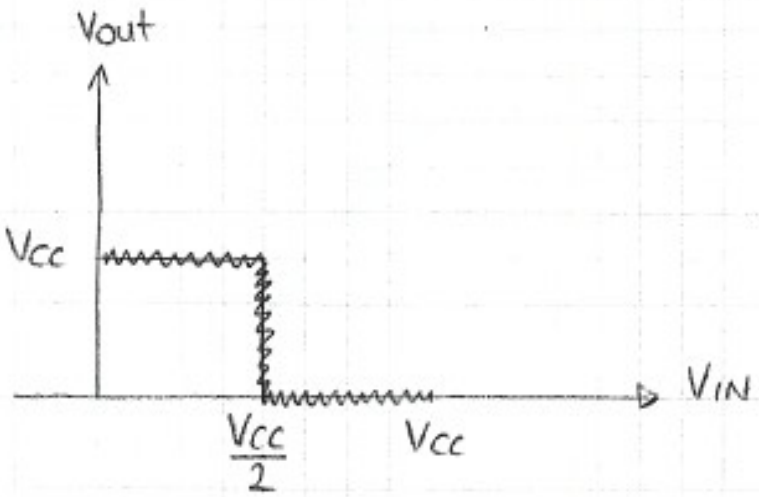


A	$\bar{A}$
1	0
0	1





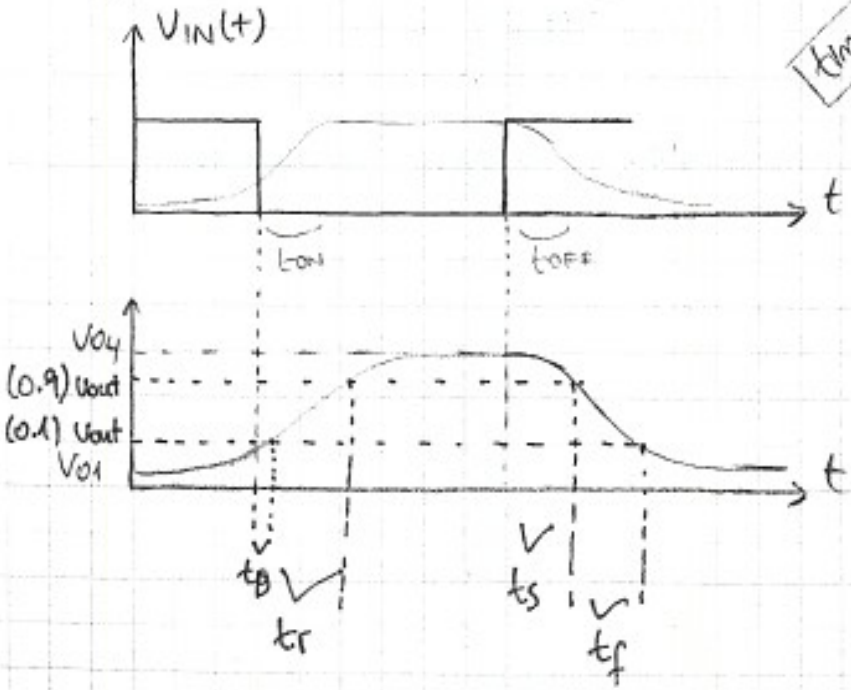




Ideal Voltage Transfer Characteristic

Transient Characteristics

timing diagram



ts : storage time

tf : fall time

tOFF = ts + tf : OFF time.

tD : delay time

tR : rise time

tON = tD + tR : ON time

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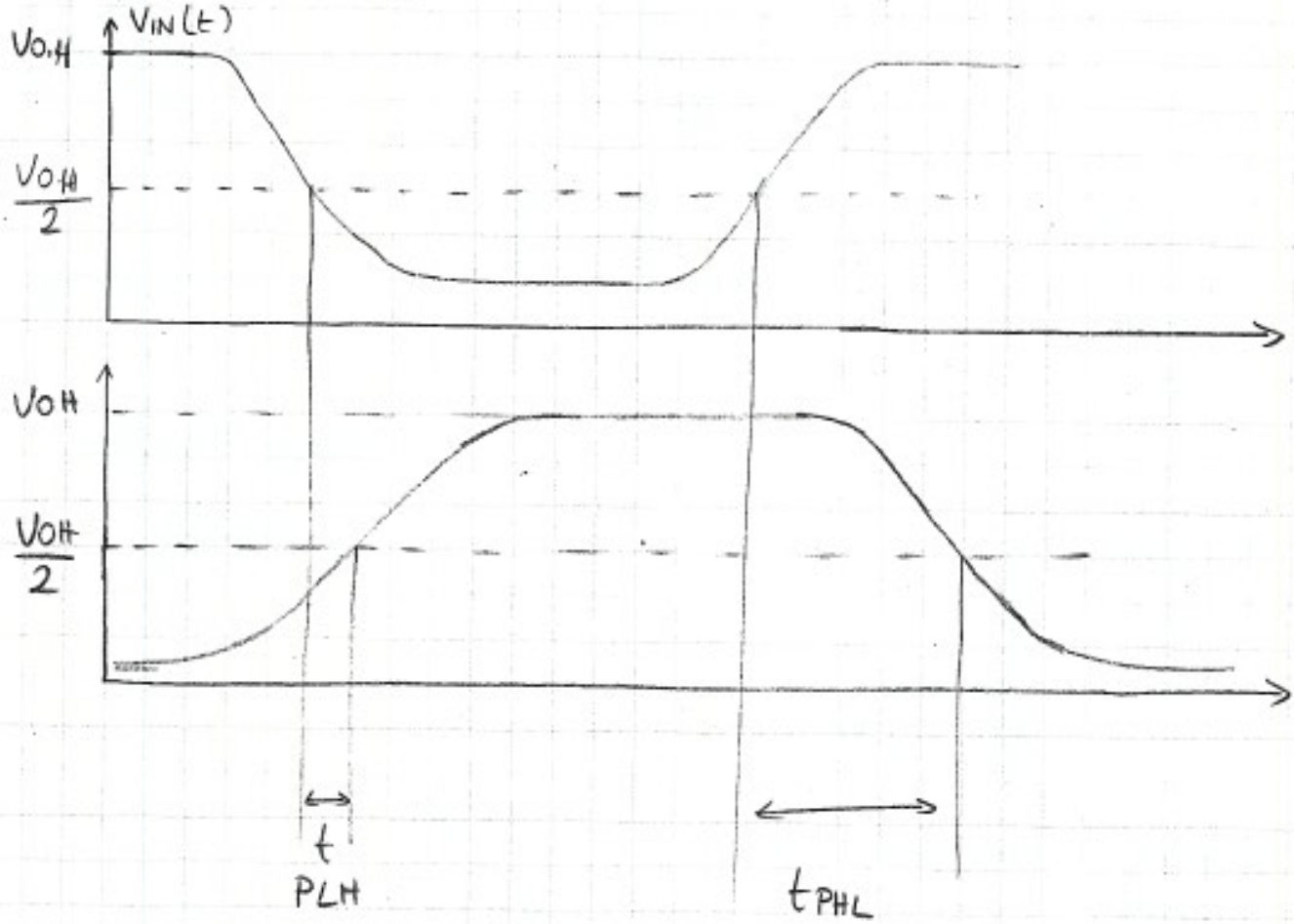
t_R, t_F : related to charcing and discharging of capacitors in the system

t_D, t_S : related to charge removal at PN junctions.

Propegation Delay :



t_{PLH} : Propegation Delay for Low → High transition.

Power Dissipation:

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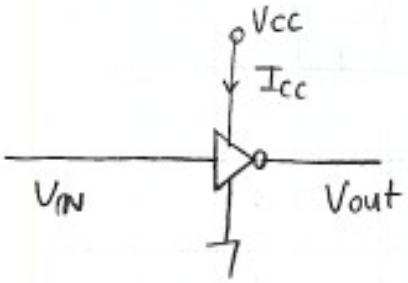

$I_{CC(OH)}$: Current supplied at OH (output high)

$I_{CC(OL)}$:

$$P_{CC}^{AVG} = V_{CC} \frac{(I_{CC(OH)} + I_{CC(OL)})}{2}$$

Relation Between Power Consumption & Transient Times:

Power ↑ ⟶ (implies) Transient Times ↓

Power ↓ ⟶ Transient Times ↑.

Power-Delay Product : multiplication of avarage power and fastest switching time.

Power-Delay product gives us some understanding on the technology and operation of logic gates.

→

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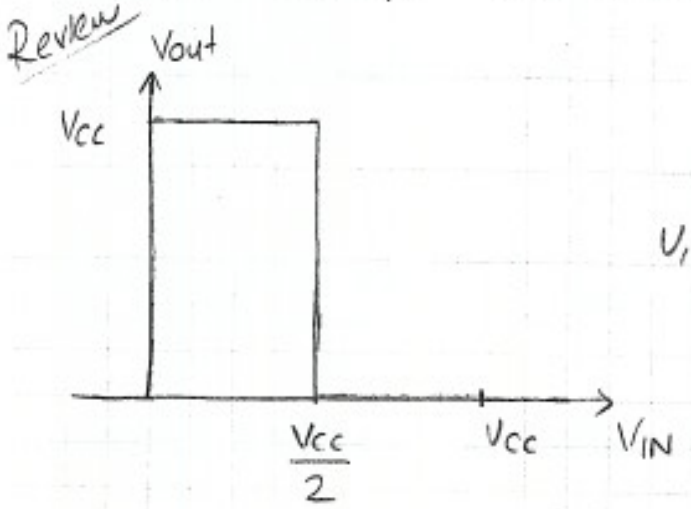
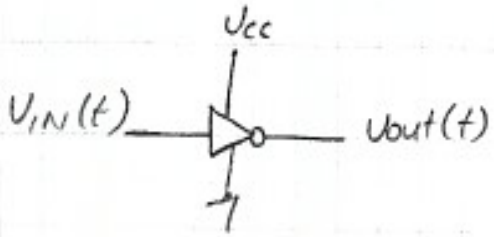
26.03.2010

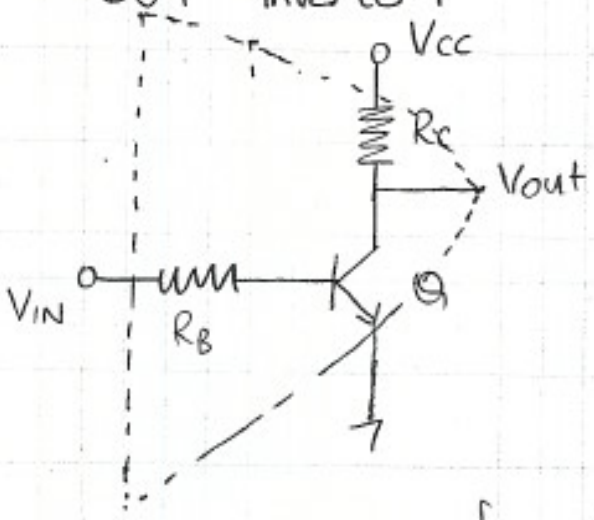
Ideal Transfer Characteristic for Inverter

Review





BJT Inverter:

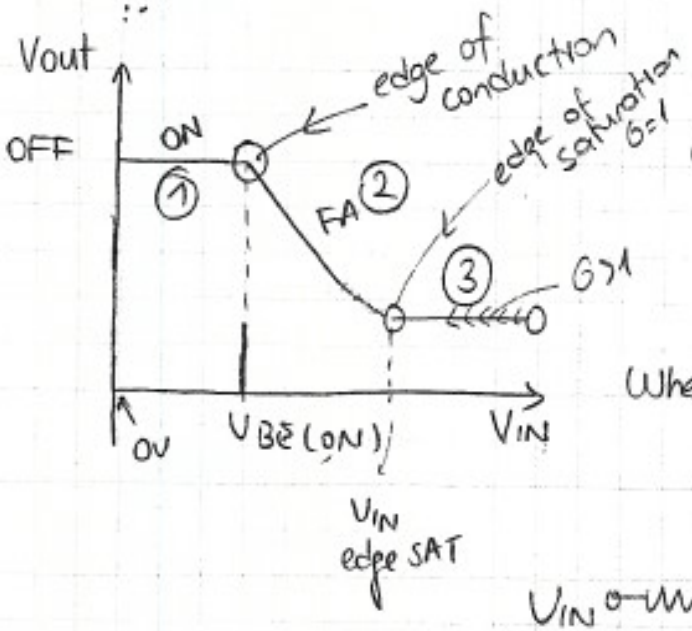


$V_{BE(ON)} = 0.7\,V$

$V_{CE(SAT)} = 0.2\,V$

$V_{BE(SAT)} = 0.8\,V$

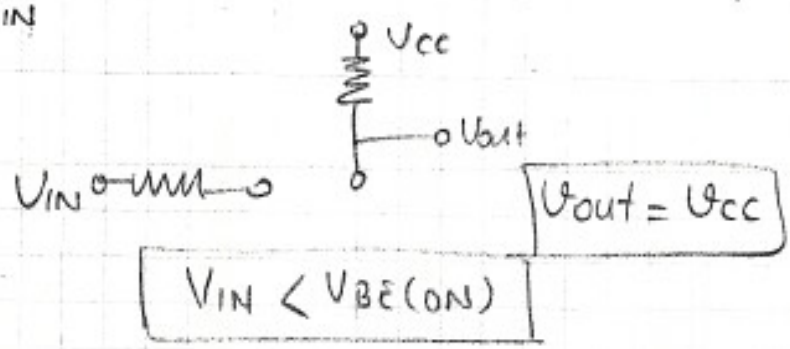
$B_F = 100$



① V_{IN} is small ($V_{IN} \simeq 0$)

↳ Not sufficient to turn Q ON.

When $V_{IN} < V_{BE(ON)}$ → Q: OFF



$V_{out} = V_{cc}$

$V_{IN} < V_{BE(ON)}$

(2) Transistor turns ON when $V_{IN} > V_{BE(ON)}$

Assume transistor is Just ON.

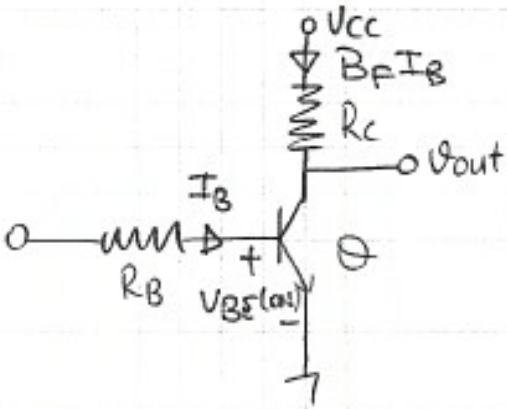
→ $V_{IN} = V_{BE(ON)}$

then if V_{IN} is increased a little bit more

→ $V_{IN} = V_{BE(ON)} + \epsilon$ → $(\epsilon > 0)$

→ Q moves into FA mode.

Then in FA mode



$V_{out} = V_{CC} - (B_F I_B) R_C$; $I_B = 0 \rightarrow V_{out} = V_{CC}$

$I_B > 0 \rightarrow$ Vout decreasing linearly wrt I_B

$\uparrow$

$\frac{V_{IN} - V_{BE(ON)}}{R_B}$

(3) Assume input is large. So large that Q in SAT. Assume SAT and find V_{IN} so that SAT mode is guaranteed.

→D

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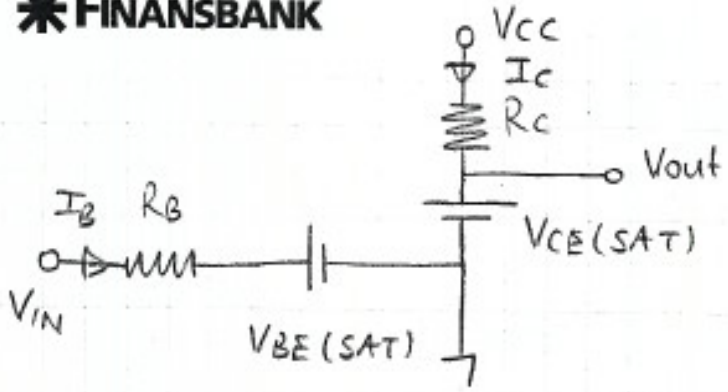


$$I_B = \frac{V_{IN} - V_{BE(SAT)}}{R_B} \qquad I_C = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$$

Condition for SAT

$\beta_F I_B > I_C$ or $G = \frac{\beta_F I_B}{I_C} > 1$ ← saturation parameter

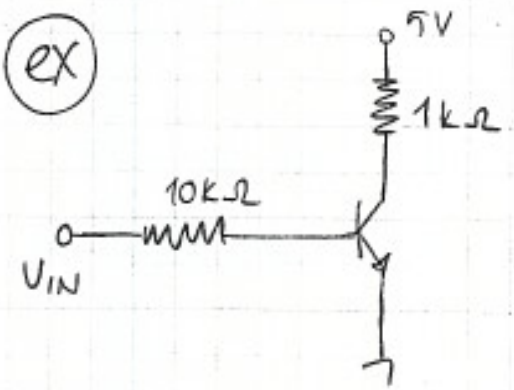
$$G = \frac{\frac{\beta_F}{R_B}(V_{IN} - V_{BE(SAT)})}{\frac{1}{R_C}(V_{CC} - V_{CE(SAT)})} \rightarrow G = 1 \text{ Edge of Saturation}$$

$G = 1 \rightarrow$

$$V_{IN} = \frac{V_{CC} - V_{CE(SAT)}}{R_C} \cdot \frac{R_B}{\beta_F} + V_{BE(SAT)}$$

Edge SAT

(ex)

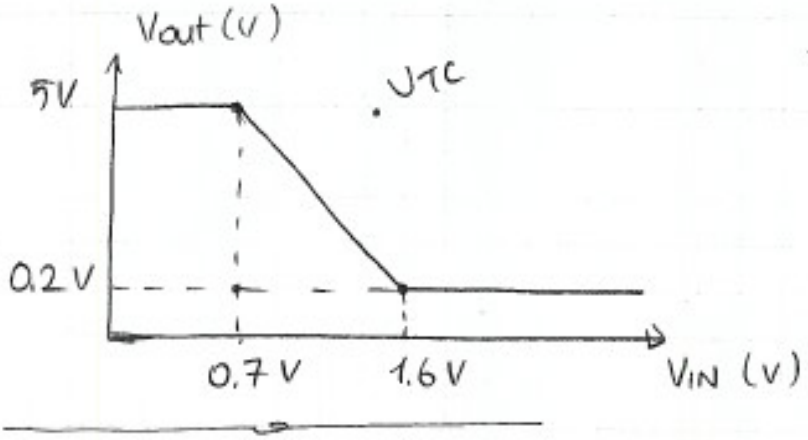


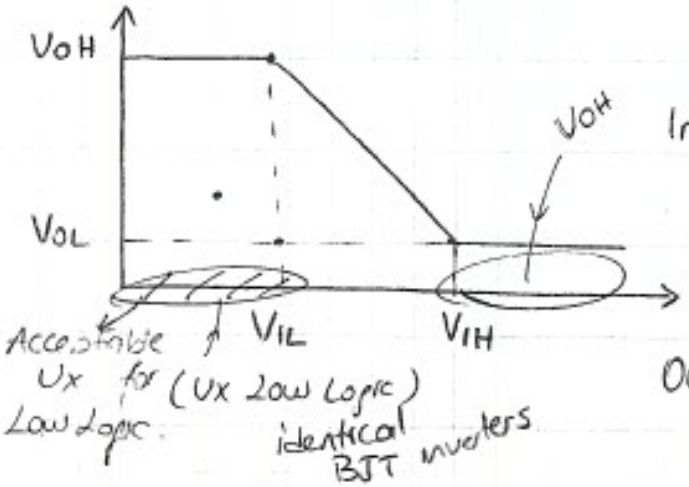
$\beta_F = 100$

$V_{BE(ON)} = 0,7\ V;$

$V_{CE(SAT)} = 0.2\ V$

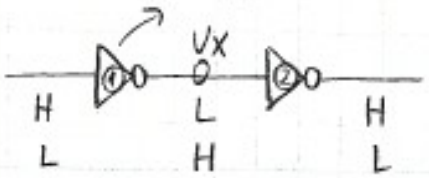
$V_{BE(SAT)} = 0.8\ V$





Input { V_{IL} : Voltage Input Low
V_{IH} : Voltage Input High

Output { V_{OH} : Voltage Output High
V_{OL} : Voltage Output Low



Logic levels & Voltage levels for both inverters should be compatible.

As an example;

output of 1st inverter can be Low, and it should be interpreted as Low logic by the input side of the 2nd inverter. That when $V_x < V_{IL}$; the 2nd inverter interprets V_x as Low Logic level.

Then $V_x = V_{OL}$ at the output of 1st Inverter.

→ $V_{OL} < V_{IL}$

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NML: Noise Margin Low

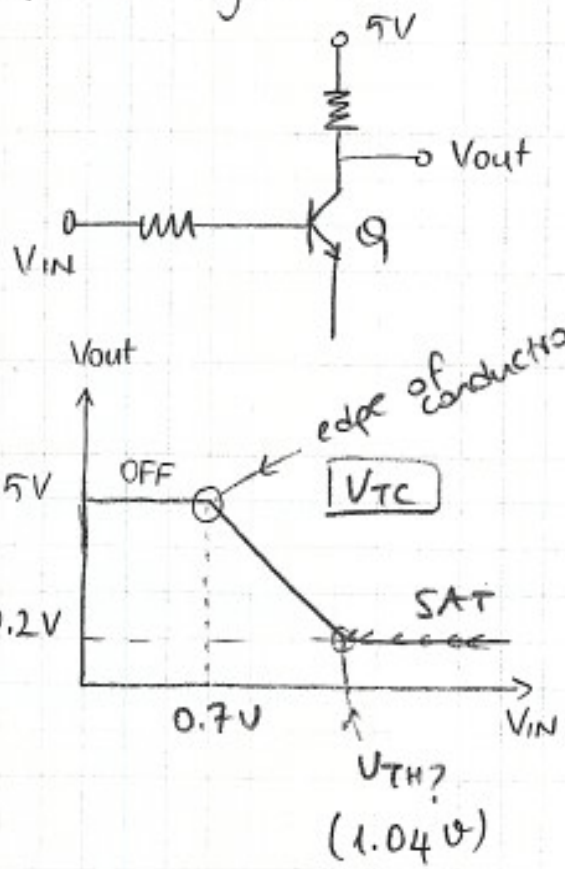
$$NML = V_{IL} - V_{OL}$$

Similarly:

High Logic at V_x output 1 $V_x =$ $V_{OH} > V_{IH}$ (for proper operation)

$$NMH = V_{OH} - V_{IH}$$

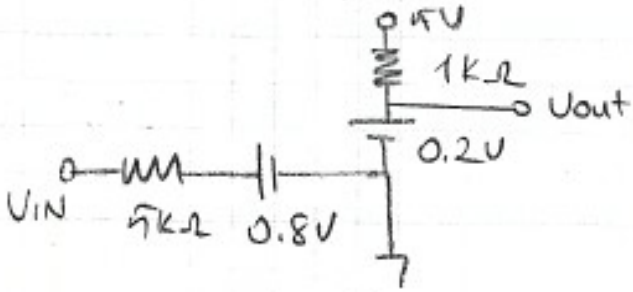
Question again



Find V_{TC}, NMH, NML and average power consumption

U_{TH} : ?

Assume Q : SAT



$I_C = 4.8$ mA

at the edge of saturation

$(\beta = 1) \rightarrow \beta_F I_B = I_C$

$I_B = 4.8mA / 100$

$$V_{IN}\left(\text{at SAT edge}\right) = 0.8 + 5000\, I_B^{\text{SAT edge}}$$

$$= 0.8 + 50.(4.8)$$

$$= 0.8 + 240\ mV$$

$$= 1.04\ V,$$

$$NMH = V_{OH} - V_{IH} = 5 - 1.04$$

$$= 3.06\ V;$$

$$NML = V_{IL} - V_{OL} = 0.7 - 0.2$$

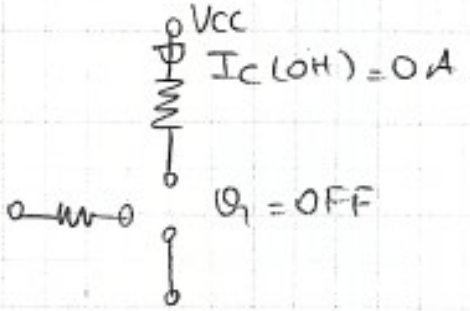
$$= 0.5\ V;$$

AVG Power Consumption :

OH : $P^{OH} = V_{CC}.\, I_{CC}(OH)$

$P^{OH} = 5.0$

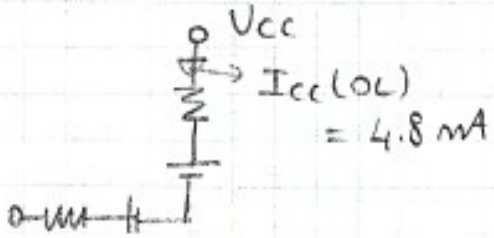
$\therefore$ $\boxed{P^{OH} = 0 \text{ Watts.}}$



OL: $P^{OL} = V_{CC}.\, I_{CC}(OL)$

$P^{OL} = 5.\ (4.8\,mA)$

$\boxed{P^{OL} = 24 \text{ mWatts}}$



$$P^{AVG} = \frac{P^{OH} + P^{OL}}{2} = 12\ mW.$$

30.03.2010

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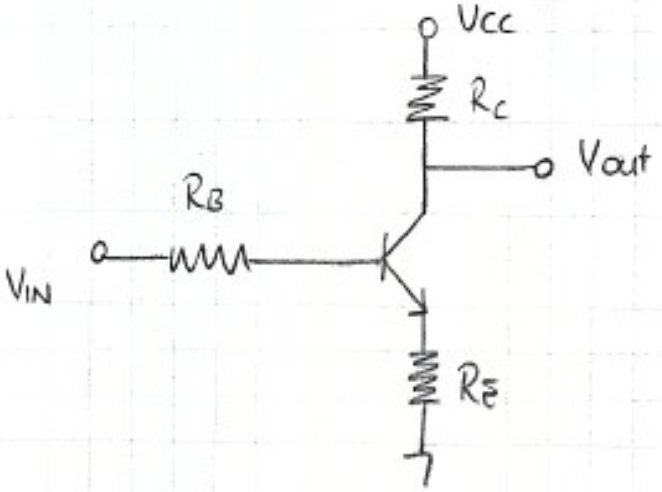
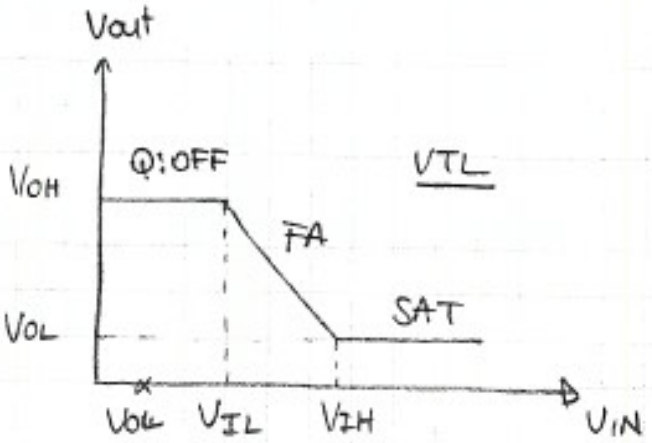
Resistor - Transistor Logic (RTL)



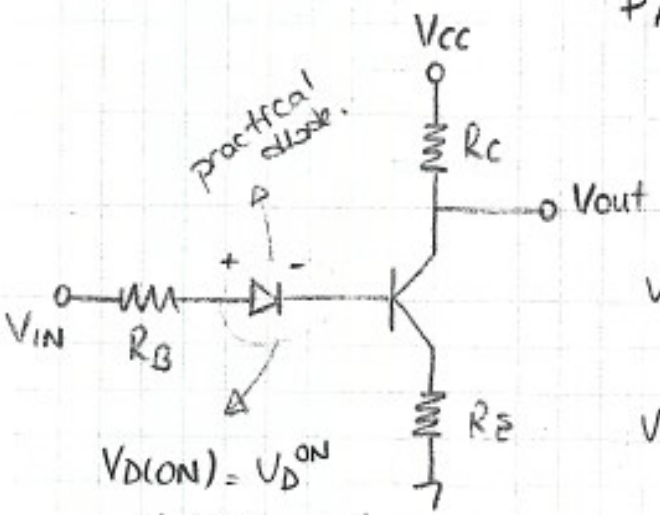


BJT inverter

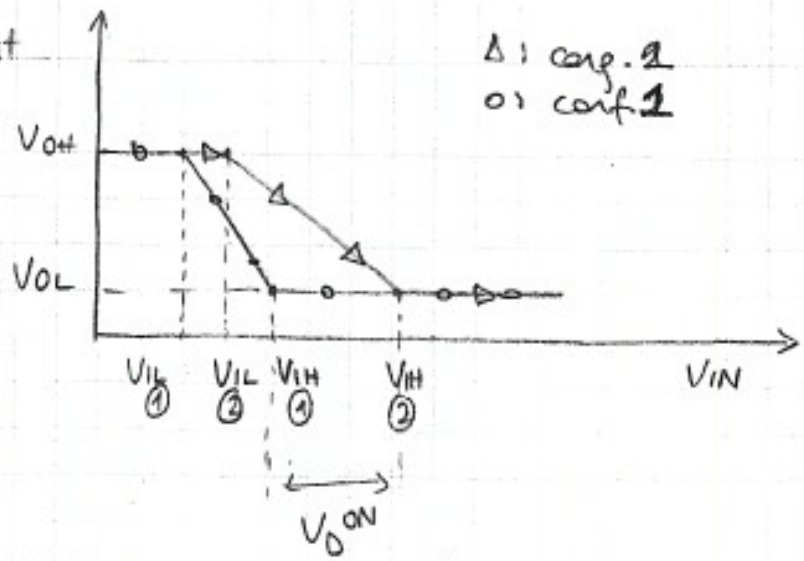
Conf. 1

$V_{OL} < V_{IL}$, $V_{OH} > V_{IH}$ → $NML = V_{IL} - V_{OL} > 0$, $NMH = V_{OH} - V_{IH} > 0$

$$P_{AVG} = \frac{V_{CC} I_{C(OH)} + V_{CC} I_{C(OL)}}{2}$$



Conf. 2



Since there is a dipot, V_B need to pass not only V_{BE} but also V_D. So graph is shifted.

By adding the Level Shift Diode

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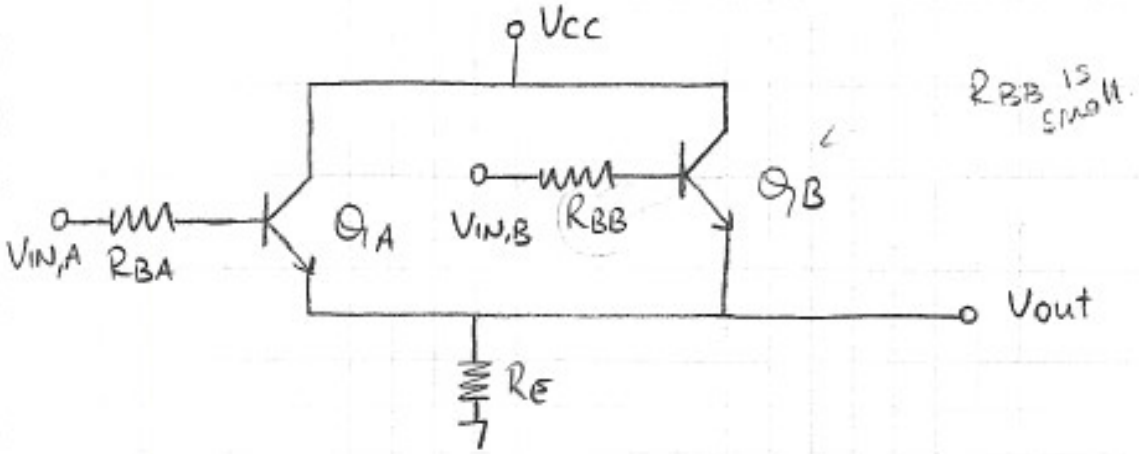
$V_{IL}^{②} = V_{IL}^{①} + V_D^{ON}$; Improves NML

$V_{IH}^{②} = V_{IH}^{①} + V_D^{ON}$; degrades NMH

RTL OR GATE



A	B	Vout	Q_A	Q_B
0(V)	0(V)	0	OFF	OFF
0	Vcc	$V_{CC} - V_{CE(SAT)}$	OFF	SAT
Vcc	0	$V_{CC} - V_{CE(SAT)}$	SAT	OFF
Vcc	Vcc	$V_{CC} - V_{CE(SAT)}$	SAT	SAT

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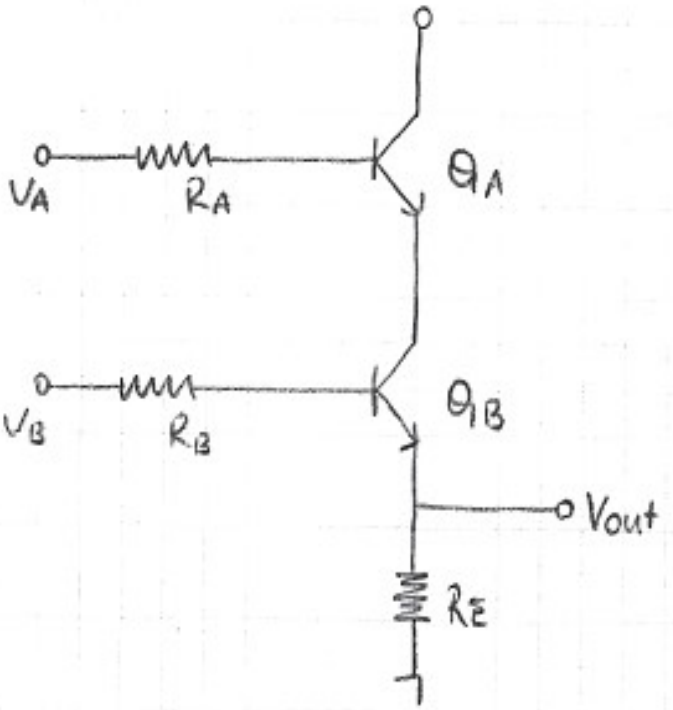
RTL AND GATE



$B_F I_B > I_C$ → SAT

FA: Amplifier

transition

A	B	Vout	Q_A	Q_B
Vcc	Vcc	$V_{CC} - 2V_{CE(SAT)}$	SAT	SAT
0	Vcc	$\neq 0$ (but small when $R_E \ll R_B$)	OFF	SAT
Vcc	0	0	X (floating transistor)	OFF
0	0	0	OFF	OFF

2.04.2010

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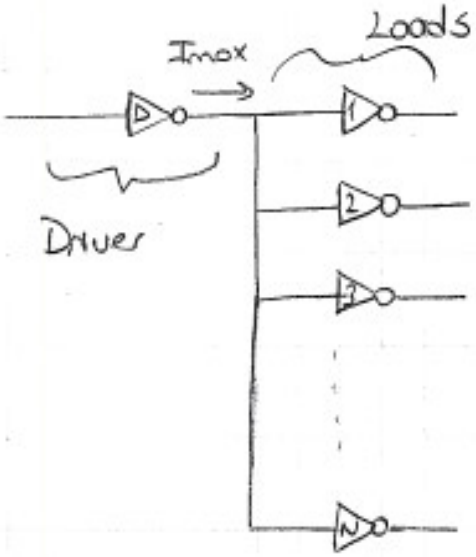
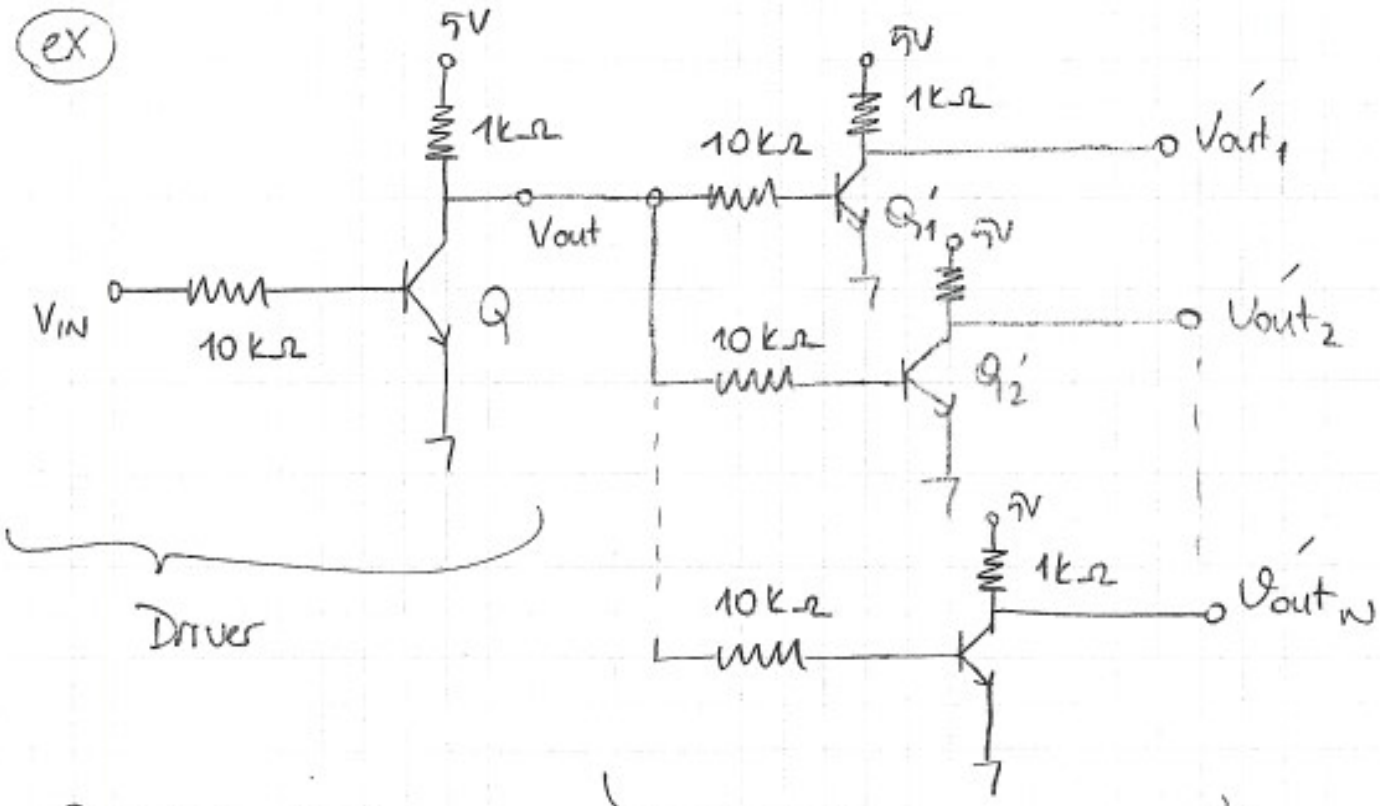
RTL Fan-Out:



Driver gate and N loads

ex



Q: Driving Gate

Q'_k: Load Gate ← Loads

{ Vout, Vout'k }

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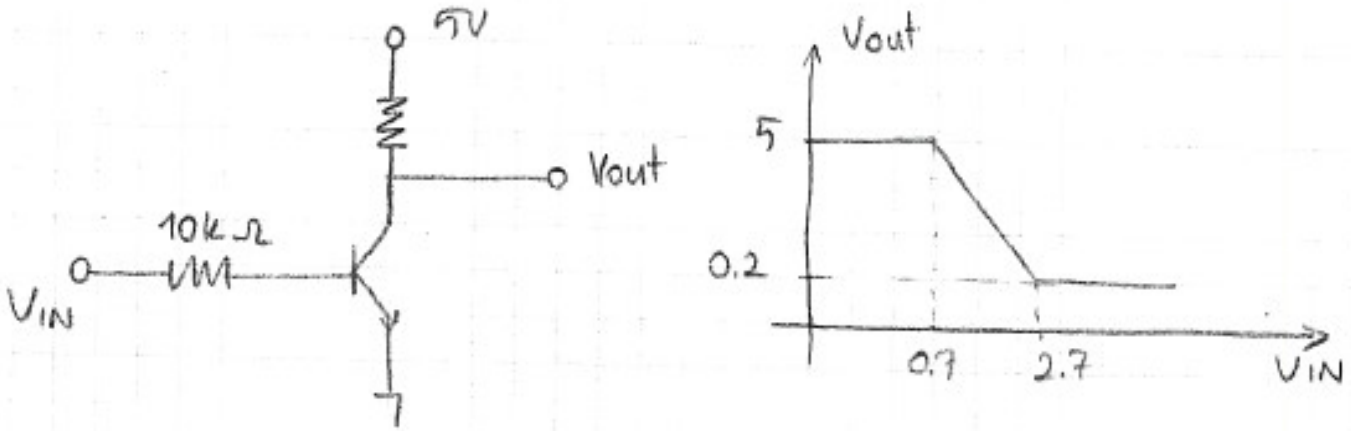
Question: What is the maximum number of inverters that can be connected at the output?

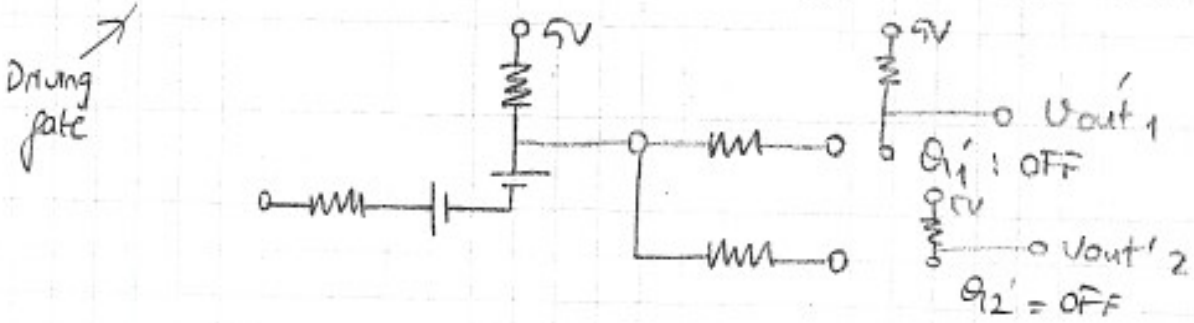


$\beta_F = 25$ $\quad V_{CE(SAT)} = 0.2V$

$V_{BE(ON)} = 0.7V$ $\quad V_{BE(SAT)} = 0.8V$

Fan-out at OL:

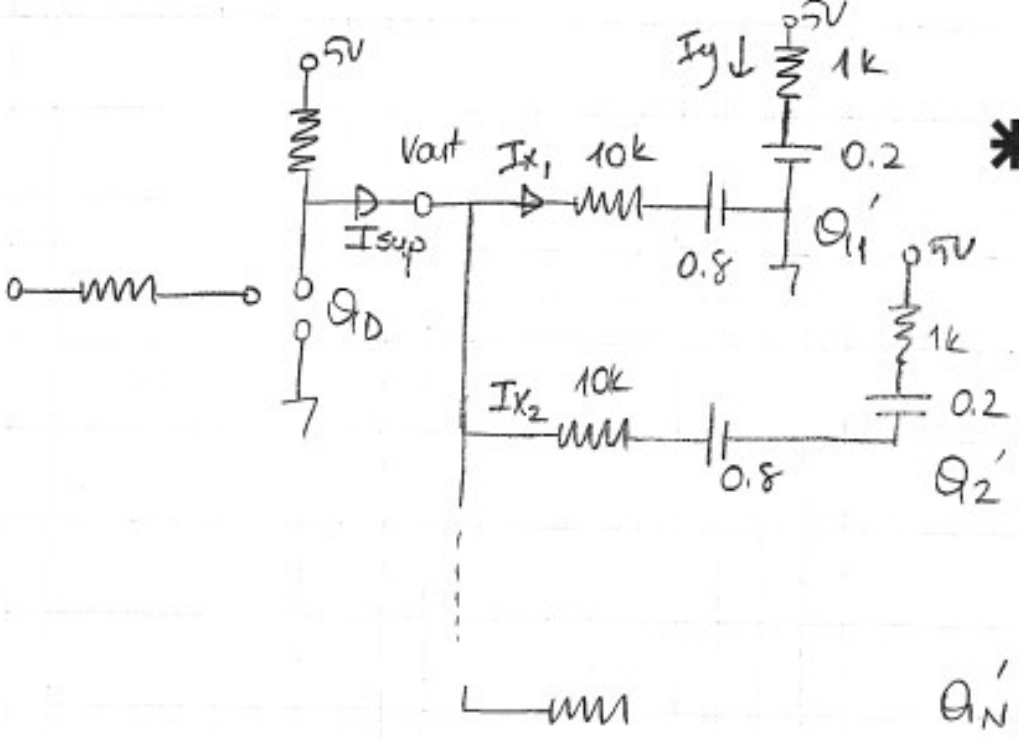
Vout : Low (0.2V) $\rightarrow$ Q_k' are all OFF



At OL then fan-out is infinite.

Fan-out at OH:

Vout : High (Q_1 : OFF ; Q_k' : SAT , $k = \{1, \dots N\}$)



$$I_x = \frac{V_{out} - 0.8}{10}\ mA, \quad I_y = \frac{5 - 0.2}{1}\ mA \quad (4.8)$$

$$25 \rightarrow \beta_F I_x > I_y \Rightarrow I_x > 0.192\ mA$$

So when $V_{out}^{Driver} >> 2.7\ V \rightarrow Q_1'$ saturates. (Look Graph)

$$I_{x_1} = \frac{V_{out} - 0.8}{10} \geq \frac{2.7 - 0.8}{10} = 0.19\ mA$$

To saturate $Q_1', Q_2', \ldots Q_N'$ together,

$$\boxed{I_{sup} \geq (0.19).N\ mA}$$

For proper operation of Driver Gate

$$V_{OH}^{Driver}(N\ loads) \geq V_{IH} \leftarrow 2.7$$

$$V_{OH}^{Driver}(N\ Loads) = 2.7\ V;$$

$$I_{sup} = \frac{5 - 2.7}{1k\Omega} = 2.3\ mA \quad (\text{calculated from Driver})$$

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$I_{sup}^{Driver} = 2.3\ mA \geq N(0.19)\ mA$

$N \leq 12$

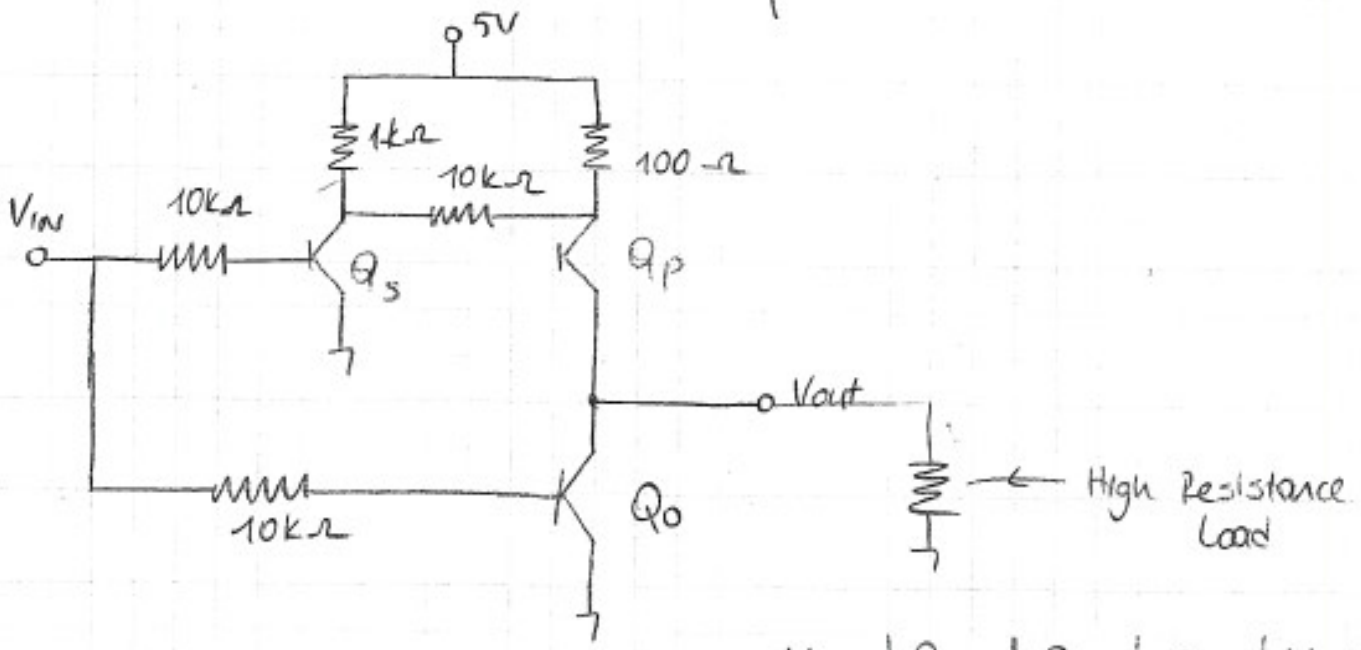
Fan-out at OH is 12.

Fan-out of the gate

= min (Fan-out $_{OH}$, Fan-Out $_{OL}$)

= 12

RTL with Active Pull-up:

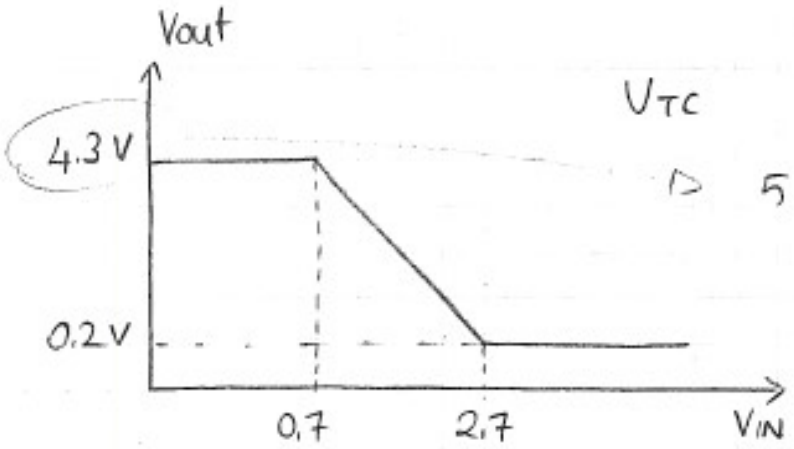


Q_T: Saturating transistor

Q_p: Pull-up transistor

Q_o: Output transistor

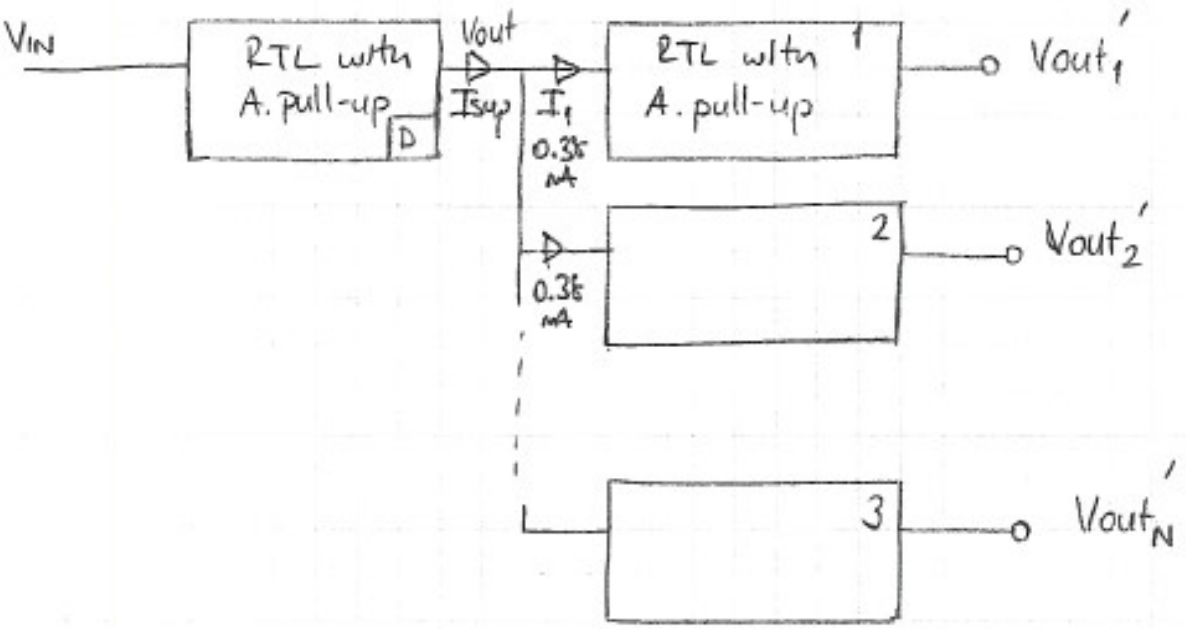
V_{IN}	Q_s	Q_o	Q_p	Vout
Low	OFF	OFF	ON	High
High	SAT	SAT	OFF	Low



V_{TC}

▷ $5 - 0.7 = 4.3$ V;

Fan-Out Calculation



① Vout : Low ; ⟶ All loads have Q_S, Q_D : OFF

↙

$Fan\text{-}out_{OL} = \infty$ ← No effect on Driving Gate

② Vout : High ; $Vout > \underbrace{2.7\ V}_{V_{IH}}$

$$\left[\begin{array}{c} V_{OH} > V_{IH} \text{ for proper op.} \\ NM_H = V_{OH} - V_{IH} > 0 \end{array}\right]$$

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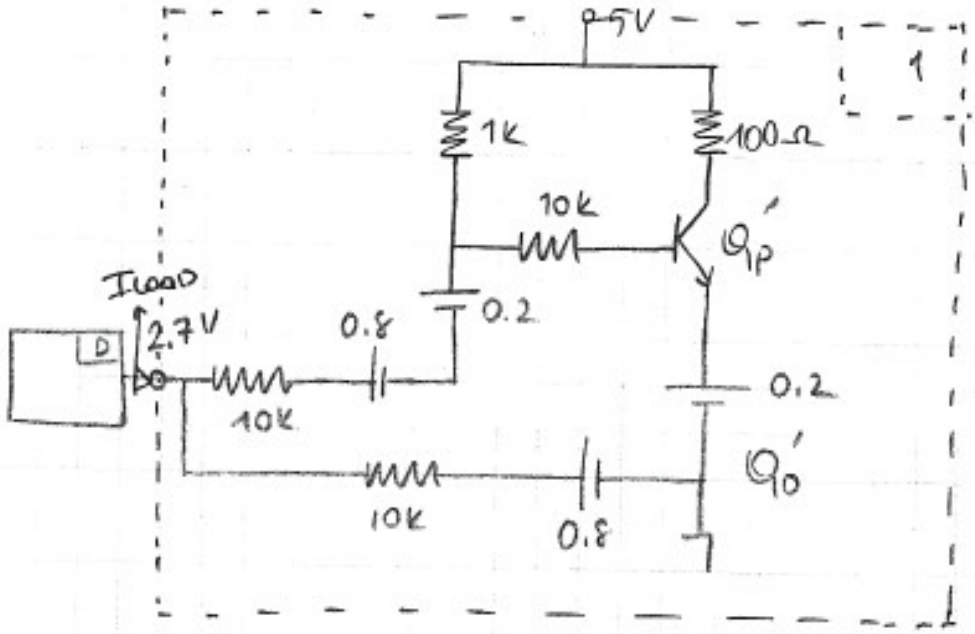
Assume $V_{out} = 2.7\ V$;

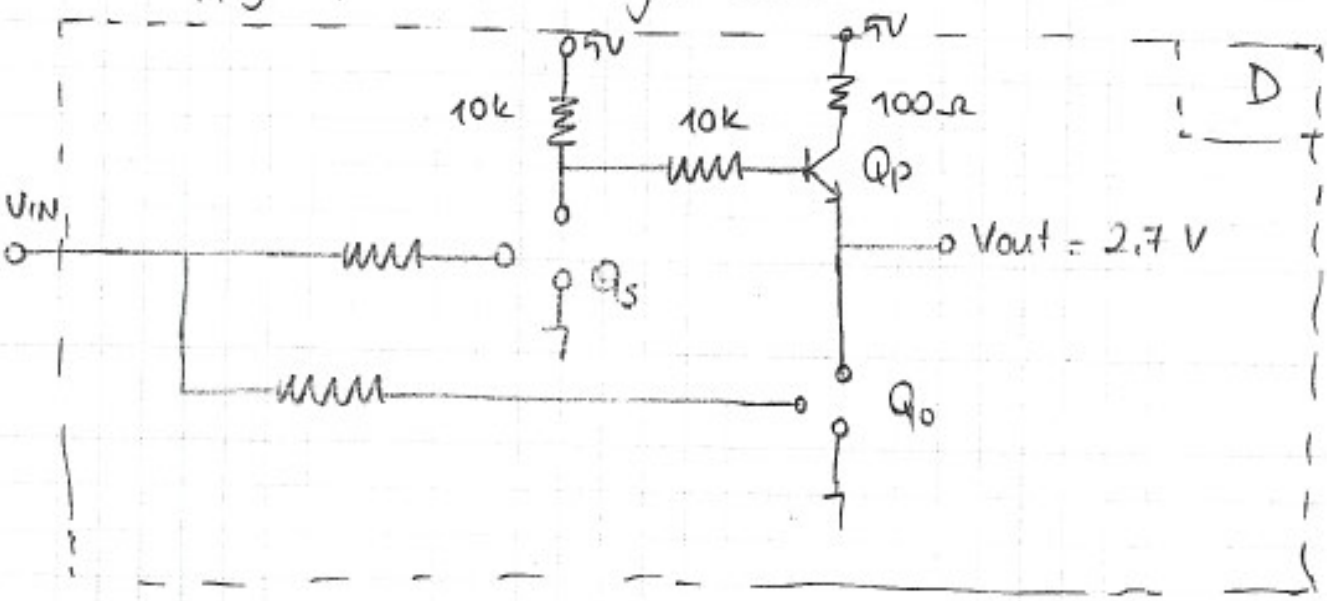


$$I_{LOAD} = \left(\frac{2.7 - 0.8}{10}\right) \cdot 2\ mA$$

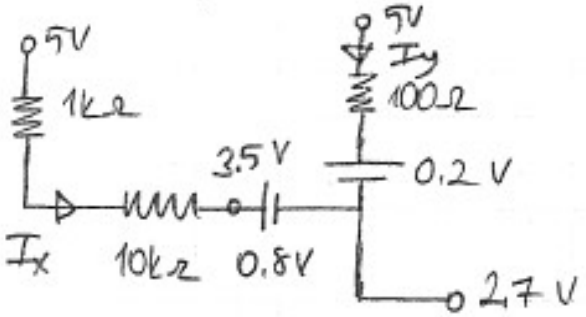
$$= 0.38\ mA$$

Assuming N Loads $\longrightarrow$ $I_{sup} \geq N.(0.38)mA$

Let's find the maximum amount of current that driver can supply for Vout : High Case.



Assume Q_p in SAT :



$$I_x = \left(\frac{5-3.5}{1}\right) mA = 0.136\ mA$$

$$I_y = \left(\frac{5-2.9}{100}\right) = 21\ mA$$

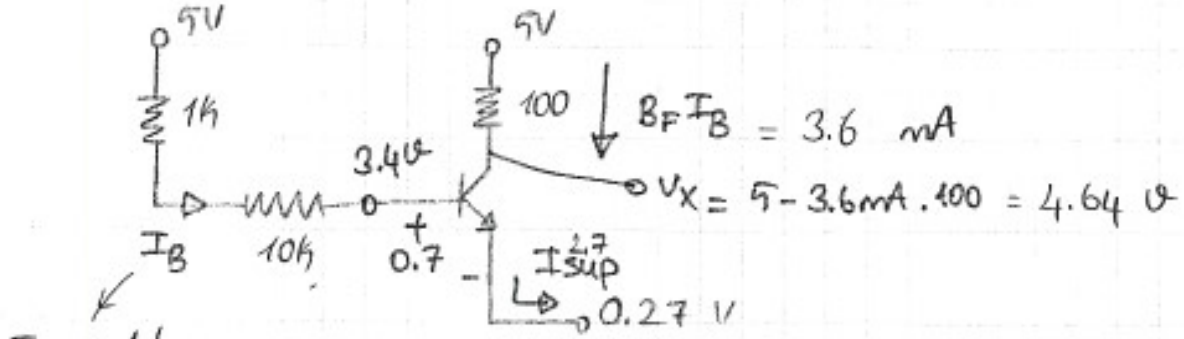
check ☺

$\beta_F I_x > I_y$?

$(25)(0.136) \gtrless 21$ ✗

NOT SAT ☺

Assume Q_p in FA :



$$I_B = \frac{1.6}{10k}$$

$= 0.145\ mA$

$I_E = I_{sup}^{2.7} = 3.6 + 0.145$

$= 3.745\ mA$

check FA ☺

① $I_B > 0$ ✓

② $V_{BC} < 0.7$

$3.4 - 4.64 < 0.7$ ✓

$$I_{sup}^{2.7} = 3.745\ mA$$

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So, for proper op.

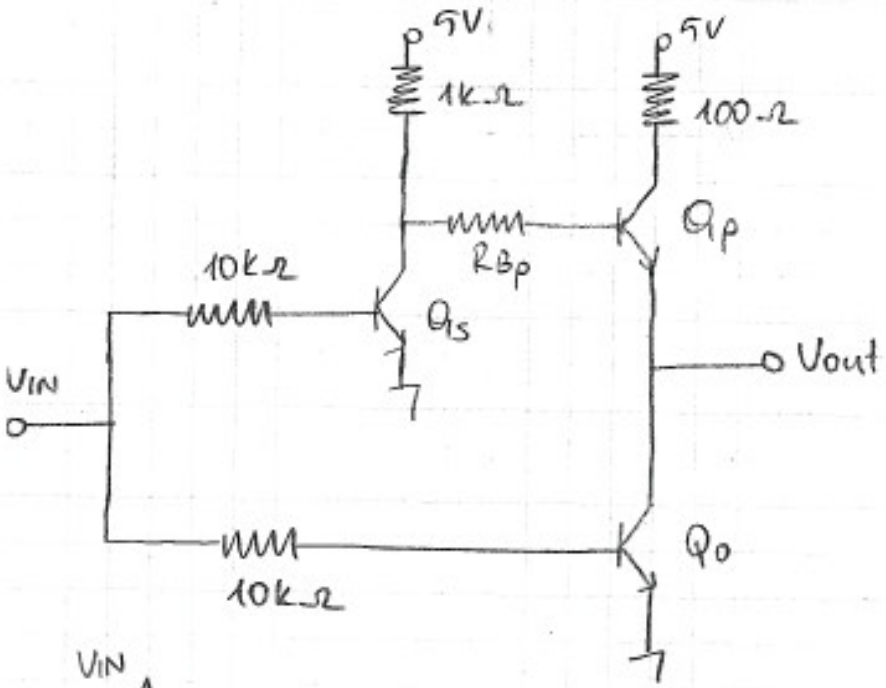
$I_{sup} \geq N.\ (0.38)\,mA$

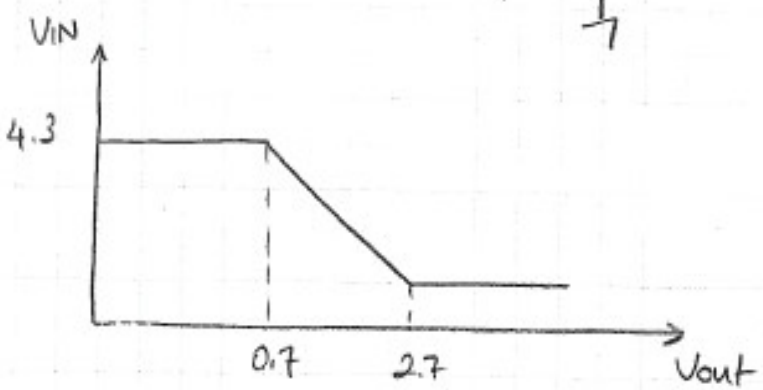
$$N_{OH} = \frac{3.75}{0.38} = 9$$

Fan-out with this system $\min(N_{OL}, N_{OH}) = 9$.

6.04.2010

RTL with active pull-up:





(a) $R_{BP} = 10\ K\Omega \longrightarrow$ Fan-out = 9

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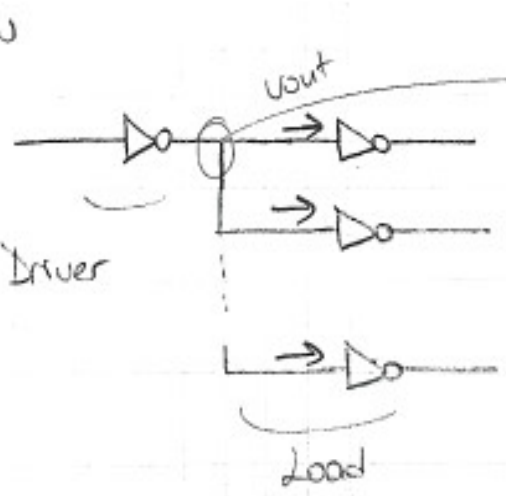
Review

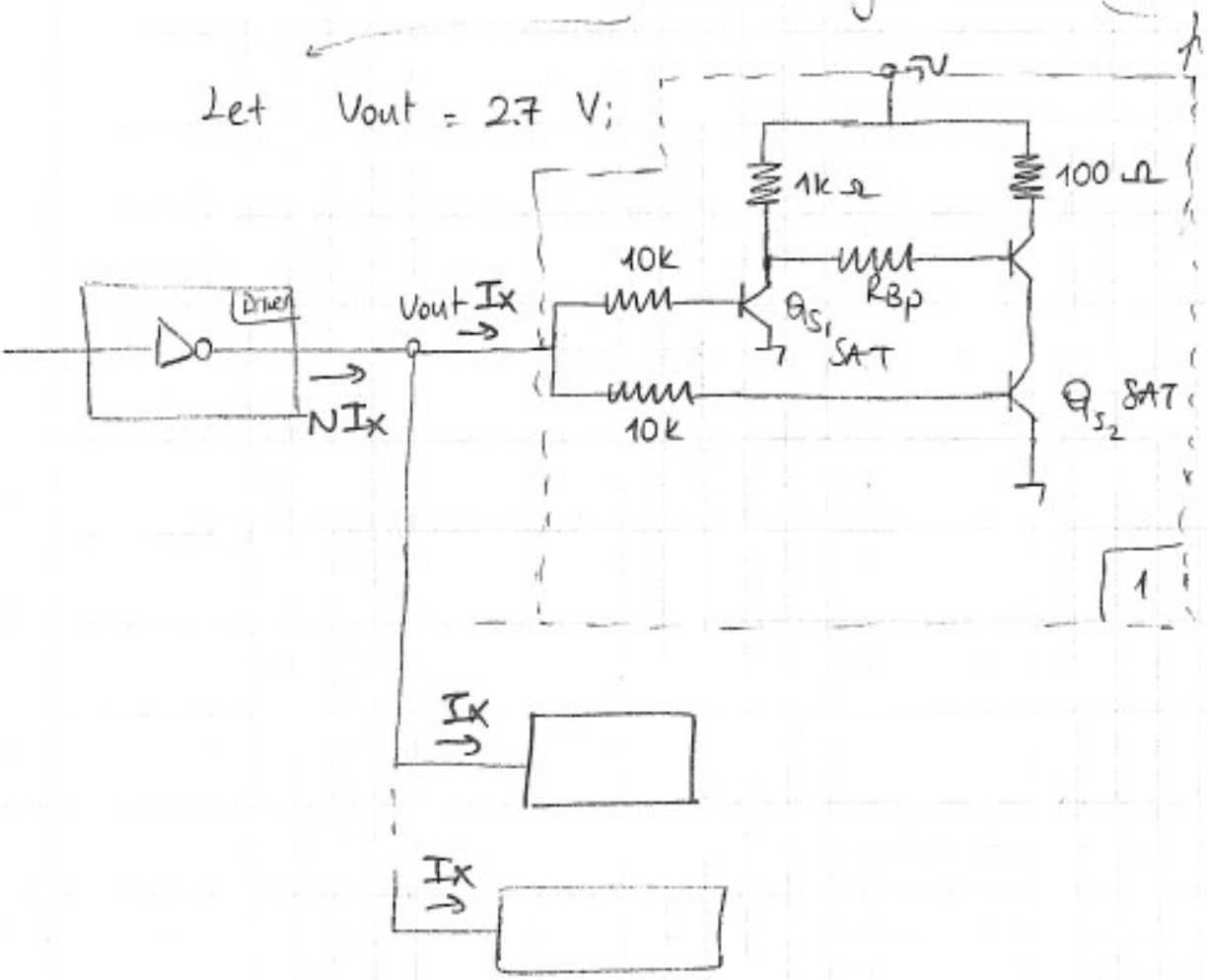


① Vout ≠ Low → All load inverters have Q_S, Q_D is OFF mode ∴

Fan-out (OL) = ∞

② Vout => High (Vout > 2.7 V)

Let Vout = 2.7 V;



$$I_x = \left(\frac{2.7 - 0.8}{10\,k}\right) \cdot 2$$

$$= 0.38\ mA$$

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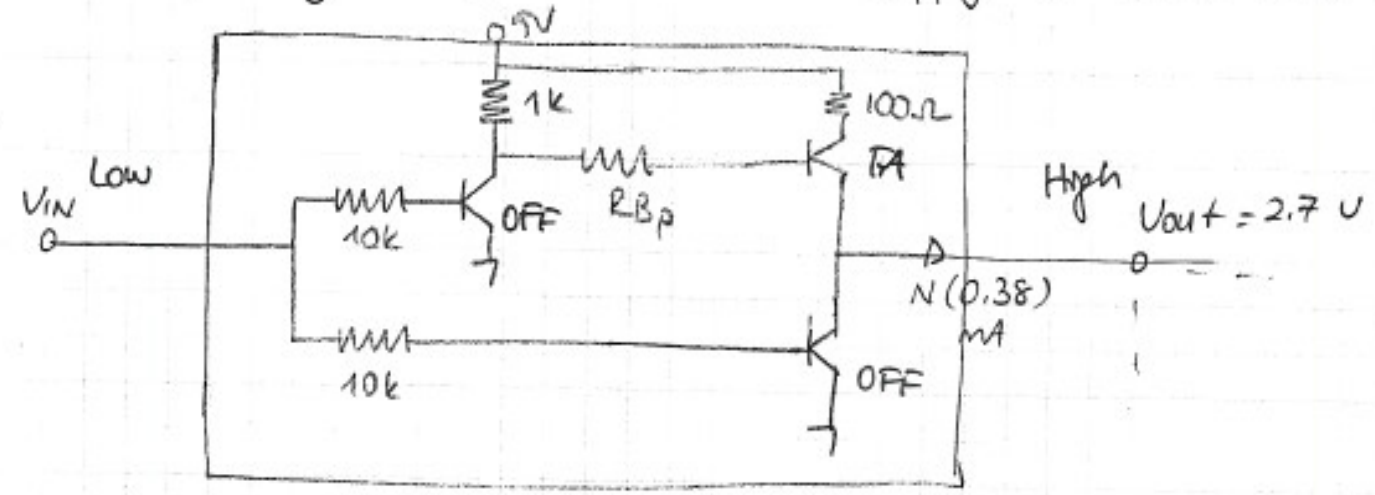
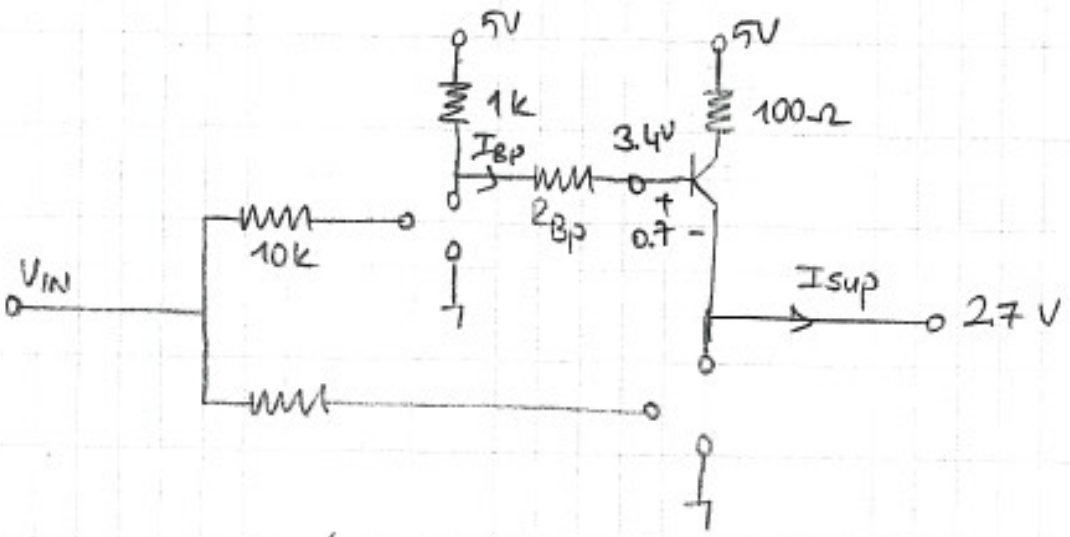
(b) Set R_{BP} such that Fan-out is 50. Assuming N loads for any R_{BP}, Driver should supply at least NI_X A.





$$I_{BP} = \frac{(5 - 3.4)}{(1 + R_{BP})} \text{ mA} \quad ;$$

$$I_{sup} = I_E = (\beta + 1) I_{BP} = 26 \cdot \left(\frac{1.6}{1 + R_{BP}} \right) \text{mA}$$

26

To have fan-out 50:

$$I_{sup} \geq 50 \cdot (0.38)$$

$$\boxed{I_{sup} \geq 19 \text{ mA}}$$

$$R_{Bp} \leq \frac{26.(1.6)}{19} - 1$$

$$R_{Bp} \leq 1.2\ k\Omega$$

Check FA:

$$V_{BC} = 3.4 - (5 - I_{cp}.100)$$
$$\simeq 3.4 - (5 - 19.(0.1))$$
$$\simeq 3.4 - 3.1$$
$$\simeq 0.3$$

9.04.2010

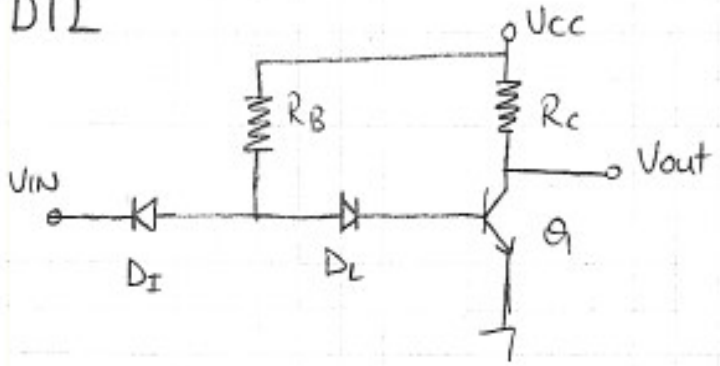
Diode Transistor Logic (DTL):

Problems with RTL

① Low Fan-out ($N_{OL} = \infty$, $N_{OH} \simeq 50$)
↑ given example

② Low Noise-Margins

DTL



$V_{BE(ON)} = 0.7\ V$

$V_{BC(ON)} = 0.7\ V$

$V_{CE(SAT)} = 0.2\ V$

$V_{BE(SAT)} = 0.8\ V$

$V_{DIODE(ON)} = 0.7\ V$

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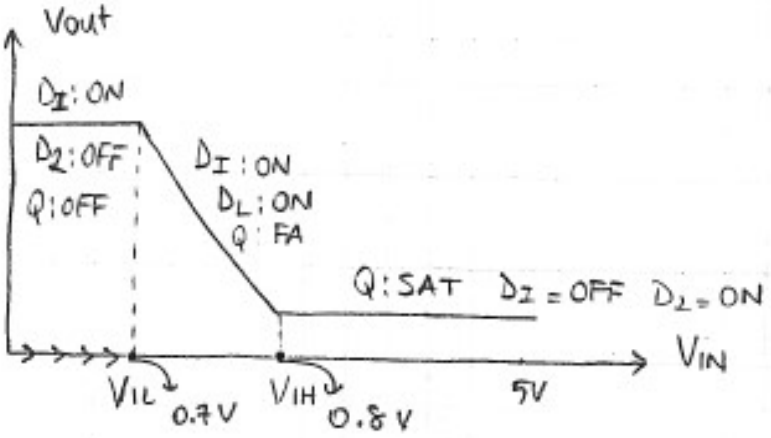
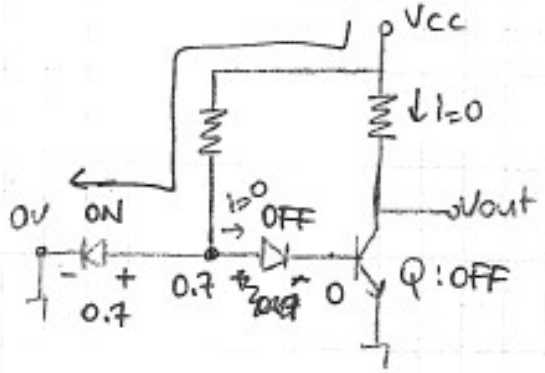
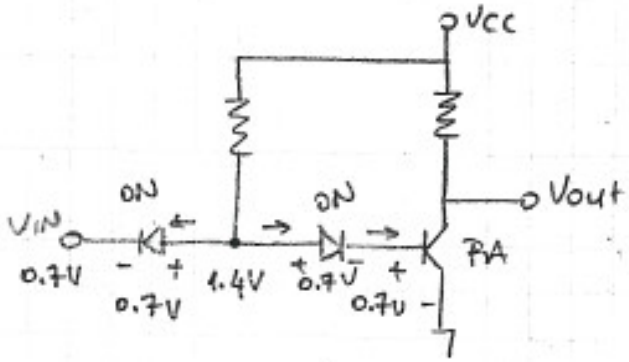


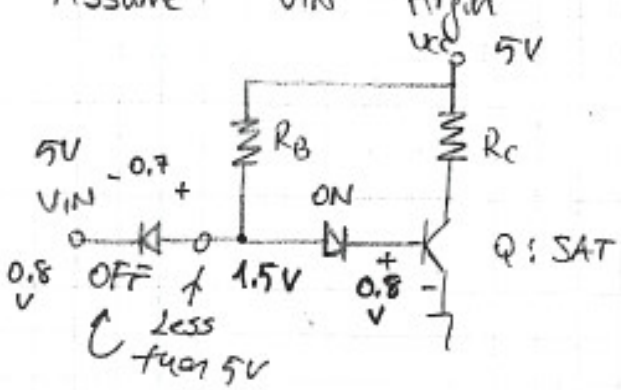
Assume V_{IN} : Low



Assume $V_{IN} = 0.7$ V



Assume V_{IN} High



$V_{IH} = 0.8$ V → SAT

Revisiting RTL Problems for DTL Circuits

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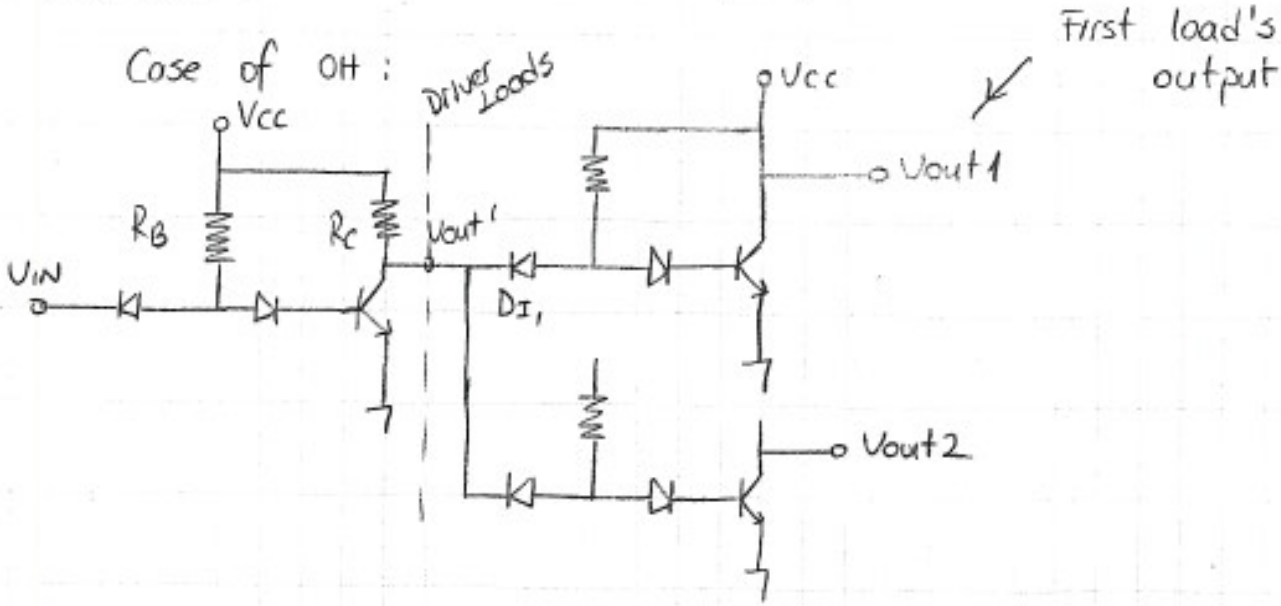
① Fan-out :



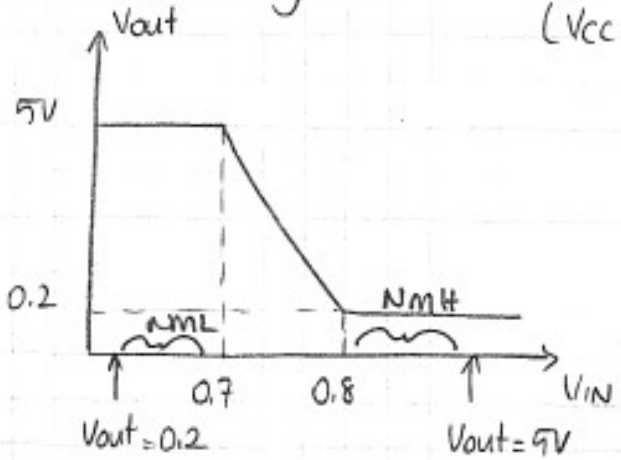
When Vout : OH

D_I's of load Transistors are OFF. Then $N_{OH} = \infty$

(DTL has N_{OL} limitations)

(Analysis of OL fan-out will be given later)

② Noise Margins :



$N_{ML} = 0.7 - 0.2 = 0.5\,V$

$N_{MH} = 5 - 0.8 = 4.2\,V$

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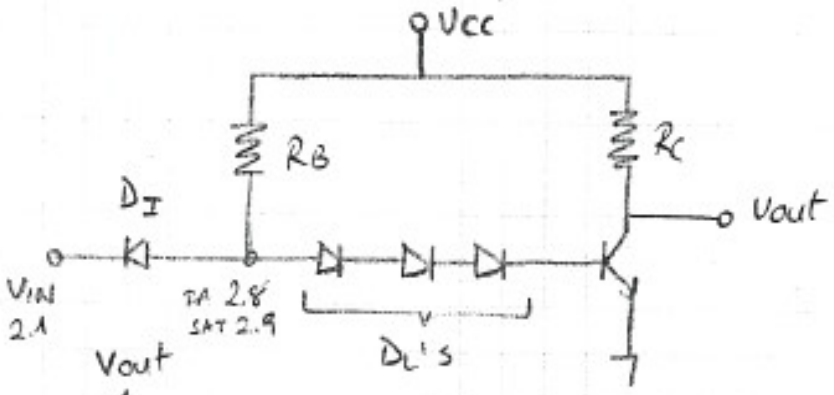
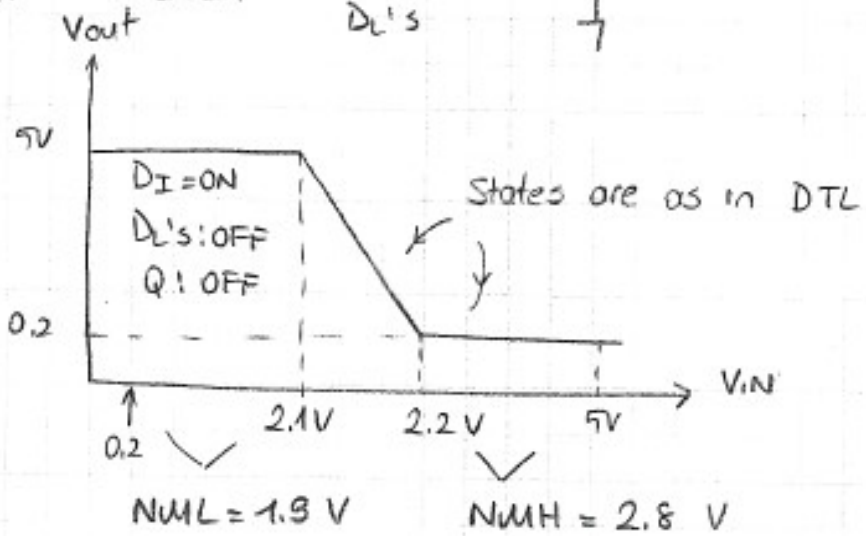
Improving DTL NML!

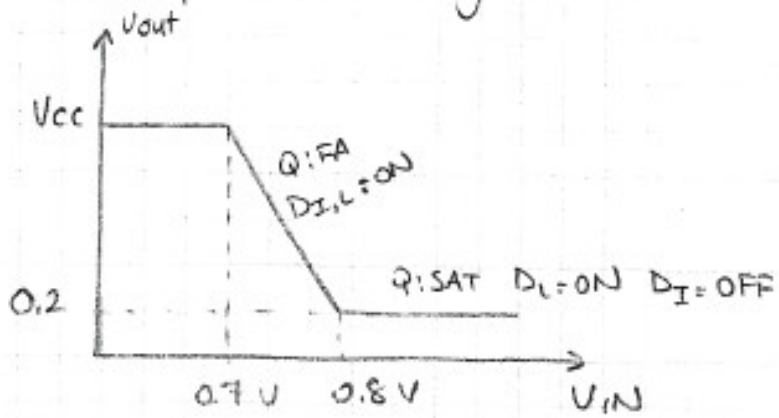


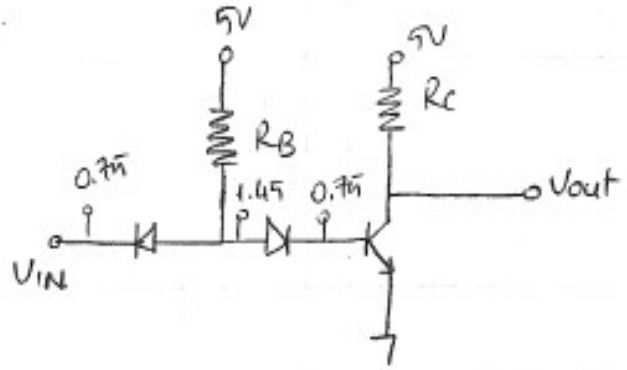


On the VTC of DTL!

DTL has the following problem which is due to simplistic modeling of the BJT transistor.

VTC of DTL is given as



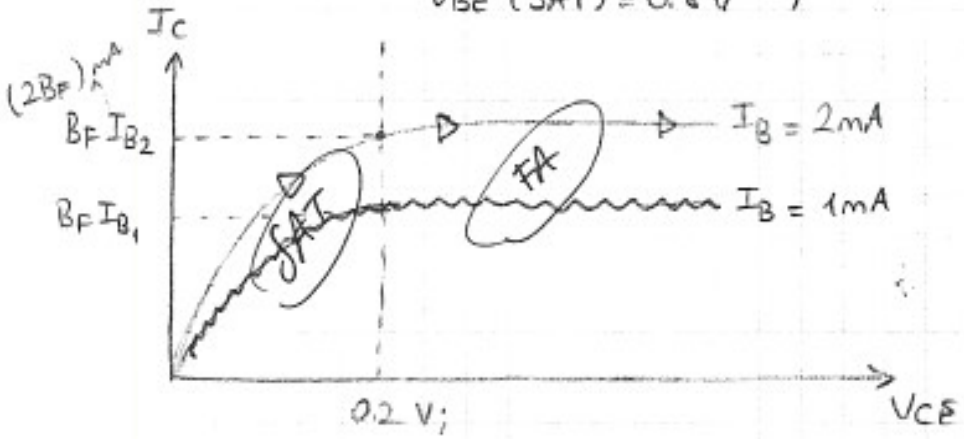


"Problem" $V_{out} = ?$ when $V_{IN} = 0.7\ V$;

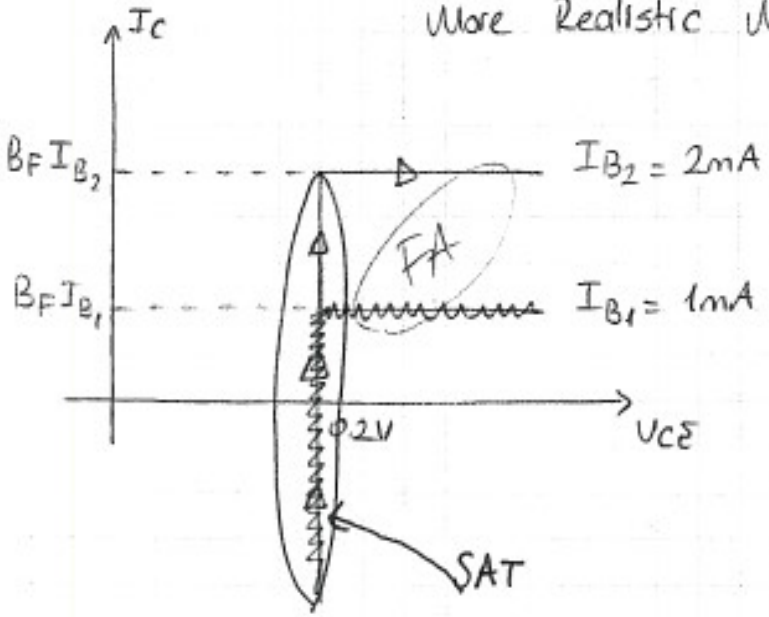
$V_{BE} = 0.7\ V$;

$V_{BE(FA)} = 0.7\ V$

$V_{BE(SAT)} = 0.8\ V$ } Simple Model



"More Realistic Model"



Simplistic Model

SAT → $V_{CE(SAT)} = 0.2\ V$

$B_F I_C > I_C$

FA → $I_C = B_F I_B$

$I_B > 0$

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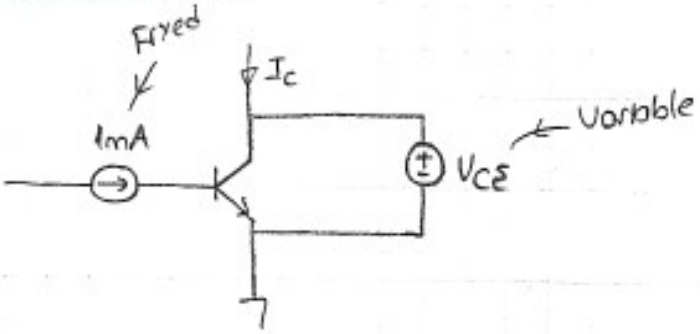
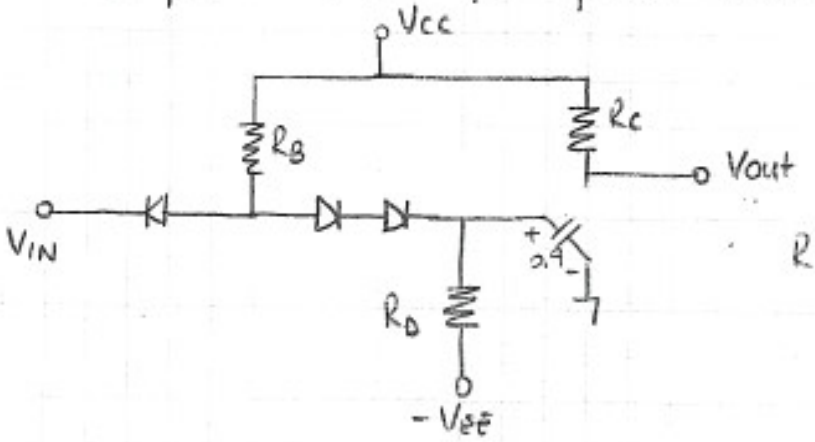
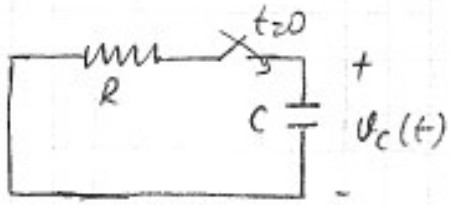


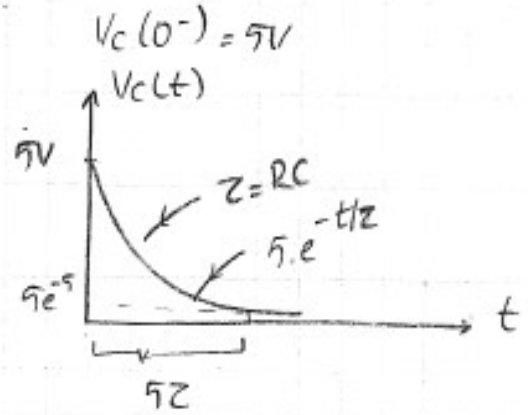
Modified DTL for fever switching:



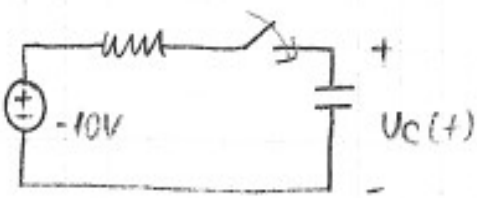
R_D: Discharge resistor



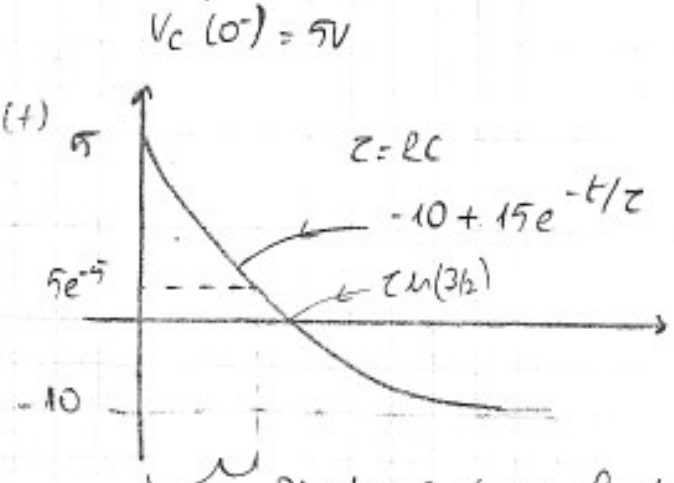
C_1:



C_1: I need to wait (5RC) to discharge the cap.



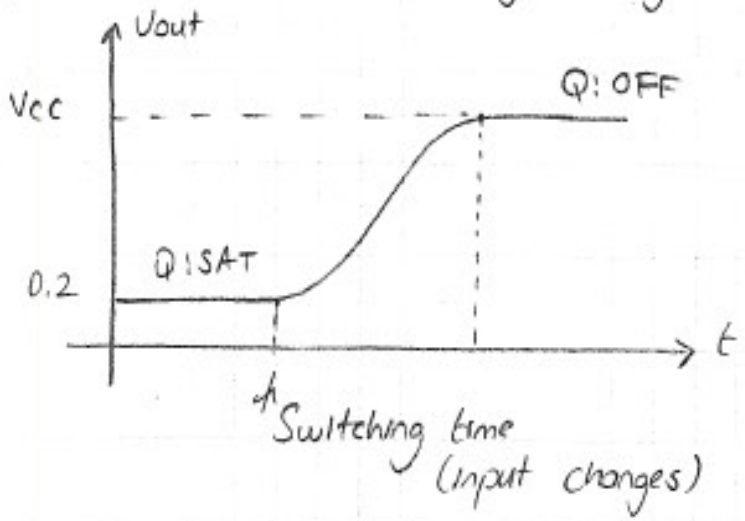
C_2:



C_2 has a smaller discharge time ←

Discharge time for the capacitor for C_2

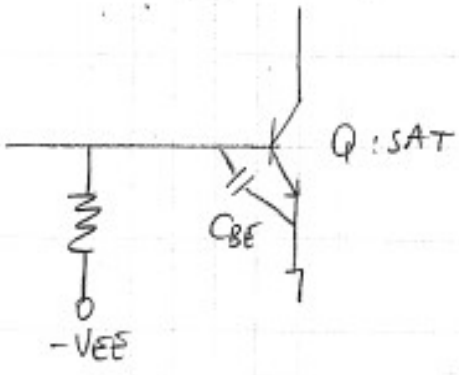
Assume Q is in SAT (Output: Low); there is a change in Input and Input becomes Low, then output should increase gradually to High



Q: How fast you can turn off the Q?

When Q is is SAT, $V_{BE(SAT)} = 0.8\ V$ implies that capacitors over BE junction are fully charged.

R_D and $-V_{EE}$ provides a path for the fast discharge of BE junction capacitor. (Note without R_D C_{BE} cannot discharge according to the idealized component models!)



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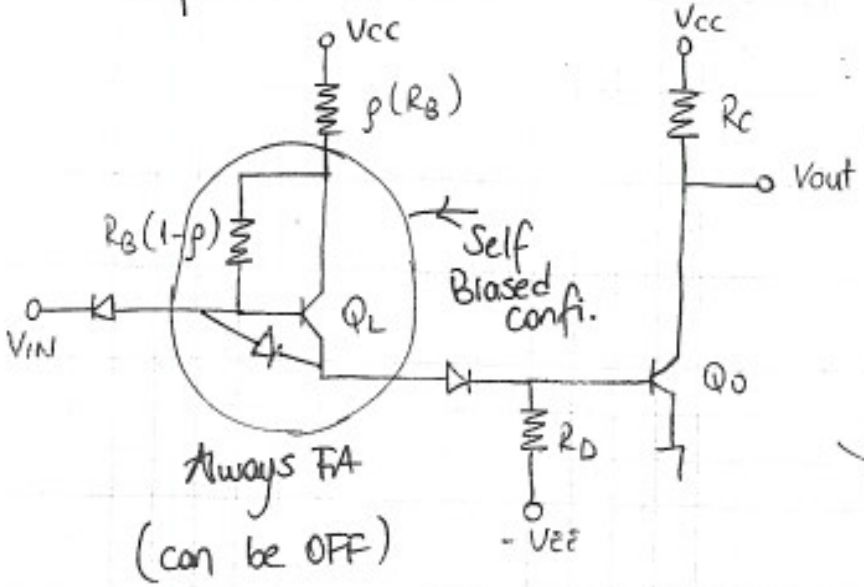
20.04.2010

Improved DTL



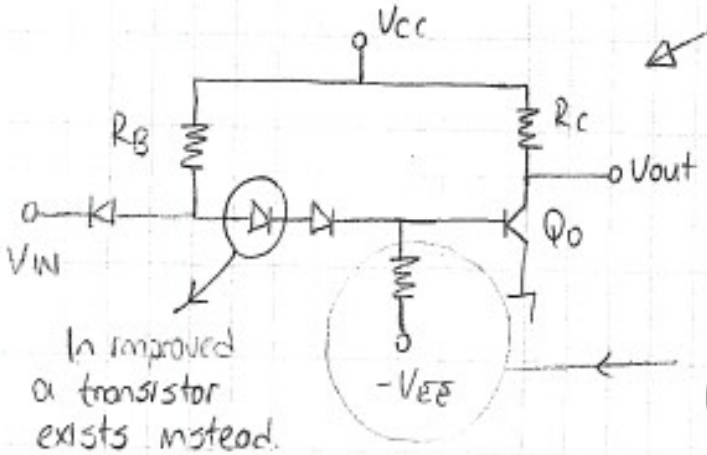
(*)

VIN → high : FA

VIN → low : OFF

$0 < \rho < 1$

improved DTL



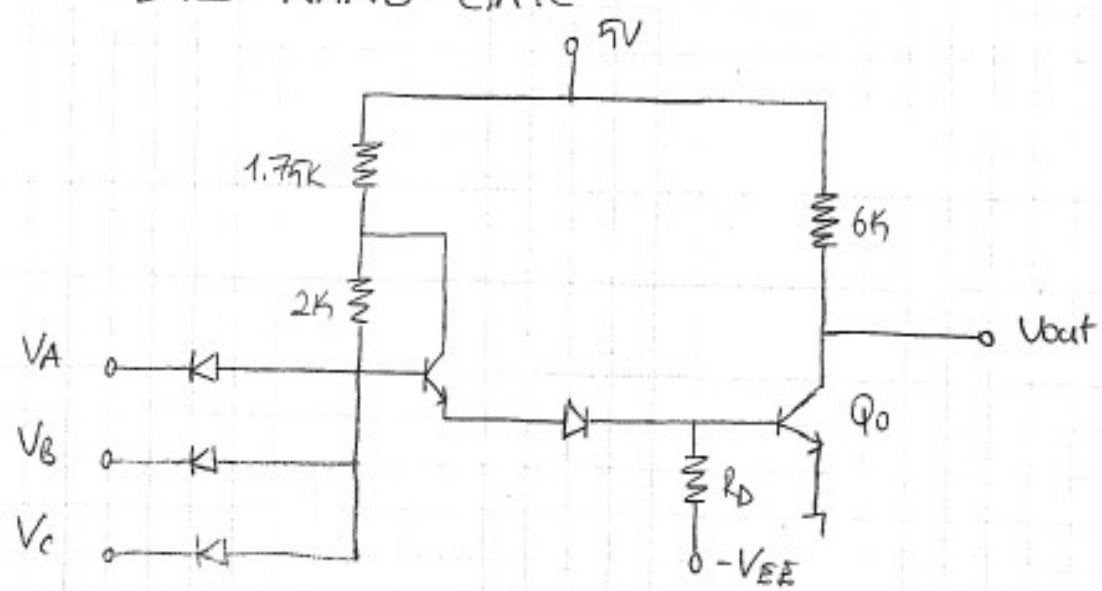
Standard DTL

In improved a transistor exists instead.

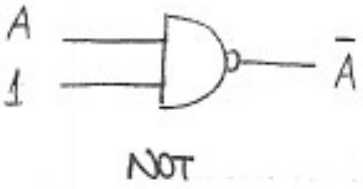
faster discharge

(does not improve VTC characteristics)

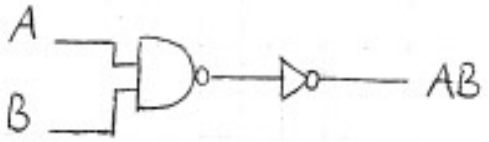
DTL NAND GATE



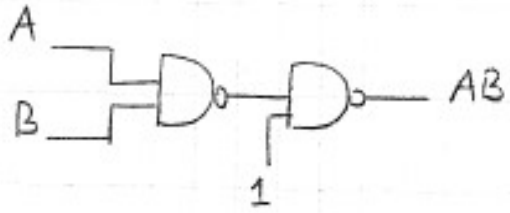
NAND GATES

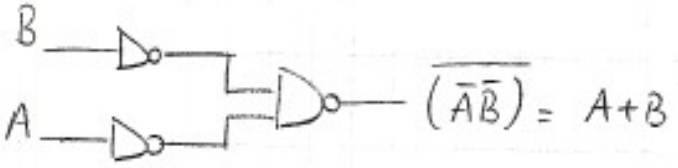


NOT



AND

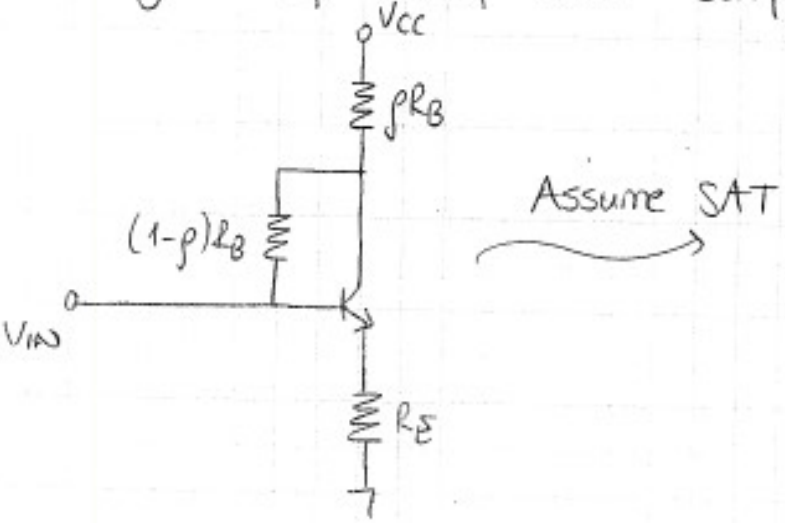




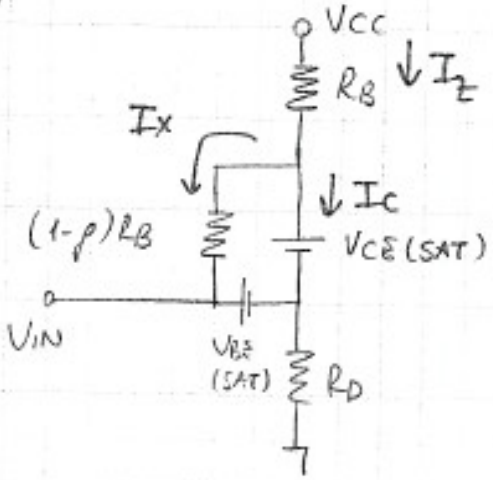
OR

✓ So, with NAND any logic operation can be implemented

Analysis Of Self-Bias Configuration :



Assume SAT



$$I_X = \frac{V_{CE(SAT)} - V_{BE(SAT)}}{(1-\beta)R_B}$$

$$I_E = \frac{V_{IN} - V_{BE(SAT)}}{R_D}$$

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$$I_C = \frac{(V_{CC} - V_{in} + V_{BE(SAT)} - V_{CE(SAT)})}{\rho R_B}$$

$$I_C = I_1 - I_X$$

$$= \frac{V_{CC} - V_{in} + V_{BE(SAT)} - V_{CE(SAT)}}{\rho R_B} + \frac{V_{BE(SAT)} - V_{CE(SAT)}}{(1-\rho) R_B}$$

$$I_B = I_E - I_C$$

$$= \frac{V_{IN} - V_{BE(SAT)}}{R_D} - I_C$$

Saturation Condition:

$$\beta_F I_B > I_C \Rightarrow \beta_F I_E > (\beta_F + 1) I_C$$

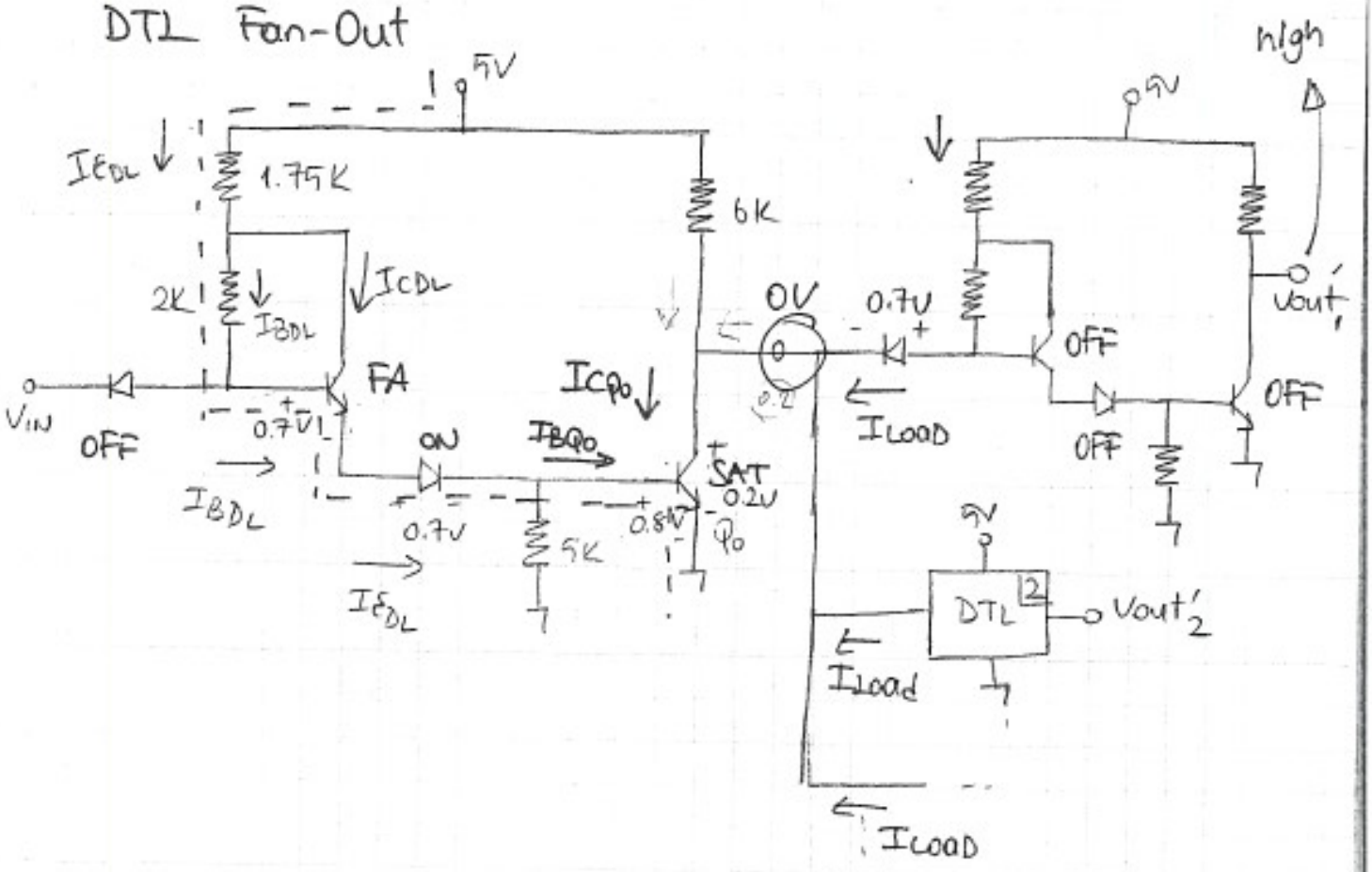
($I_B = I_E - I_C$)

$$\Rightarrow \frac{\beta_F}{R_D} (V_{in} - V_{BE(SAT)}) > (\beta_F + 1) \frac{(1-\rho)(V_{CC} - V_{IN})}{(1-\rho)\rho R_B} + (\beta_F + 1) \frac{V_{BE(SAT)} - V_{CE(SAT)}}{(1-\rho)\rho R_B}$$

V_{IN} ↑ satisfied

27.04.2010 FINANSBANK

DTL Fan-Out



(a) OH (Vout = High)

[Load DTL's have D_I in OFF mode, so NO effect on driver]

Fan-out = ∞

(b) OL (Vout = Low)

$$I_{LOAD} = \frac{5 - 0.9}{(2+1.75)K} = 1.09\ mA$$

$$I_{CQ_0} = N.I_{LOAD} + \frac{(5-0.2)}{6K} = N(1.09) + 0.8\ mA$$

To saturate Q_0 $\beta_F I_{BQ_0} > I_{CQ_0}$

$I_{BQ_0} = ?$

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KVL (- - -)

$$5 - \frac{7}{4} I_{EDL} - 2 I_{BDL} - 0.7 - 0.7 - 0.8 = 0$$

$I_{BDL} = \frac{I_{EDL}}{(B_F + 1)}$, $49 \sim$

$I_{EDL} = 1.6\ mA$

$$I_{BQ0} = I_{EDL} - \frac{0.8}{5K} = 1.6 - 0.16 = 1.44\ mA$$

$B_F . I_{BQ0} > N(1.09) + 0.8$

$B_F . (1.44) > N(1.09) + 0.8$

$49 . (1.44) > N(1.09) + 0.8$

$$N < \frac{(1.36)\,49}{1.09}$$

$N < 64 \ldots$

$\boxed{N_{OL} = 64}$

(ex) DTL fan-out calculation can also be done for a specific saturation parameter. Repeat the previous calculations if the driver is allowed to saturate at $G_{SAT} = 0.85$

$$G_{SAT} = \frac{I_C}{B_F I_B} = 0.85 \qquad B_F I_{BQ0} . (0.85) = I_{CQ0}$$

$49\,(1.44)\,(0.85) = N(1.09) + 0.8$

$\boxed{N = 54}$

Reverse Active Region (TTL)

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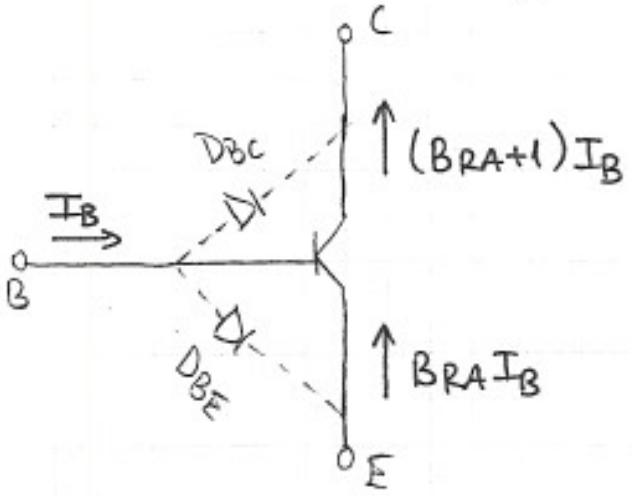
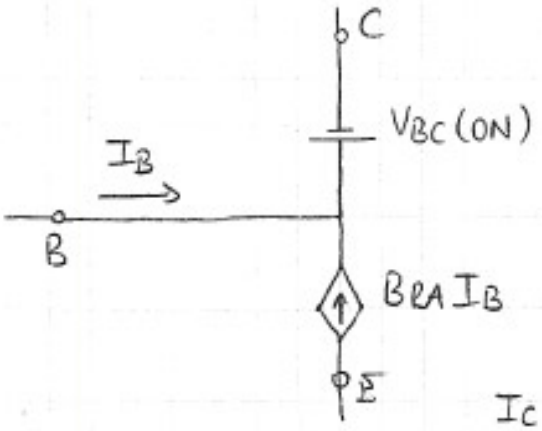
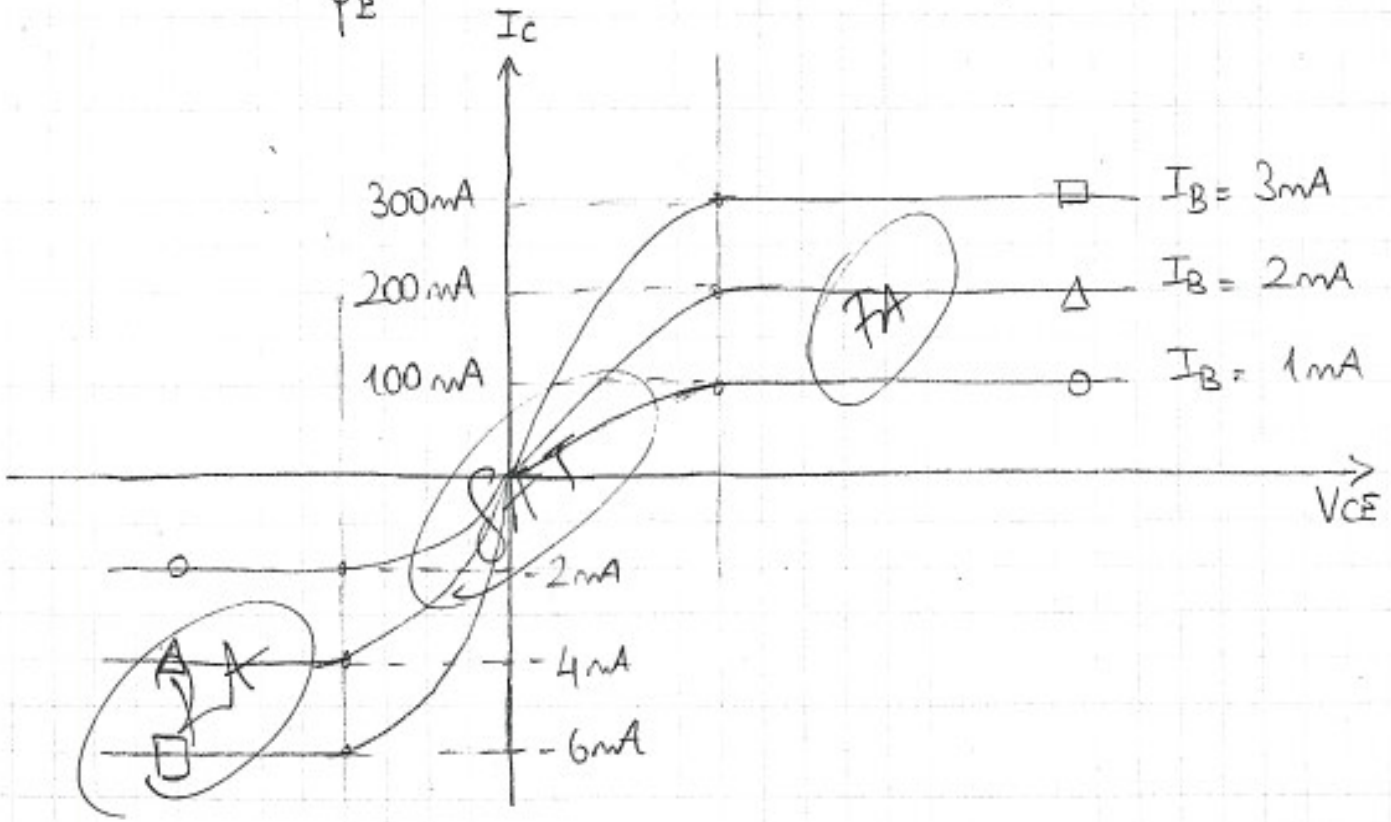


D_{BC}	D_{BE}	Q
OFF	OFF	OFF
ON	OFF	RA
OFF	ON	FA
ON	ON	SAT

Model For RA:



$B_{RA} \lesssim 1$ (Remember $B_{FA} \lesssim 100$)



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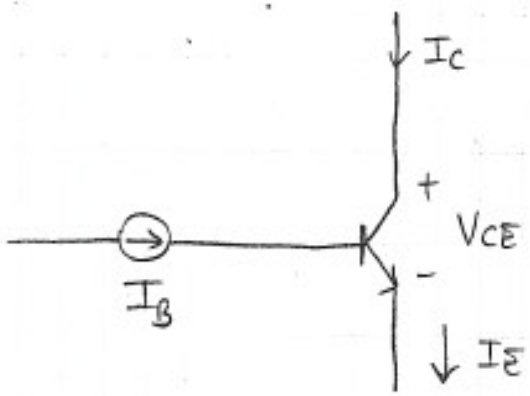
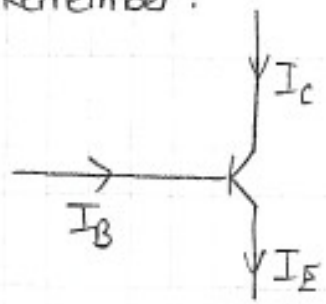


Modifications for SAT condition:

① $\beta_F I_B > I_C \longrightarrow$ Not FA
$\beta_{RA} I_B > -I_E \longrightarrow$ Not RA
} SAT

Remember:



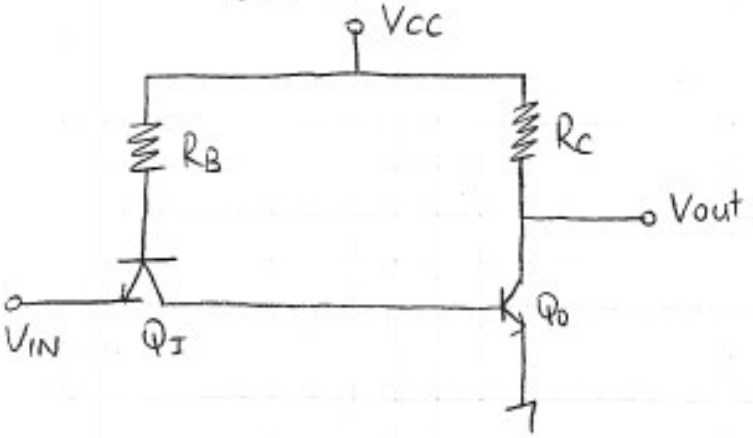
I_B, I_C, I_E as defined.

So, in RA $I_B > 0$ (Q should ON)

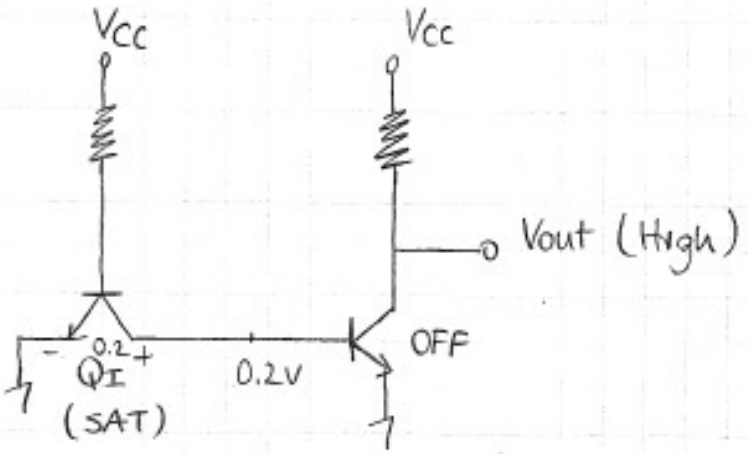
But $I_E < 0$ and

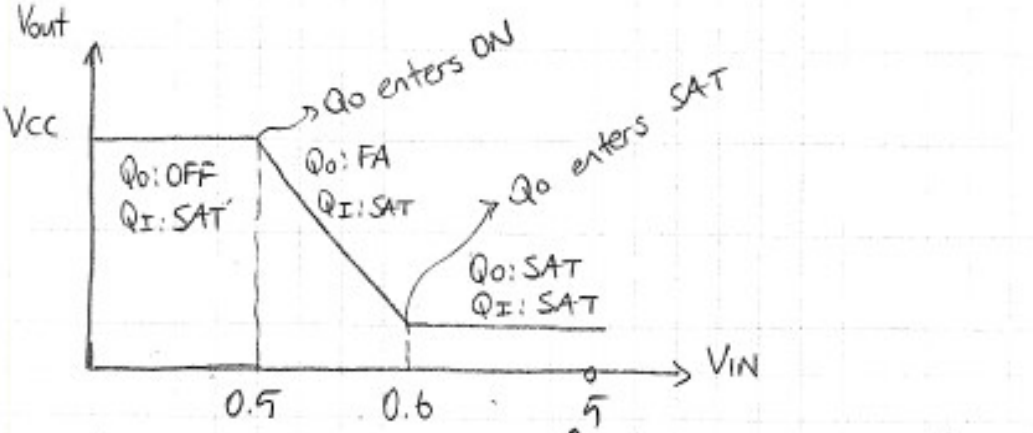
$I_C < 0$

TTL (Transistor – Transistor Logic)



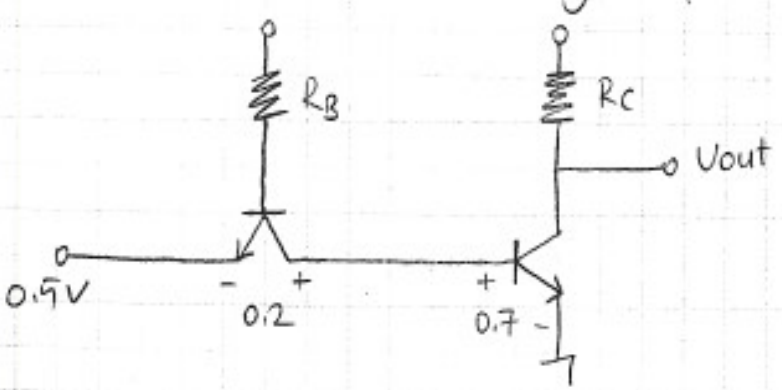
(1) V_{IN} : low





↑ at some higher voltage Q_I enters to RA

(2) Assume Q_o : at the edge of conduction



(3) (SAT is saturation)

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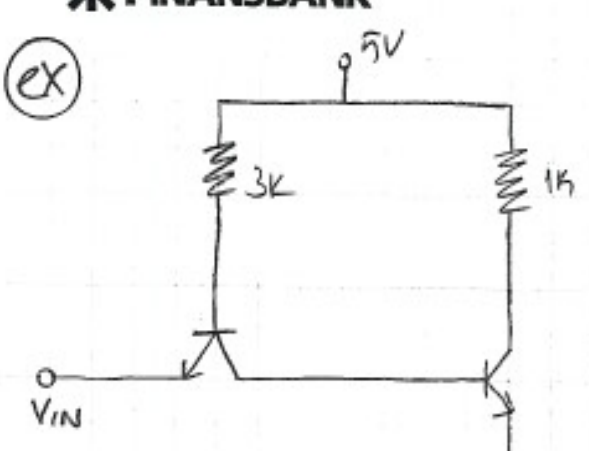
ex

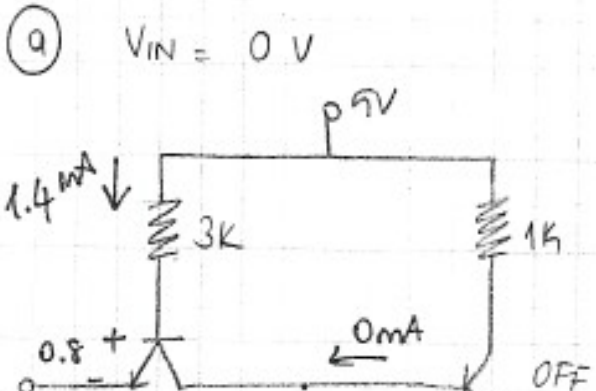


$B_F = 100 \quad B_R = 0.1$

(a) Analyze the system at

$V_{IN} = \{0.5\ V\}$

(a) $V_{IN} = 0\ V$



check OFF

① $V_{BE,Q_0} < 0.7\ V$ ✓

② $V_{BC,Q_0} < 0.7V$ ✓

check SAT

① $I_B > 0$ ✓ $(I_B = 1.4\ mA)$

② $B_F I_B > I_C \quad (I_C = 0)$

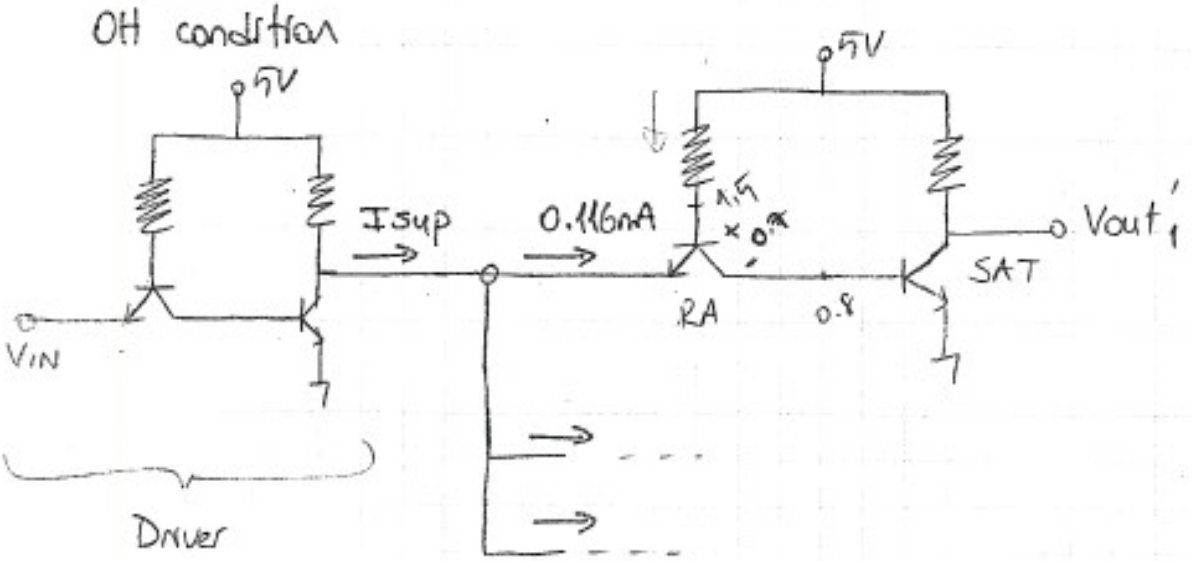
③ $B_R I_B > -I_E$

(b) Find fan-out, if under load conditions

(1) OH of driver can be at most 1 V less than ∞ load condition

(2) OL of driver should be saturated at most $G_{SAT} = 0.85$

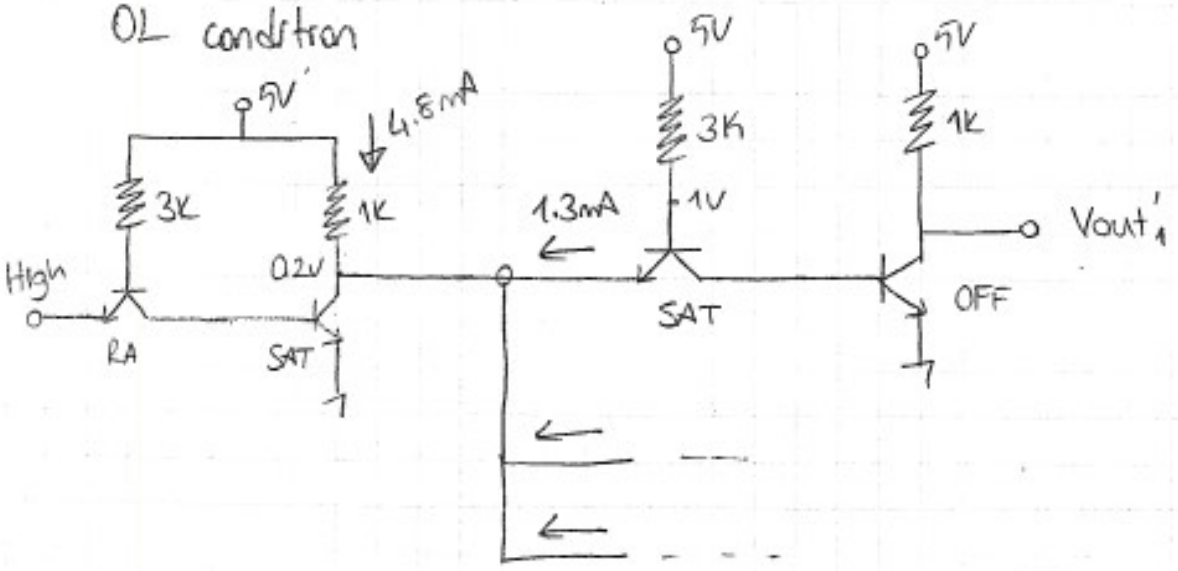
OH condition



$I_{sup} = N.(0.116)\,mA$

Valid value for Vout is 4V or higher

OL condition



$N(1.3)\,mA$ should be absorbed by the driver.

$$G_{SAT,Q_3} = \frac{B_F . I_{B,Q_3}}{I_{C,Q_3}} = 0.85$$

$$\left(4.8 + N.\frac{4}{3}\right)$$

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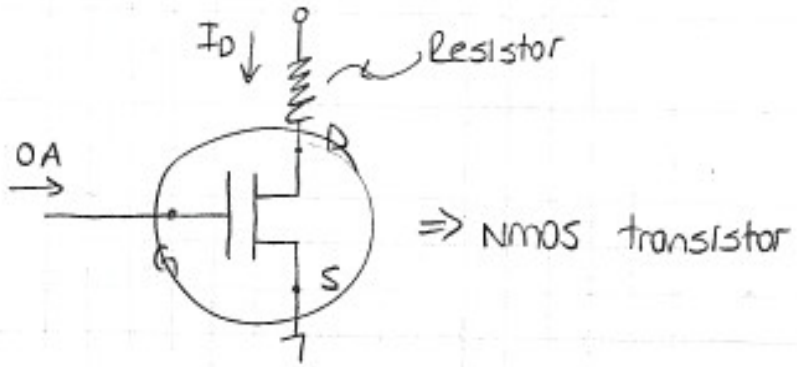
Resistor Loaded NMOS:

NMOS : N type MOS device

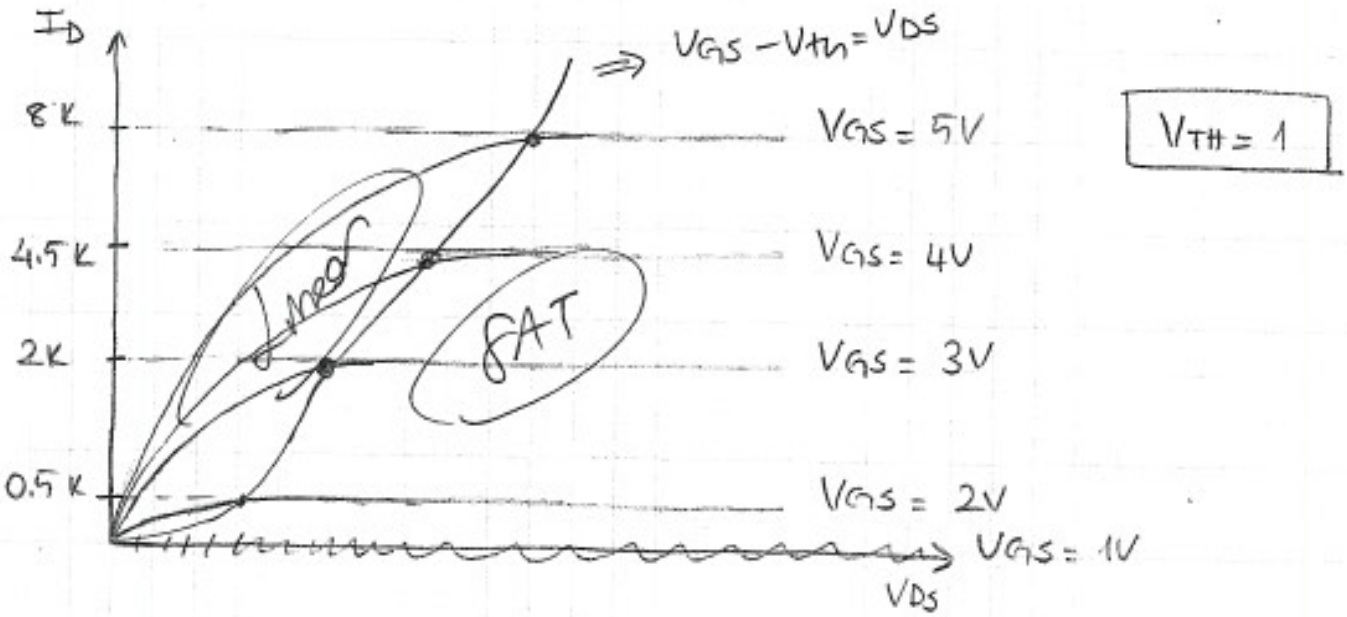


⇒ NMOS transistor

G: Gate (B)

D: Drain (C)

S: Source (E)



$V_{TH} = 1$

$$I_D^{SAT} = \frac{K}{2}\left[V_{GS} - V_{th}\right]^2 \quad ; \quad V_{DS} \geq V_{GS} - V_{th}$$

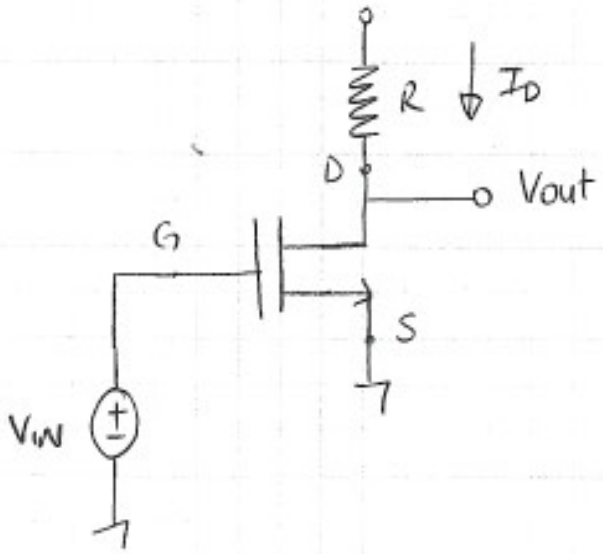
$$I_D^{linear} = K\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad ; \quad V_{DS} \leq V_{GS} - V_{th}$$

V_{th} : Threshold Voltage

K : A constant with units A/V^2

For SAT and linear region, the global turn-on condition

$$V_{GS} > V_{th}$$



$$V_{out} = V_{DS} = V_{DD} - R I_D$$

$$V_{IN} = V_{GS}$$

$$V_{out} = V_{DD} - R I_D$$

$$I_D = \frac{V_{DD} - V_{out}}{R}$$

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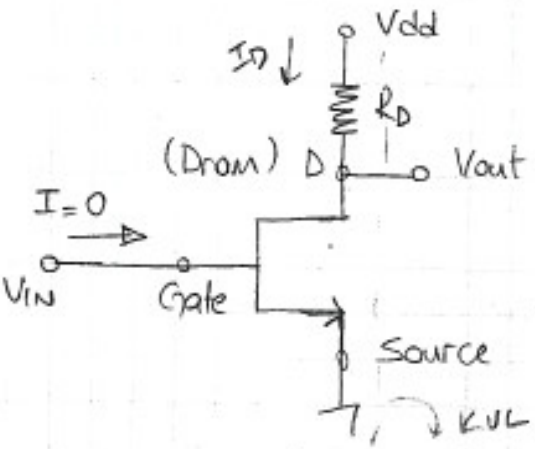
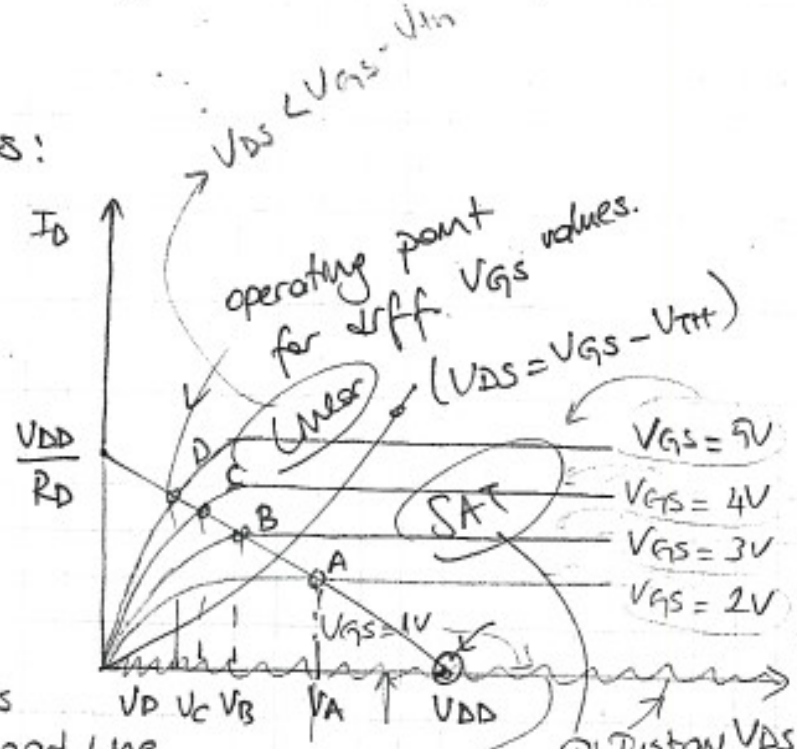
7.05.2010

Review

Resistor Loaded NMOS:



$V_{DD} = I_D R_D + V_{DS}$ ← Load Line



Q: Tuston VDS

$V_{DS} > V_{GS} - V_{th}$ ← eşik volt.

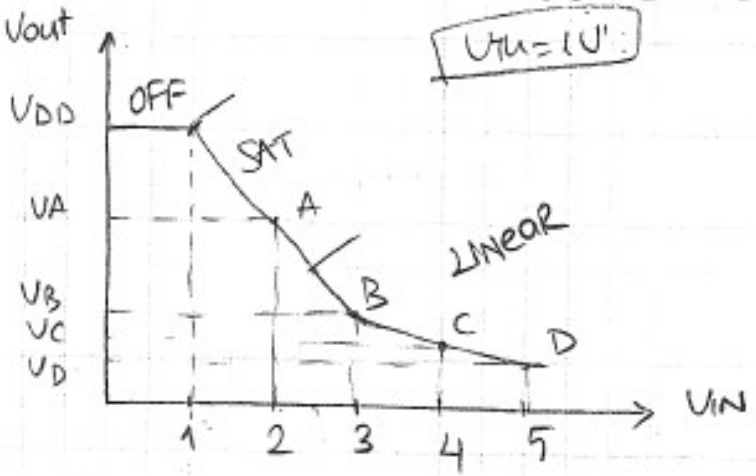
$I_D > 0$ (Q: ON) when $V_{GS} > V_{th}$

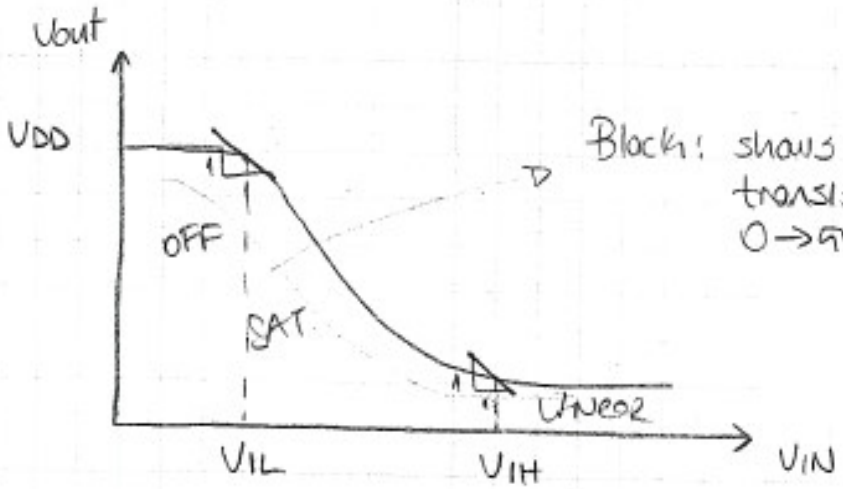
Note: $V_{IN} = V_{GS}$

$V_{out} = V_{DS}$

$V_{th} = 1V$

NMOS





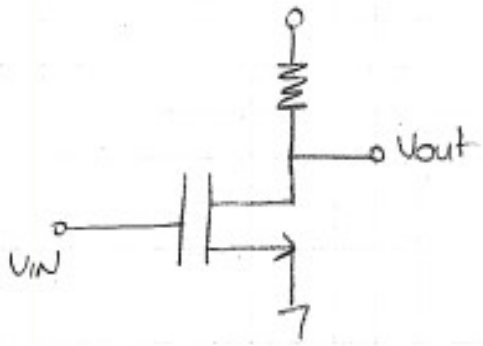
Black: shows the state of the transistor as VIN goes from 0 → 5V

For NMOS systems V_{IL}, V_{IH} is defined as

V_{IL} : Q: SAT and $\frac{\partial V_{out}}{\partial V_{IN}} = -1$

V_{IH} : Q: Linear and //

Power Dissipation of Resistor Loaded NMOS



Vout → OH → Q: OFF, $I_D = 0A$

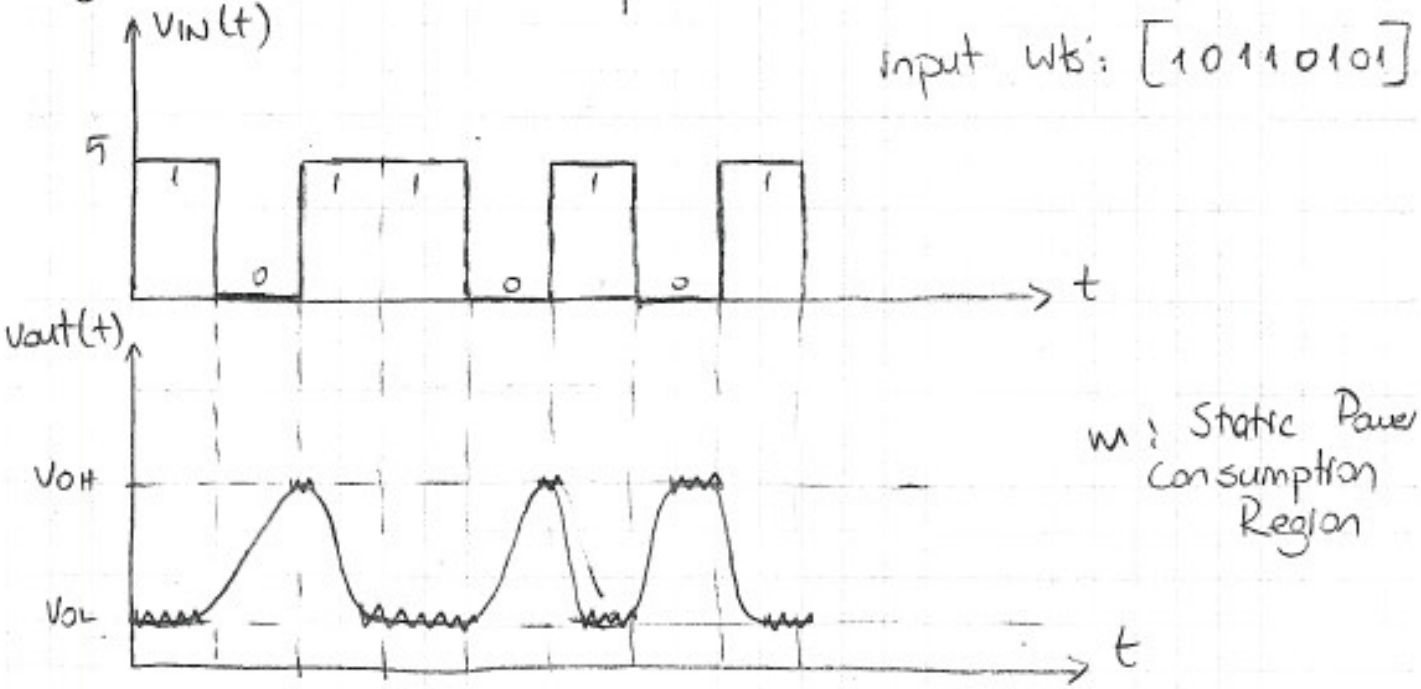
↳ OL → Q: Linear,

$$I_D = \frac{(V_{DD} - V_{OL})}{R_D}$$

$$P_{AVG} = \left(\frac{I_{D(OH)} + I_{D(OL)}}{2} \right) V_{DD} \quad \text{watts}$$

(Consumes power only in OL state!)

Dynamic Power Consumption



input wf: [10110101]

w: Static Power Consumption Region

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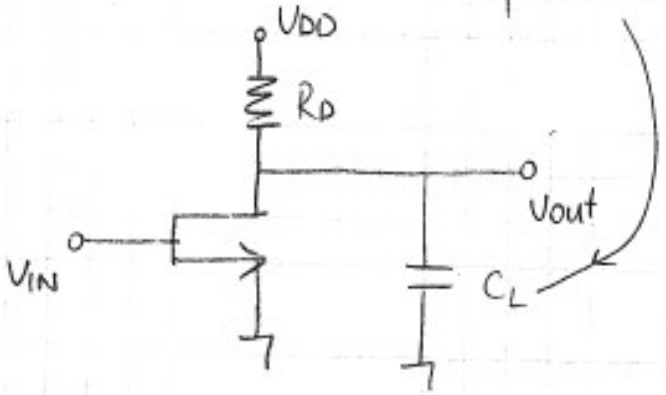
$$P^{Dynamic} = C_L \cdot f \cdot V_{DD}^2$$

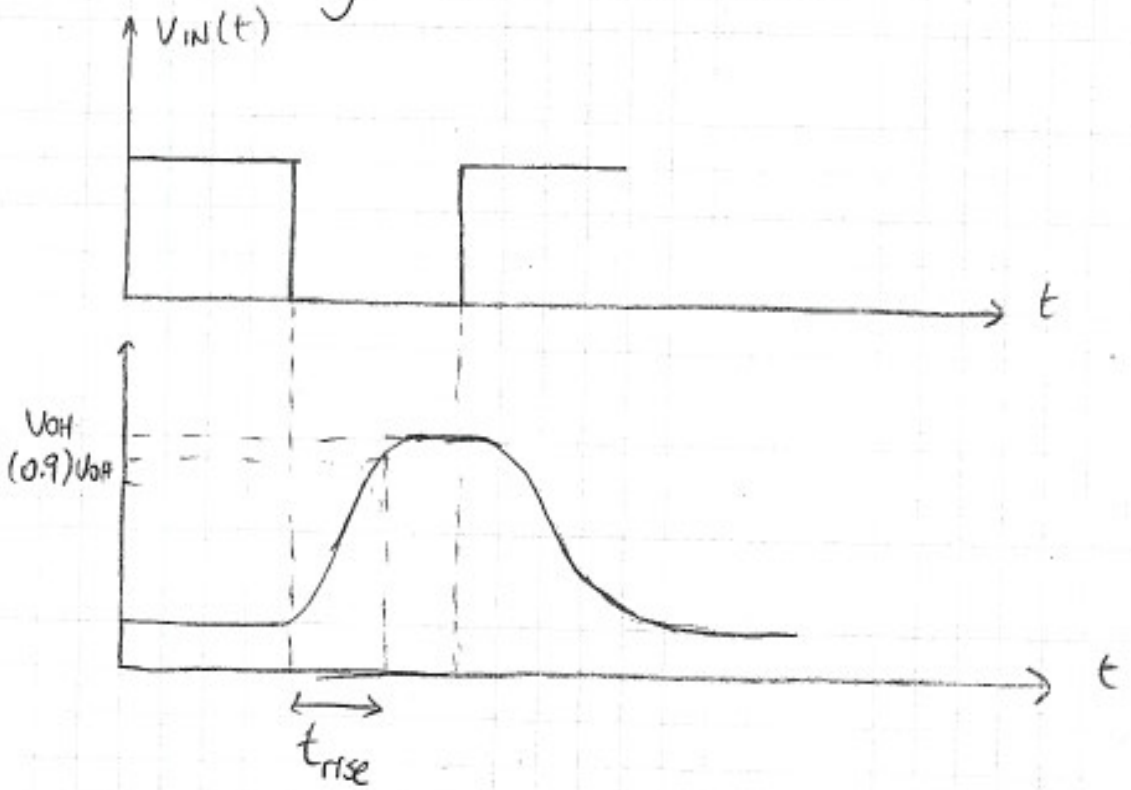
- C_L: Load Capacitance
- f: frequency of switching (1/sec) → V_{tn}
- V_{DD}

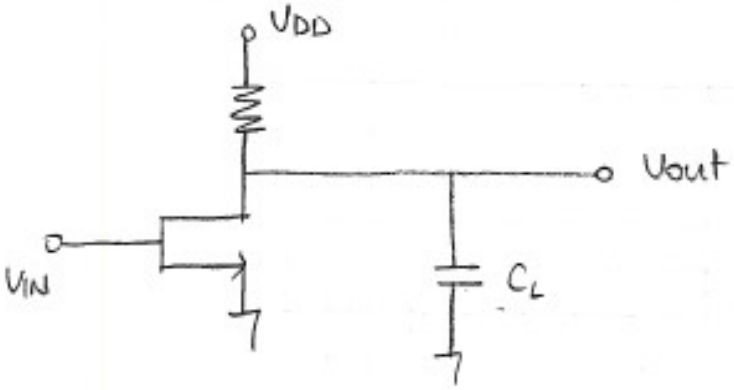


As freq. increases dynamic power consumption increases.

(RTL circuit dynamic power consumption is negligible in comp. to static power cons.)

Switching Time Calculation





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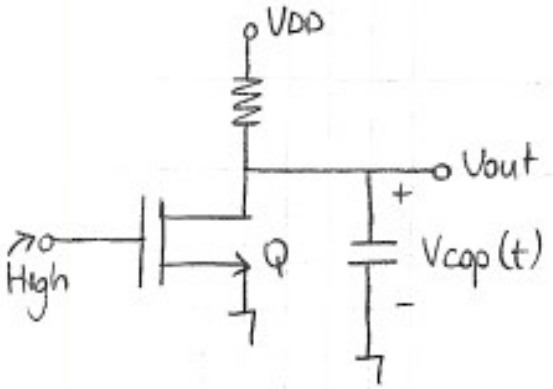
(a) 0L → 0H (Input is suddenly charged from High to Low)

Before Switching

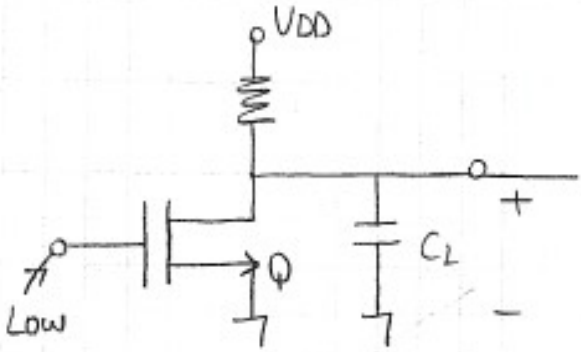


Q : Linear Region

$V_{out}(0^-) = V_{cap}(0^-) = V_{OL}$

↗ just before switching

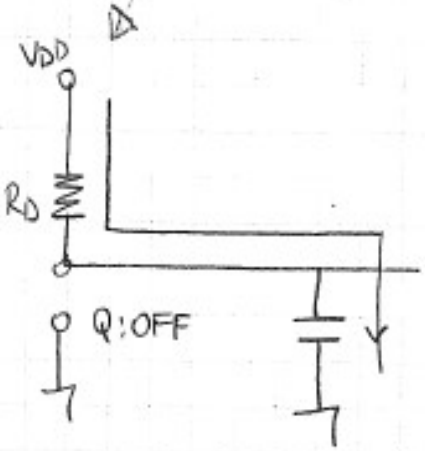
After Switching



$V_{out}(0^+) = V_{cap}(0^+) = V_{cap}(0^-)$

$= V_{OL}$

Q: OFF ($V_{GS} > V_{th}$ ↙ 1V is no longer satisfied)



$V_{cap}(0^+) = V_{OL}$

$V_{cap}(\infty) = V_{DD}$

$\tau = RC$

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$$V_{cap}(t) = V_{cap}(\infty) + \left[\begin{array}{c} V_{cap}(0^+) \\ - \\ V_{cap}(\infty) \end{array} \right] e^{-t/\tau}$$

Then $V_{OH} = V_{DD}$, the time when

$V_{out} = (0.9)\, V_{OH} = 0.9\, V_{DD}$ is the rise time.

$$V_{cap}(t) = V_{DD} + [V_{OL} - V_{DD}]\, e^{-t/RC} \quad \downarrow t = t_{rise}$$

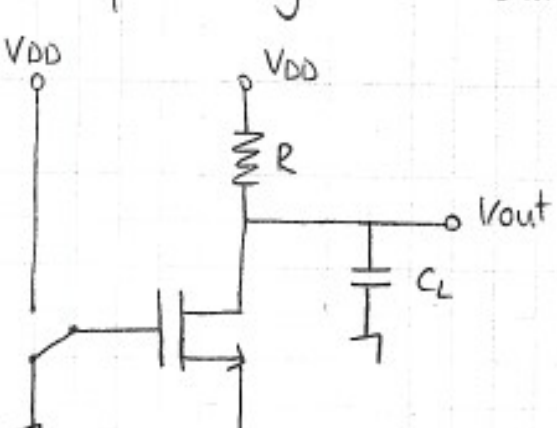
$$0.9\, V_{DD} = V_{DD} + [V_{OL} - V_{DD}]\, e^{-t_{rise}/RC}$$

$\downarrow$

t_{rise} is found from here

18.05.2010

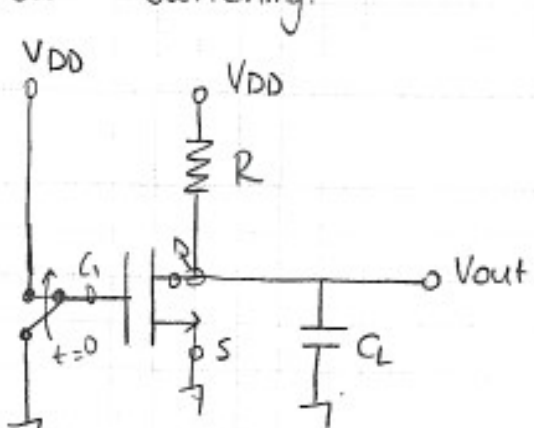
(b) Output: High $\longrightarrow$ Output: Low Switching.



$t = 0^-$

Q: OFF $\rightarrow$ $V_{out}(0^-) = V_{DD}$

$V_{cap}(0^-) = V_{DD}$



$t = 0^+$

Q: (NOT OFF, $\nearrow$ $\searrow$

$V_{cap}(0^+) = V_{cap}(0^-) = V_{DD}$

Q: (Not OFF, $\xrightarrow{SAT}$ $V_{DS}(t) > V_{GS}(t) - V_{th}$

$\xrightarrow{Lineer}$ $V_{DS}(t) < V_{GS}(t) - V_{th}$

at $t = 0^+$

$V_{DS}(0^+) = V_{DD}$

$V_{GS}(0^+) = V_{DD}$

at $t = 0^+ \longrightarrow V_{DS}(0^+) > V_{GS}(0^+) - V_{th}$ ✓

↓

Q in SAT

(just after switching)

Q remains SAT until

$V_{DS}(t) = V_{GS}(t) - V_{th}$

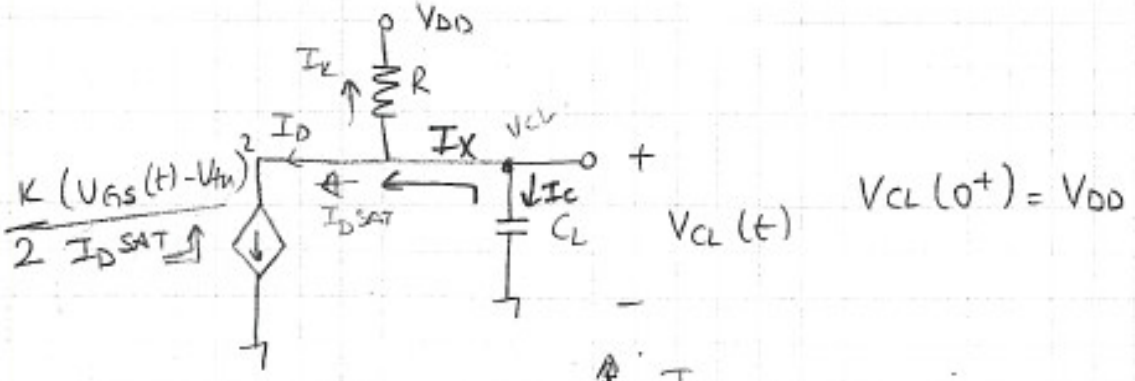
$V_{DS}(t) = V_{out}(t)$; $V_{GS} = V_{DD}$

until

$V_{out} = V_{DD} - V_{th}$

Q: in SAT

$V_{DD} - V_{th} < V_{out}(t) < V_{DD}$



$V_{CL}(0^+) = V_{DD}$

$$I_X = I_D^{SAT} + \frac{V_{CL}(t) - V_{DD}}{R} = -I_C$$

$$I_C = C_L \cdot \frac{dV_{CL}}{dt}$$

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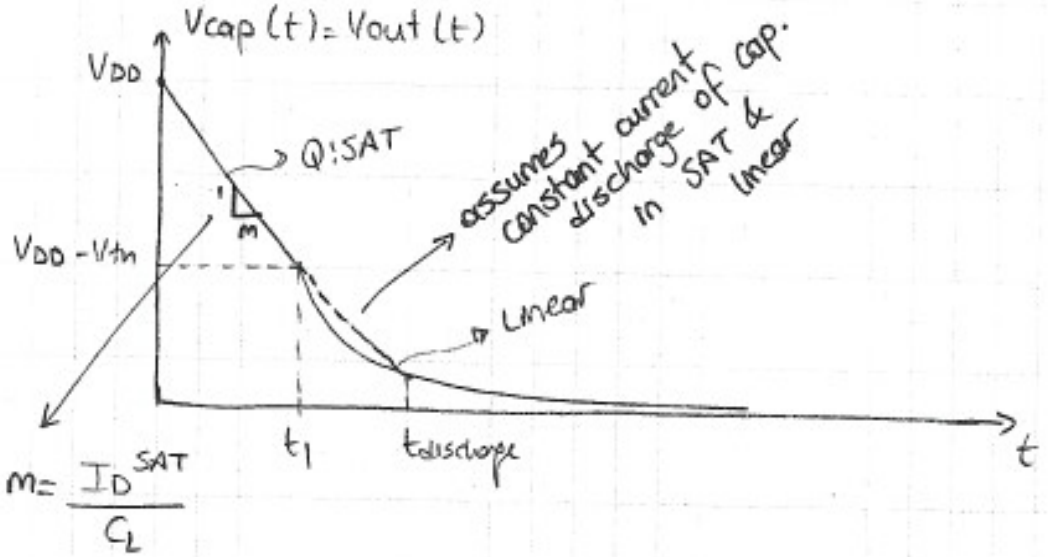
$$\frac{d}{dt} V_{CL}(t) + \frac{V_{CL}(t)}{RC_L} = -\frac{I_D^{SAT}}{C_L} + \frac{V_{DD}}{RC_L}$$

First order diff. eq.

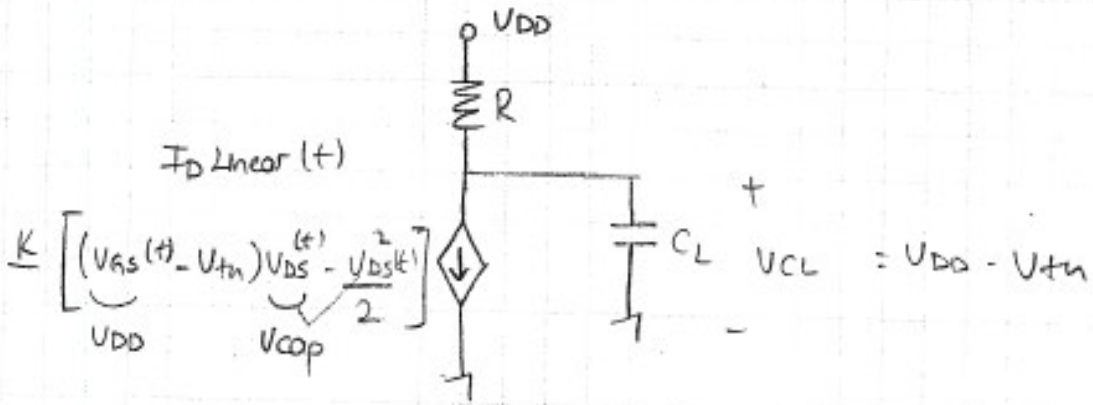
In practice R is large so that $RC_L >> C_L$

$$\downarrow$$

$$\frac{d}{dt} V_{CL}(t) \cong -\frac{I_D^{SAT}}{C_L}$$



$V_{out} < V_{DD} - V_{th} \rightarrow$ Q is linear



$$C.\ \frac{dV_{CL}}{dt} = \frac{V_{DD} - V_{CL}(t)}{R_L} - K\left[(V_{DD} - V_{th})V_{cap}(t) - \frac{V_{cap}^2(t)}{2}\right]$$

$V_{CL}(t_1) = V_{DD} - V_{th}$

Even if R is large $(R >> C)$ $\left(\frac{1}{R} << C\right)$

$$C\frac{dV_{CL}}{dt} \cong -K\left[V_{DD} - V_{th}\right] V_{cap}(t) + \frac{K}{2} V_{cap}^2(t)$$

↑ non-linear dff. equa.

NOTE:

NMOS:

OFF → $V_{GS} < V_{th}$

ON → $V_{GS} > V_{th}$

SAT → $V_{DS} > V_{GS} - V_{th}$

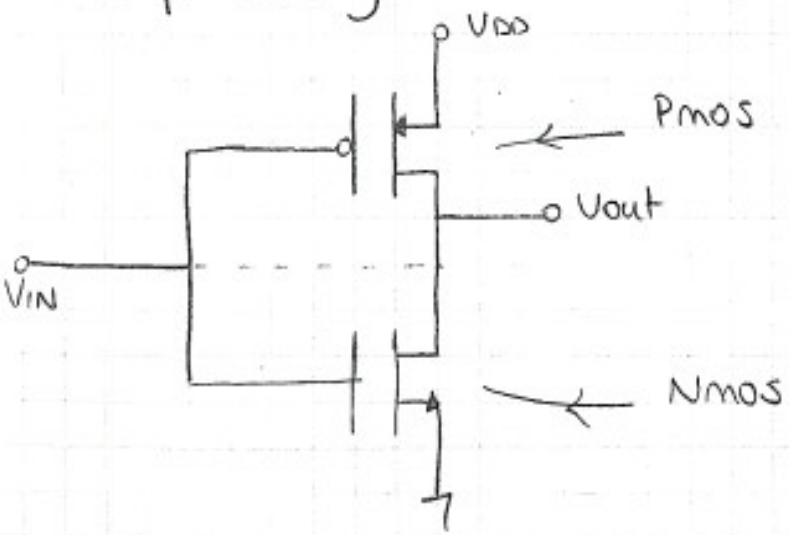
Linear → $V_{DS} < V_{GS} - V_{th}$

$$I_D^{SAT} = \frac{K}{2}.(V_{GS} - V_{th})^2$$

$$I_D^{linear} = K\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Complementary MOS Devices (CMOS)

21.09.2010



Nmos with Pmos load (resistor load)

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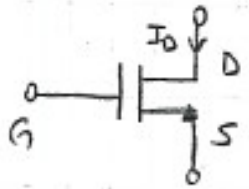
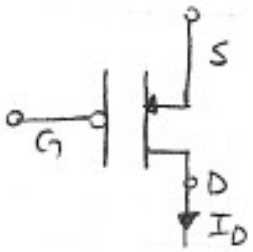
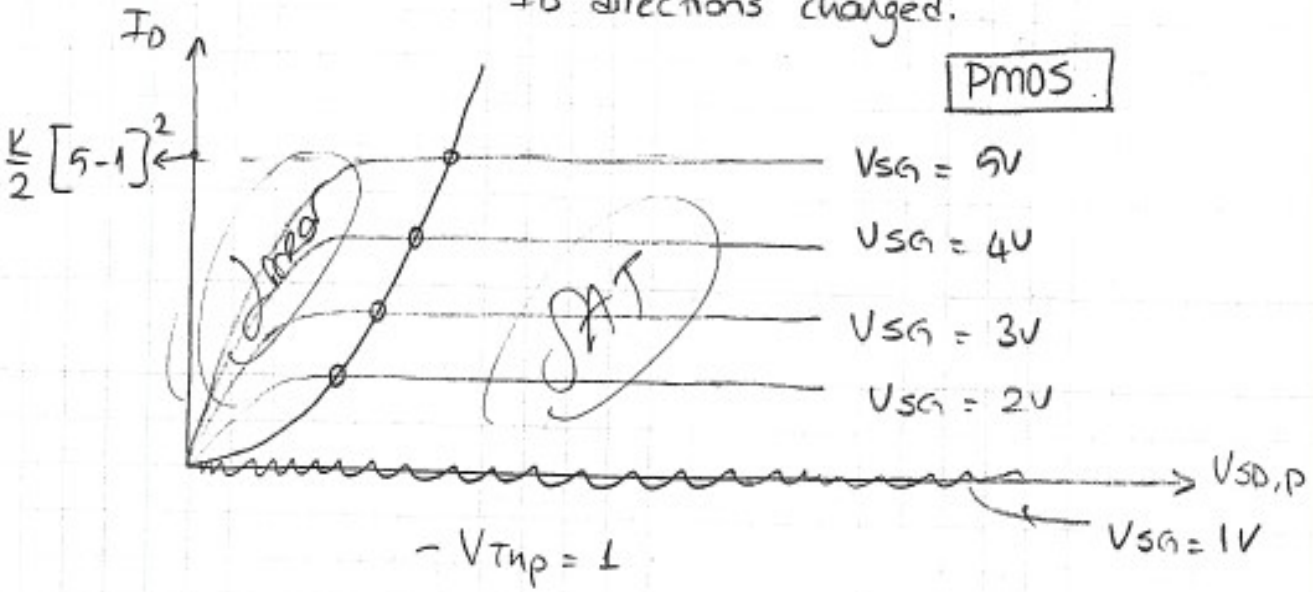
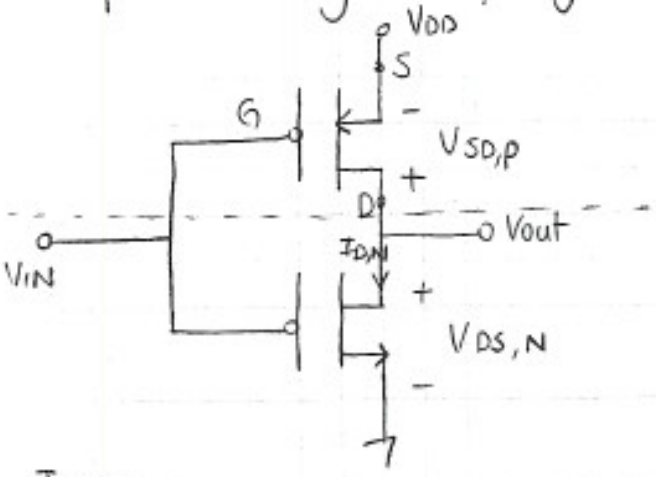
Nmos	Pmos
$V_{th}, V_{GS}, V_{DS}, I_D$	$V_{Th_p}, V_{SG}, V_{SD}, I_D$
	
ON: $V_{GS} > V_{Th}$, $(I_D > 0)$	ON: $V_{SG} > -V_{Th_p}$, $(I_D > 0)$
SAT: $I_D = \frac{K}{2}\left[V_{GS} - V_{Th}\right]^2$; $(V_{DS} > V_{GS} - V_{Th})$	SAT: $I_D = \frac{K}{2}\left[V_{SG} + V_{Th_p}\right]^2$; $V_{SD} > V_{SG} + V_{Th_p}$
LINEAR: $I_D = K\left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right]$; $(V_{DS} < V_{GS} - V_{Th})$	LINEAR: $I_D = K\left[(V_{SG} + V_{Th_p})V_{SD} - \frac{V_{SD}^2}{2}\right]$; $V_{SD} < V_{SG} + V_{Th_p}$

GS → SG
DS → SD
$V_{th} \rightarrow -V_{th}$

I_D directions changed.



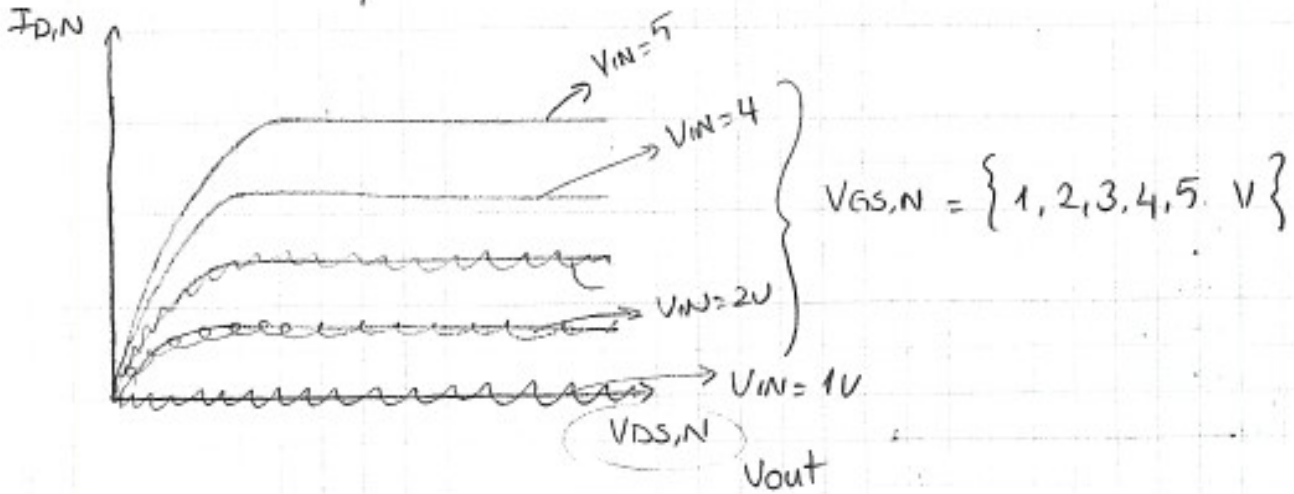
Graphical Analysis of Symetric CMOS Inverter



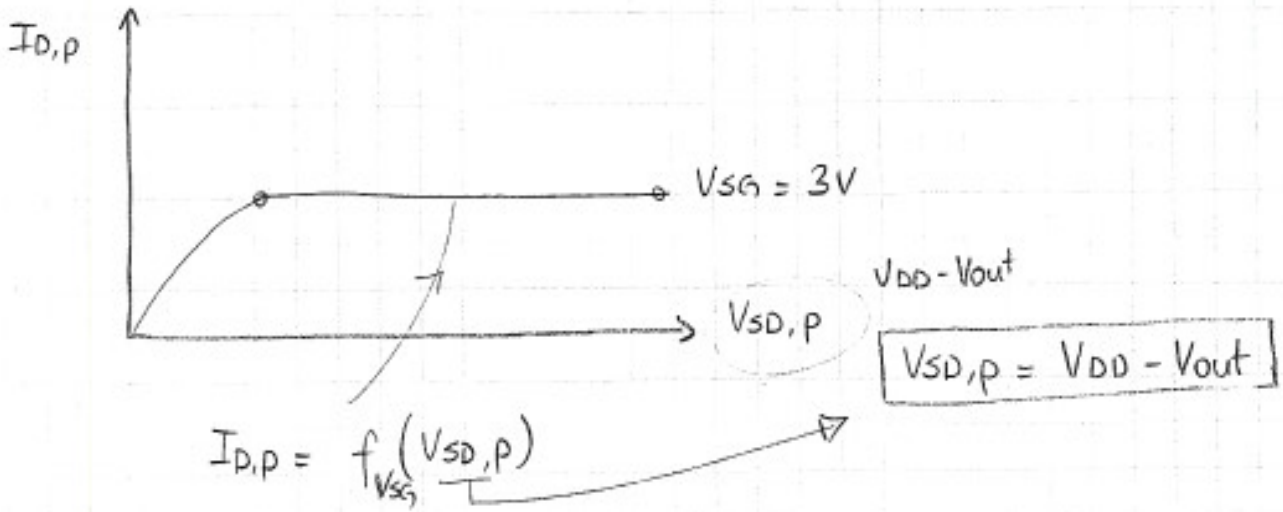
$V_{out} = V_{DS,N}$

$V_{IN} = V_{GS,N}$

$V_{IN} = V_{DD} - V_{SG,P}$



$V_{GS,N} = \{1, 2, 3, 4, 5\ V\}$



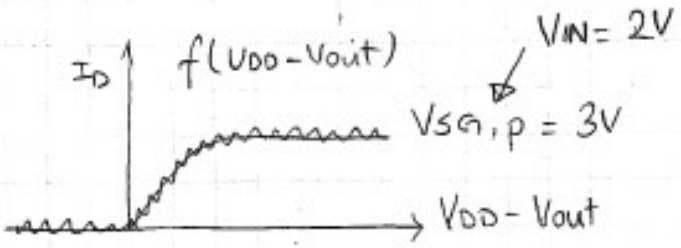
$V_{SD,P} = V_{DD} - V_{out}$

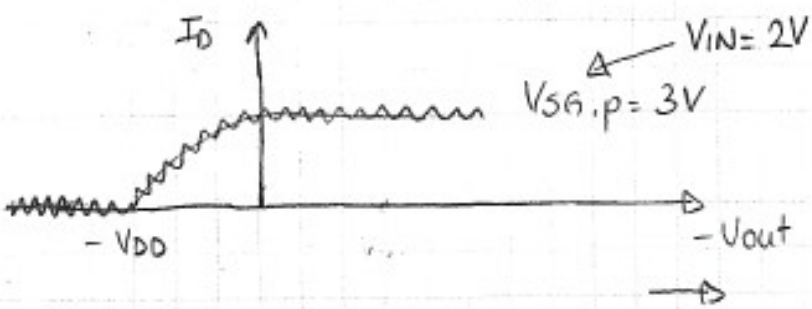
$I_{D,P} = f_{V_{SG}}(V_{SD,P})$

$I_{D,P} = f_{V_{SG}}(V_{DD} - V_{out})$

$= \hat{f}(-V_{out})$

$= f(V_{out})$





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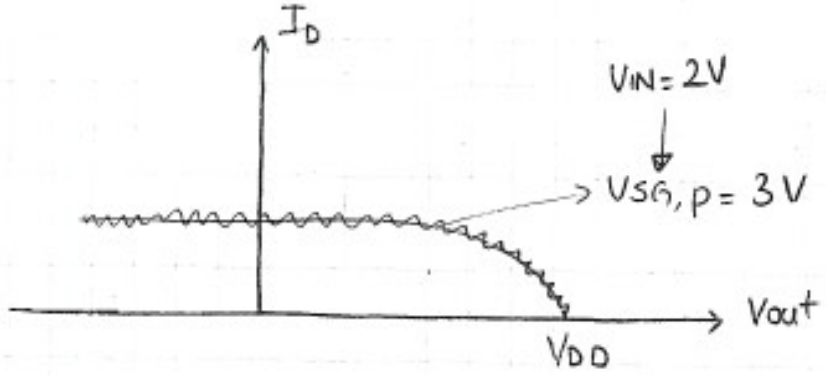
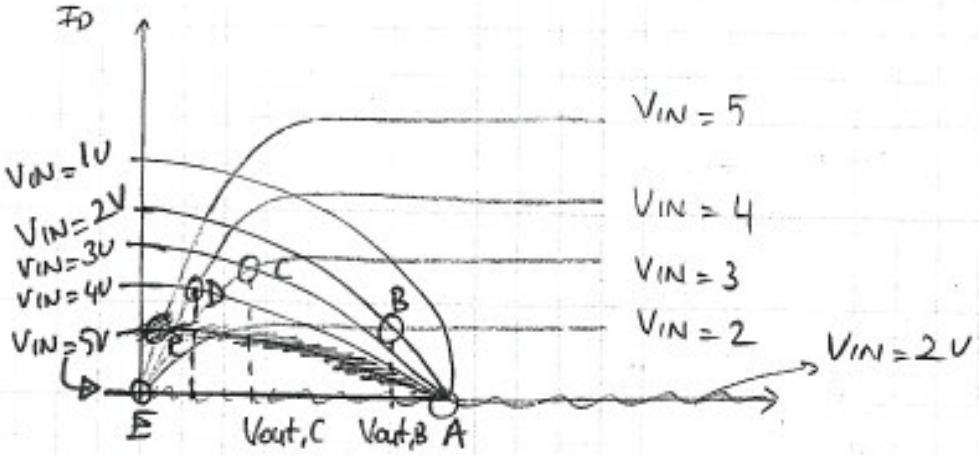
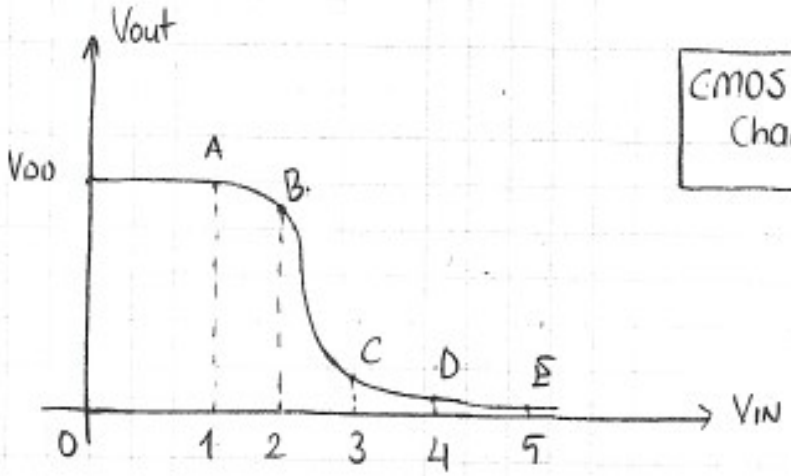


$\hat{\hat{f}}(x) = \hat{f}(-x)$



Black : N-Type Device

Pink : P-Type Device



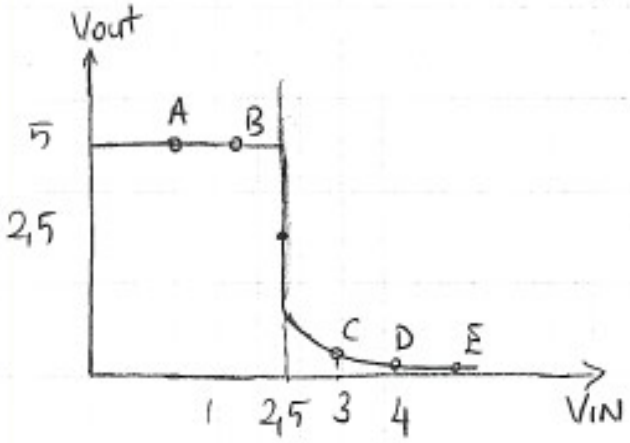
CMOS Characteristic

When $V_{Th,P} = -V_{Th,N}$ $K_P = K_N$

then NMOS and PMOS (I_D vs V_{DS})

(I_D vs V_{SD})

curves are identical and the symetrical curves result in

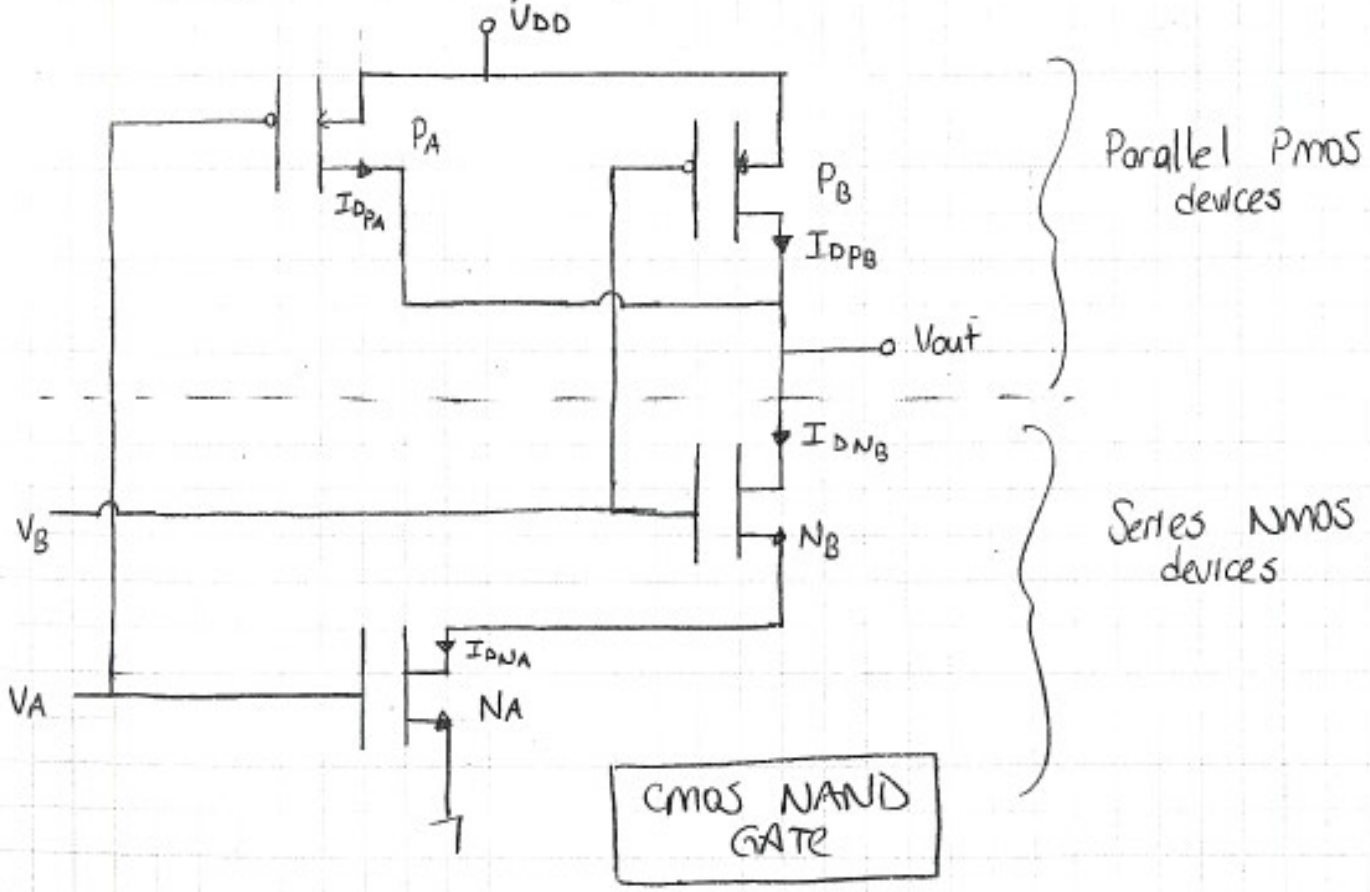


Almost equivalent to ideal inverter characteristic

(Does not consume any power at static condition)

(Only dynamic power consumption)

CMOS NAND / NOR Gates :



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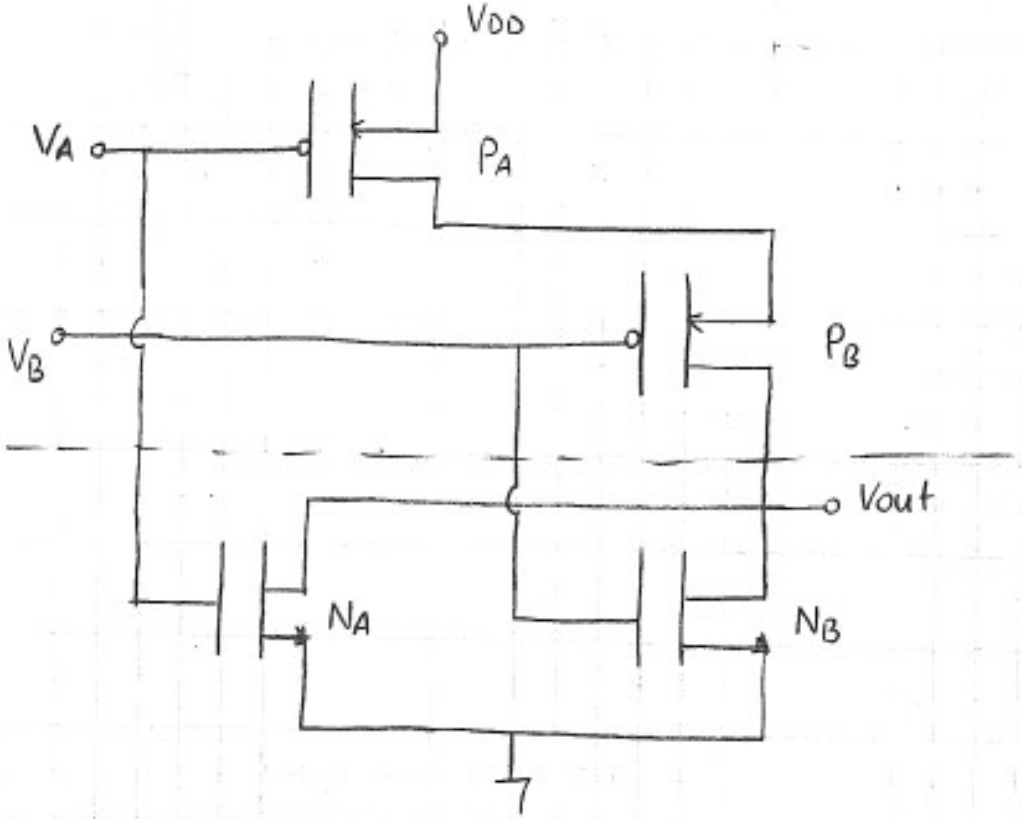
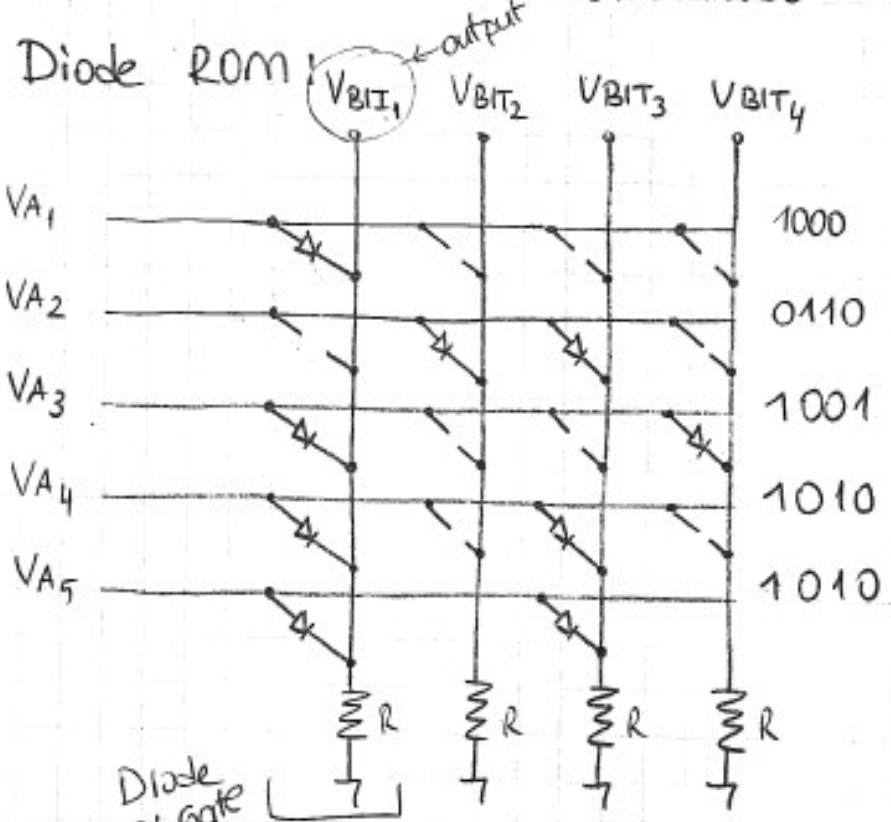


CMOS NOR Gate

Semiconductor ROM Structures

Diode ROM:

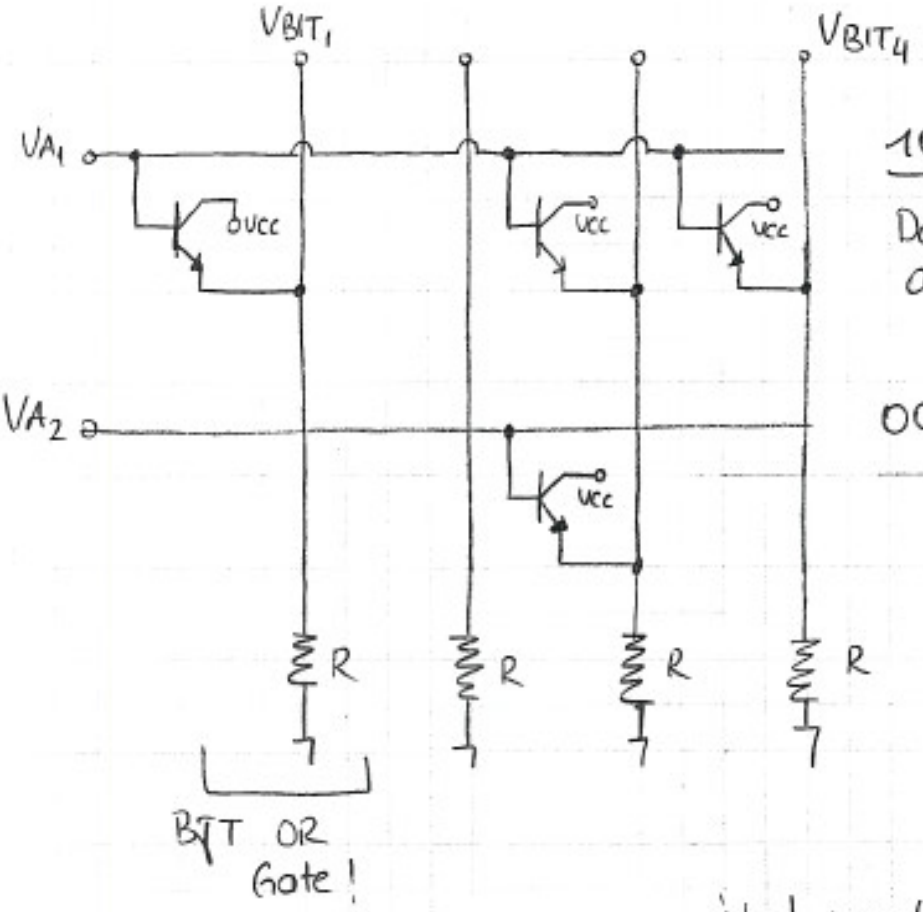


EPROM

{ VA1, VA2, VA3, VA4, VA5 }

Adress bus activation signal.

Only 1 address is selected at a time!



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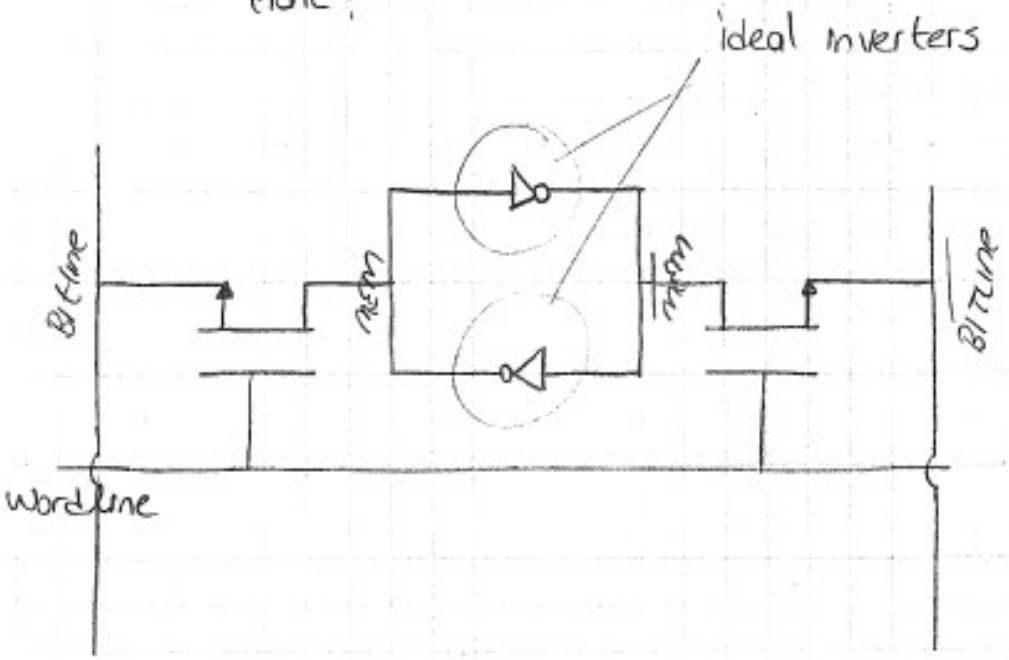
1011

Data read when A_1 is activated!

0010



Wordline : When High writes to RAM (N-MOSFET Transistors are ON when wordline is High)

Bitline : When wordline enables RAM writing, Bitline Value (High/Low) is passed to RAM

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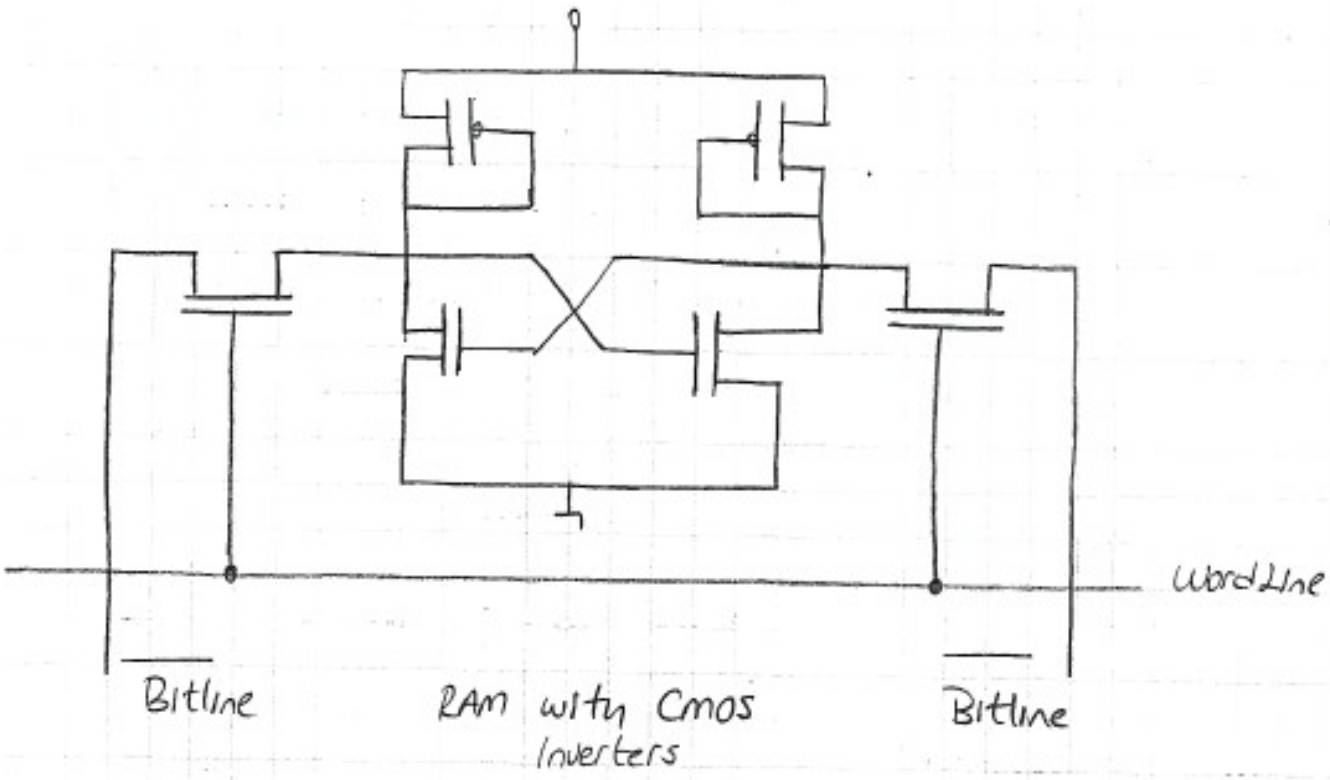


25.05.2010

Interfacing Logic Families

Considerations

1. Fast Switching (Low Delay)
2. Low Power Consumption

Power Delay Product:

In general, Power Consumption ↑

leads

faster switching

or

delay ↓

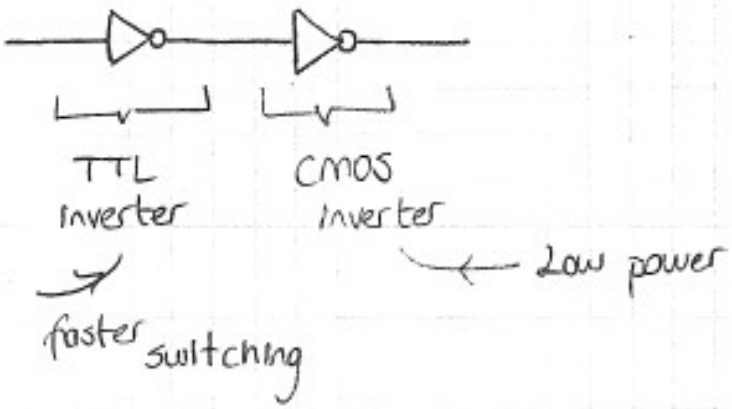
Family: Power x Delay ⇒ Power-Delay Product

watts ↑ sec ↑

For every logic family (RTL, TTL, DTL, CMOS) there is an associated power delay product.

Power-Delay product varies from family to family.

In some applications, you may want faster switching at some parts of the system, and low power consumption at others.



Interfacing Logic Families

Compatibility:

1. Voltage Compatibility
2. Current Compatibility

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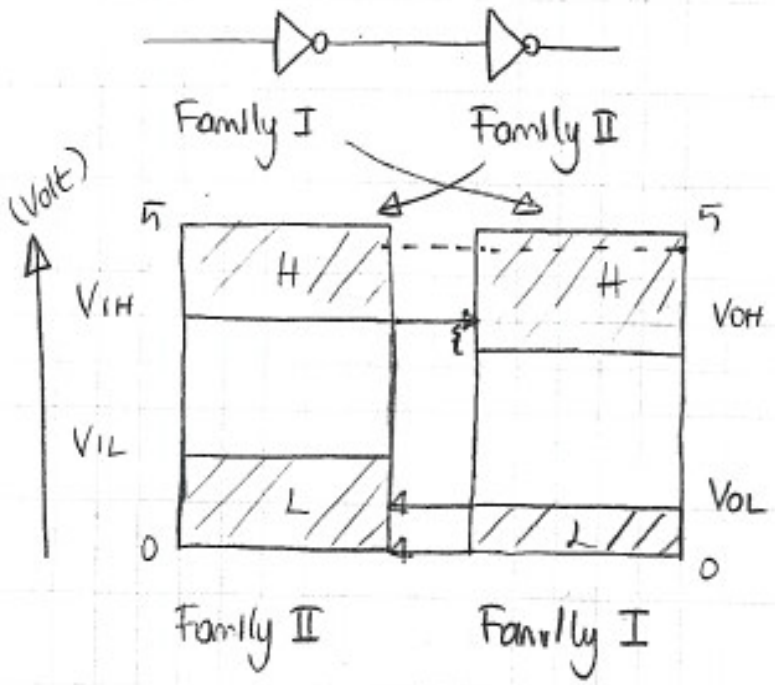
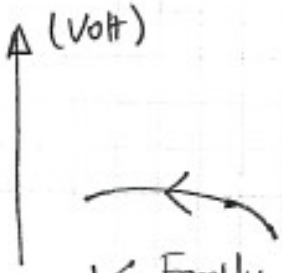
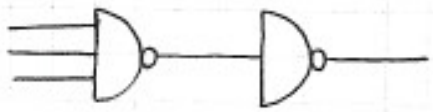
① Voltage Compatibility



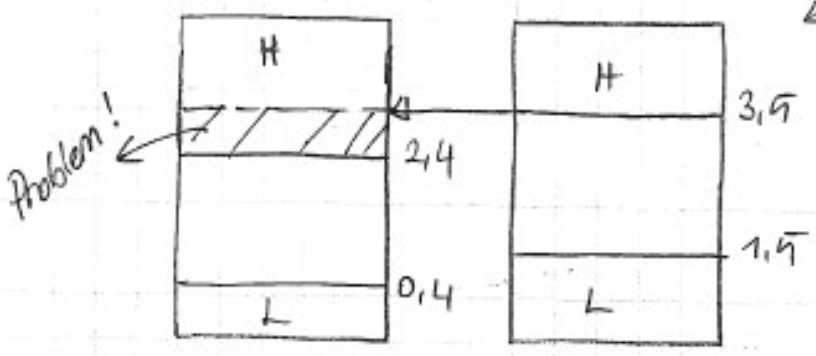


✓ Family I - Family II cascade has OH Voltage compatibility problem, but no voltage compatibility problem for OL.

(ex) TTL driving CMOS



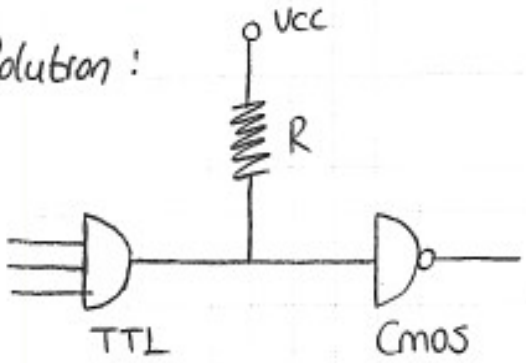
TTL (7400) CMOS (74C)

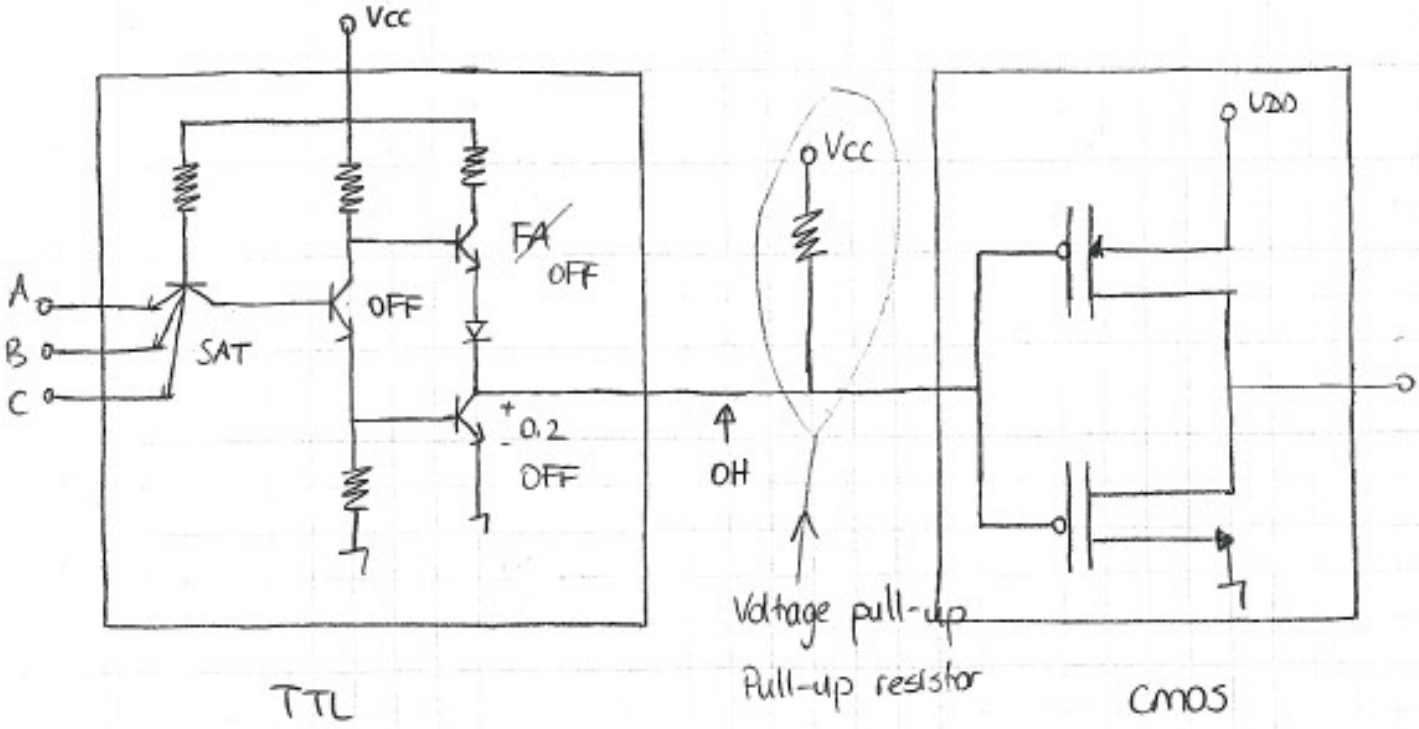


TTL output CMOS input

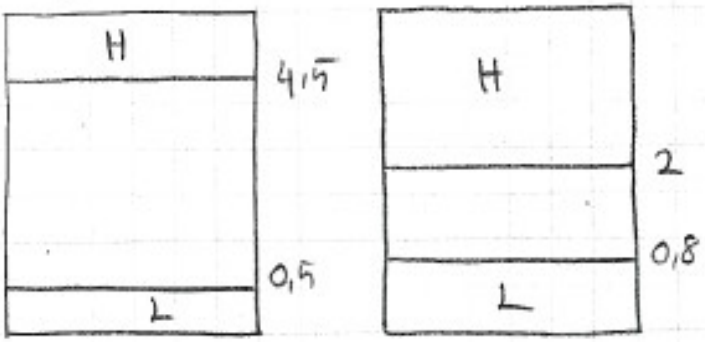
← Voltage compability problem at OH

Solution :





(ex) Cmos driving TTL



No voltage compatibility problem

31.05.2010

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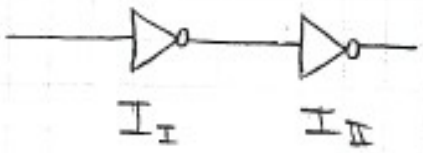
Interfacing Logic Families

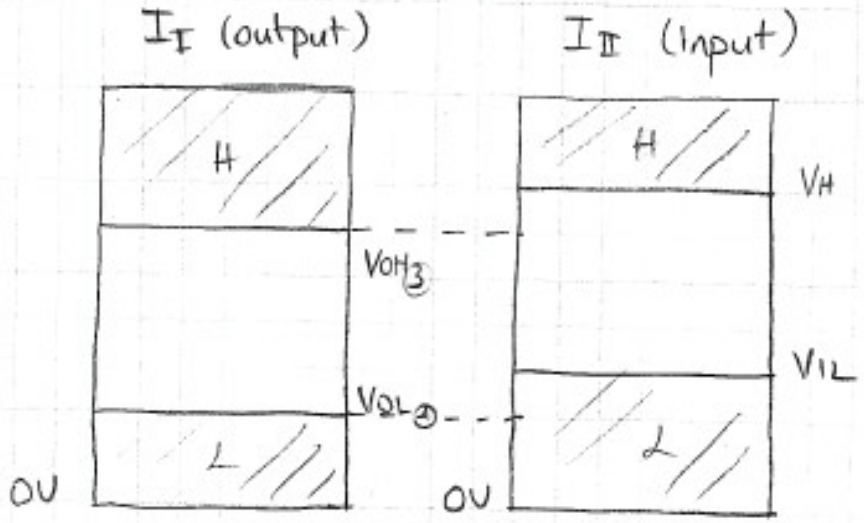
① Voltage Compatibility

② Current Compatibility

Review :

① Voltage Compability

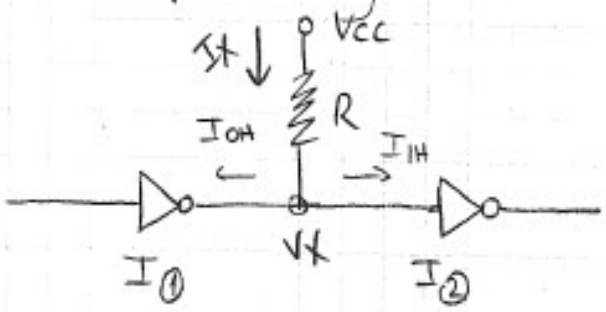




OH Voltage Compatibility Problem

No Voltage Compability problem at OL

② Current Compatibility



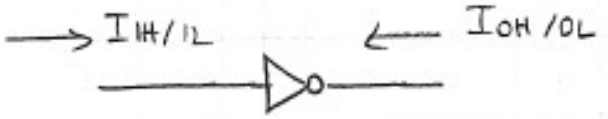
V_x: High , $I_{OH}^{①}$ and $I_{OH}^{②}$ limitations should be provided that is max ($I_{OH}^{①}$) and max ($I_{IH}^{②}$) for proper operation is given.

Then for current compatibility

$$I_x \left(\max I_{OH}^{①} + \max I_{IH}^{①} \right)$$

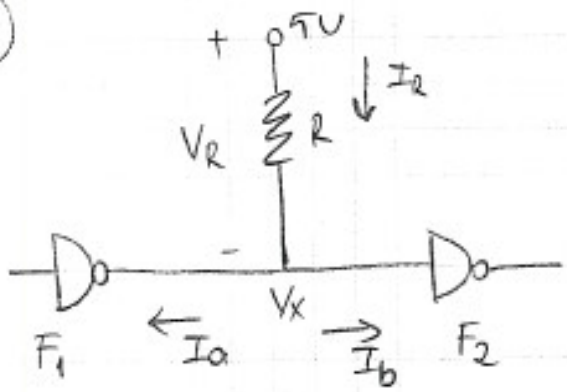
V_x : Low ; (the same reasoning)

$$I_x < \max I_{OL}^{①} + \max I_{IL}^{①}$$



Note: In the specifications currents are always entering into the component

(ex)



I_1 / F_1

$\max V_{OL}^{1} = 0.5$

V_{OH} = determined by R

$\max I_{OH}^{1} = 250\ \mu A$

$\max I_{OL}^{1} = 20\ mA$

(Both families are TTL)

I_2 / F_2

$V_{IH}^{2} = 2.4\ V$ $\quad \max I_{IH}^{1} = 20\ \mu A$

$V_{IL}^{2} = 0.8\ V$ $\quad \max I_{IL}^{2} = -360\ \mu A$

Find the interval for R for proper operation

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V_x : High

$V_x > 2.4\ V$, $V_R < 2.6\ V$ (Voltage Compa.)

$I_a = 0.25\ mA$

$I_b = 0.02\ mA$

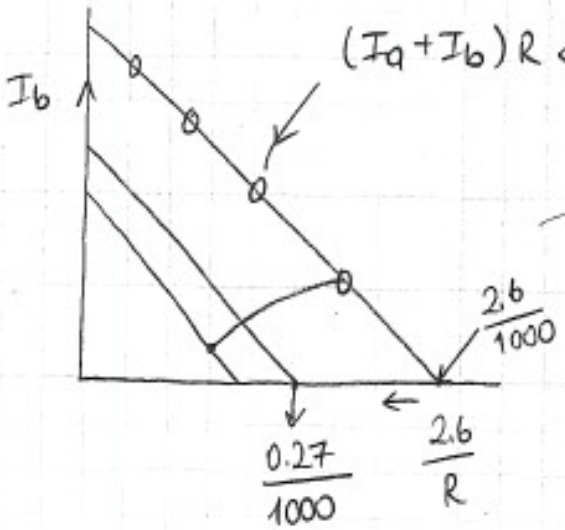
$\Big\}\ I_R < 0.27\ mA$ (Current Comp.)

Then $V_R = I_R \cdot R < 2.6\ V$

$$R < \frac{2.6V}{I_R}$$

$$\downarrow$$

$$R < \frac{2.6}{\max I_R} < \frac{2.6}{I_R}$$



$$R < \frac{2.6}{0.27\ mA} \simeq 10\ k\Omega$$

$R \leq 10\ k\Omega$

V_X = Low

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① $V_{OL}^1 < V_{IL}^2$ (No Voltage comp. Problem)

② $I_R = I_a + I_b$ $\qquad I_R = \frac{5 - V_X}{R}$

$I_a < 20\ mA$ $\qquad I_b < 036\ mA$

(i) $V_X = 0.5\ V$ ⇒ acceptable OL voltage for V_X

$$I_a \leq \frac{5 - 0.5}{R} + 360\ pA \leq 20\ mA$$

$$4.5 \leq (19.4\ mA)\, R$$

$$R \geq \frac{4.5}{19.64}\ k\Omega$$

$$\boxed{R \geq 2200}$$

(ii) $V_X = 0.2\ V$

$$R \geq \frac{4.8}{19.64} \geq 2375\ \Omega$$

Minor changes in V_X does not significantly effect R choice, so select $3 < R < 10\ k$