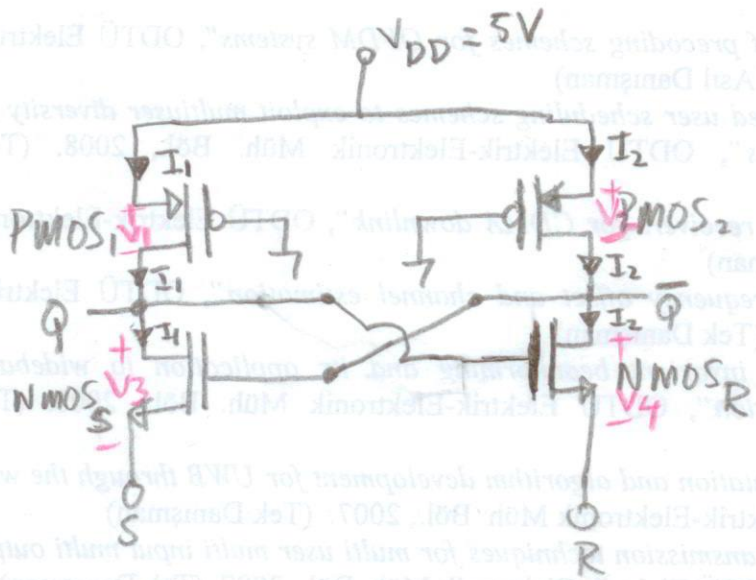
RS Flip-Flop by CMOS gates



$$V_{T_n} = -V_{T_p} = 1V$$

$$K_n = K_p$$

R	S	$NMOS_R$	$NMOS_S$	Q	$\bar{Q}$
		ON	OFF	1	0
0	0	OFF	ON	0	1
0	1	ON [6] $V_4 = 0$	OFF [2] $I_1 = 0, V_1 = 0$	1 [5]	0 [8]
1	0	OFF [2] $I_2 = 0, V_2 = 0$	ON [6] $V_3 = 0$	0	1 [5]
1	1	OFF $I_2 = 0, V_2 = 0$	OFF $I_1 = 0, V_1 = 0$	1	1

Note:
$PMOS_1$ and $PMOS_2$ are always ON.

Notes:

(1): "1" $\equiv V_{DD}$, "0" $\equiv 0$ } high-valued logic.

(2): When both inputs are "0", R=S=0; there exists a third possible operating point which is NMOS transistors in SAT and PMOS in LINEAR. Since $V_Q = V_{\bar{Q}}$ (from symmetry), for this case and this

$$I_1 = \frac{K}{2}\left[V_{\bar{Q}} - 1\right]^2 = K\left[4(5 - V_{\bar{Q}}) - \frac{(5 - V_{\bar{Q}})^2}{2}\right]$$

($V_{SG} + V_{Tp}$; $V_Q = V_{\bar{Q}}$)

$V_{\bar{Q}} = 1 + 2\sqrt{2} \cong 3.82$ Volts

($NMOS_S$: SAT) ($PMOS_1$: Linear). This corresponds to unstable equilibrium point.