32

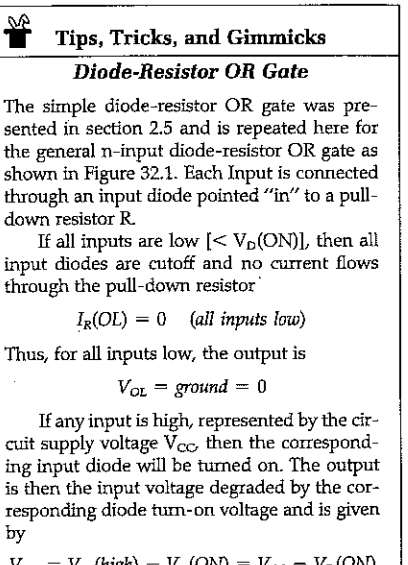
SEMICONDUCTOR READ-ONLY MEMORIES

Diode circuits, BJT circuits, and MOSFET circuits have each been used to provide semiconductor memory circuits consisting of both read-only memory (ROM) and random-access memory (RAM). Random-access memory can be read from and written into and is discussed in the next chapter. This chapter presents read-only memory circuits. Semiconductor IC *read-only* memories refer to ICs or IC sub-circuits that are designed to store a predefined pattern of values. Upon fabrication, this pattern of values is permanently stored and cannot be changed. Hence, such memories can *only* be *read* from and not written into. The predefined pattern of values is stored in a binary format by encoding each logic 0 and 1 into circuitry by the absence or presence of a single diode or transistor.

Semiconductor ROMs have many uses. Entire chips can be designed as ROMs to store a program code such as the boot up code and basic input/output service (BIOS) routines used by computers. IC ROMs can also be used to store operating software for such appliances as VCRs, dishwashers, microwave ovens, and many types of musical equipment. A ROM in the form of an IC sub-circuit can also serve the very useful purpose of a look-up table. That is, decoders requiring many gates and a subsequently higher number of transistors can be replaced with a ROM that requires far fewer transistors.

Special types of ROMs can be programmed *after* fabrication and are referred to as ***programmable read-only memory*** (PROM). As will be seen, programmable ROMs are formed by constructing a fuse in series with a diode or transistor so that all bits have the same logic level upon fabrication of the ROM. The PROM is then programmed by intentionally "*blowing*" the fuse of each bit that is desired to be inverted.

Advancements in semiconductor IC MOS fabrication techniques brought about the possibility of ROMs that could not only be programmed after fabrication but can be erased and later reprogrammed.



Tips, Tricks, and Gimmicks

Diode-Resistor OR Gate

The simple diode-resistor OR gate was presented in section 2.5 and is repeated here for the general n-input diode-resistor OR gate as shown in Figure 32.1. Each Input is connected through an input diode pointed "in" to a pull-down resistor R.

If all inputs are low [$< V_D(ON)$], then all input diodes are cutoff and no current flows through the pull-down resistor

$$I_R(OL) = 0 \quad (all\ inputs\ low)$$

Thus, for all inputs low, the output is

$$V_{OL} = ground = 0$$

If any input is high, represented by the circuit supply voltage V_{CC}, then the corresponding input diode will be turned on. The output is then the input voltage degraded by the corresponding diode turn-on voltage and is given by

$$V_{OH} = V_{IN}(high) - V_D(ON) = V_{CC} - V_D(ON)$$

The diode OR gate provides the basis for a diode ROM cell presented in the following section. The use of Schottky diodes is more practical since $V_{SBD}(ON) < V_D(ON)$.

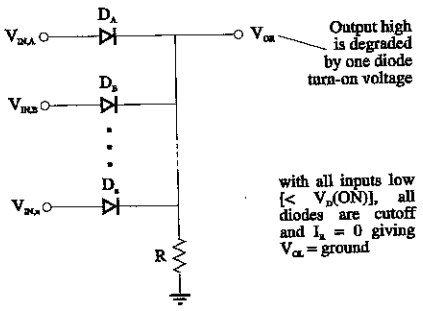


FIGURE 32.1 Simple Diode-Resistor OR Gate

These ROMs are referred to as ***erasable programmable read-only memory*** (EPROM). A subset of EPROMs are the ***electrically erasable programmable read-only memory*** (E^2PROM). The late 1980s brought about a new type of E^2PROM that can be programmed relatively much faster than their predecessors and are referred to as **flash E^2PROMs.**

This chapter presents the details of ROMs based on different approaches using diode-resistor circuits, BJT-resistor circuits, NMOS technology, and CMOS technology. Each of the sections describing the particular approach is self contained and may be studied in any order. The case of CMOS is by far the most important, since this technology is used extensively in today's (1995) ROMs.

32.1 DIODE READ-ONLY MEMORIES

The circuit of Figure 32.2 is a diode ROM cell. This circuit consists of four of the diode-resistor OR gates of Figure 32.1 placed in parallel. Six inputs to the circuit of Figure 32.2 are shared in different combinations as the inputs to the four constituent OR gates. The inputs are labeled V_0, V_1, V_2, V_3, V_4, and V_5. The right most four-input OR gate has inputs V_0, V_1, V_4, and V_5. The next right most OR gate has inputs V_1, V_3, and V_5 and the next (two-input) has inputs V_2 and V_3 and the left most (two-input) OR gate has inputs V_4 and V_5. This circuit represents a simple four bit, six address ROM cell. The data out bit lines are labeled V_{BIT3}, V_{BIT2}, V_{BIT1}, and V_{BIT0}. In all the ROM circuits described, a high voltage is regarded as a 1 and a low voltage as a 0.

Operation of Diode ROM Circuit

Proper operation of the ROM circuit of Figure 32.2 requires that a single input (of the six) be high with all remaining inputs low. Thus, each OR gate has at most one input high, and possibly no high inputs.

V_0 high, all other inputs low
If V_0 is high and all other inputs are low, only the right most OR gate has a high input. The four data out values are then 0, 0, 0, and 1, as indicated to the right of the circuit in Figure 32.2.

V_1 high, all other inputs low
If V_1 is high and all other inputs low, the two right OR gates have high inputs. The four data out values are then 0, 0, 1, and 1.

V_2 high, all other inputs low
If V_2 is high and all other inputs low, the OR gate with output labeled V_{BIT2} has a high input. The four data out values are then 0, 1, 0, and 0.

V_3 high, all other inputs low
If V_3 is high and all other inputs low, the two middle OR gates have high inputs. The four data out values are then 0, 1, 1, and 0.

V_4 High, All Other Inputs Low

If V_4 is high and all other inputs low, the two outer OR gates have high inputs. The four data out values are then 1, 0, 0, and 1.

V_5 high, all other inputs low
If V_5 is high and all other inputs low, only the OR gate with output labeled V_{BIT2} does not have a high input. The four data out values are then 1, 0, 1, and 1.

No Inputs High
It should be noted that if no inputs are high, then none of the parallel OR gates has a high input and all data out values are zero.

Utilization of Diode ROM Circuit

The previous sub-section showed that the circuit of Figure 32.2 can be used as a lookup table of the decimal values 1, 3, 4, 6, 9, and 11. These values are "looked up" by bringing a single input high at a time.

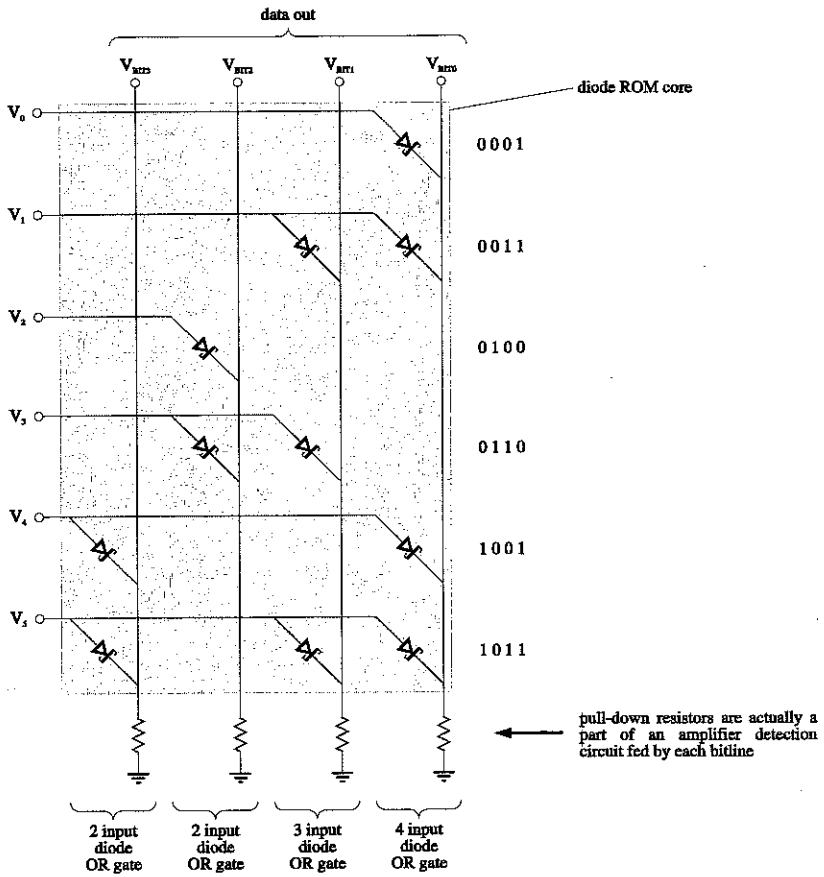


FIGURE 32.2 Diode ROM Cell

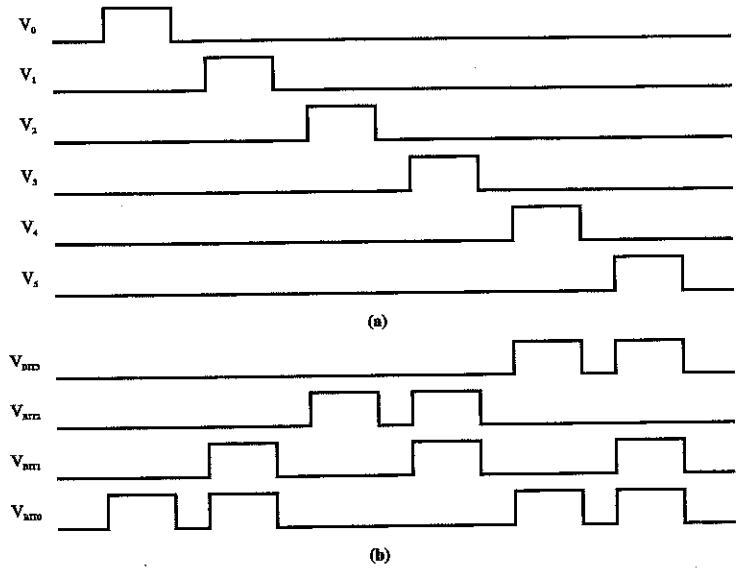


FIGURE 32.3 Addressing Each Row of Figure 32.2 Diode ROM Cell: **(a)** Input stimulus: each input brought high one at a time, **(b)** Resulting outputs

Figure 32.3 shows waveform stimuli to the six inputs in **(a)** and the resulting four outputs are shown in **(b)**. Each input is brought high one at a time and the resulting outputs in base 10 (or base 2) are 1_{10} (0001_2), 3_{10} (0011_2), 4_{10} (0100_2), 6_{10} (0110_2), 9_{10} (1001_2), and 11_{10} (1011_2). These waveforms provide further understanding of the diode-resistor ROM.

Design of a Diode ROM Circuit: *Presence of a Diode Results in a Logic High Output Bit*

Diode ROM circuits of the type in Figure 32.2 can be designed to have any number of data out bits and as many *stored values* as desired. Since the presence of a diode between an input line (row) and an output data bit line (column) results in a logic high.

diode ROM circuits are designed by placement of diodes between input row lines and data out column lines where logic high bits are desired—absence of a diode stores logic low

The portion of the ROM containing the diodes (and lack of resistors) is referred to as the **ROM core.**

PN Junction or Schottky MN Diodes

The circuit of Figure 32.2 specifically shows the use of Schottky diodes in the ROM core. It should be emphasized that these are utilized instead of PN junction diodes because they have a smaller turn-on voltage:

$$V_{SBD}(ON) = 0.3\ V < V_D(ON) = 0.7\ V$$

Pull-Down Resistors Are Part of an Amplifier Sub-Circuit

As discussed in section 2.5 and the *Tips, Tricks, and Gimmicks* box preceding this section, placement of a pull-down resistor is necessary to achieve the logical OR function with diodes. It should be specifically noted here that the pull-down resistors used to complete the realization of each individual OR gate are actually a part of a sense amplifier circuit discussed in section 32.3.

Example 32.1 ***Diode ROM Circuit Design***

Design a diode ROM circuit that has five data out bits and stores the six decimal values 21, 14, 1, 10, 13, and 18. Draw the ROM core of this circuit and use Schottky diodes.

Solution Since a diode ROM circuit stores binary values, the six decimal values must first be converted to binary as in the following table:

Input	Decimal Value	Binary Equivalent
V_0	21_{10}	10101_2
V_1	14_{10}	01110_2
V_2	1_{10}	00001_2
V_3	10_{10}	01010_2
V_4	13_{10}	01101_2
V_5	18_{10}	10010_2

The diode ROM core desired is of the form shown in Figure 32.2 with five parallel diode OR gates sharing different combinations of six different inputs. Figure 32.4 shows a five-bit diode ROM cell with six inputs. A diode is placed between the input (row) line and output bit (column) line in each place a logic 1 is desired. The following example verifies the design of this ROM cell with a SPICE simulation.

Example 32.2 ***SPICE Simulation of Diode ROM Cell***

Verify the design of the diode ROM cell of the previous example with a SPICE simulation.

Solution Figure 32.5 shows the ROM cell of the previous example with pull-down resistors, capacitive loads, piecewise linear voltage sources, and appropriate SPICE labelings. The SPICE input CIRcuit file for this circuit is

```
* Schottky Diode ROM Cell
* 5 Bits, 6 Addresses
.OPTIONS NOECHO NOPAGE NOMOD
+ LIMPTS=300
VA 20 0 PWL(0 0V 10N 0V 11N 5V
+ 90N 5V 91N 0V)
VB 21 0 PWL(0 0V 110N 0V 111N
+ 5V 190N 5V 191N 0V)
VC 22 0 PWL(0 0V 210N 0V 211N
+ 5V 290N 5V 291N 0V)
VD 23 0 PWL(0 0V 310N 0V 311N
+ 5V 390N 5V 391N 0V)
VE 24 0 PWL(0 0V 410N 0V 411N
+ 5V 490N 5V 491N 0V)
VF 25 0 PWL(0 0V 510N 0V 511N
+ 5V 590N 5V 591N 0V)
DA4 20 14 SBD
DA2 20 12 SBD
DA0 20 10 SBD
DB3 21 13 SBD
DB2 21 12 SBD
DB1 21 11 SBD
DC0 22 10 SBD
DD3 23 13 SBD
DD1 23 11 SBD
DE3 24 13 SBD
DE2 24 12 SBD
DE0 24 10 SBD
DF4 25 14 SBD
DF1 25 11 SBD
R4 14 0 2KOHM
R3 13 0 2KOHM
R2 12 0 2KOHM
R1 11 0 2KOHM
R0 10 0 2KOHM
C4 14 0 1PF
C3 13 0 1PF
C2 12 0 1PF
C1 11 0 1PF
C0 10 0 1PF
.MODEL SBD D(IS=7.3E-11
+ VJ=0.5V CJ0=0.05PF EG=0.69
+ XTI=2.0)
.TRAN 2NS 600NS
.PLOT TRAN V(VA) V(VB) V(VC)
+ V(VD) V(VE) V(VF)
.PLOT TRAN V(14) V(13) V(12)
+ V(11) V(10)
.END
```

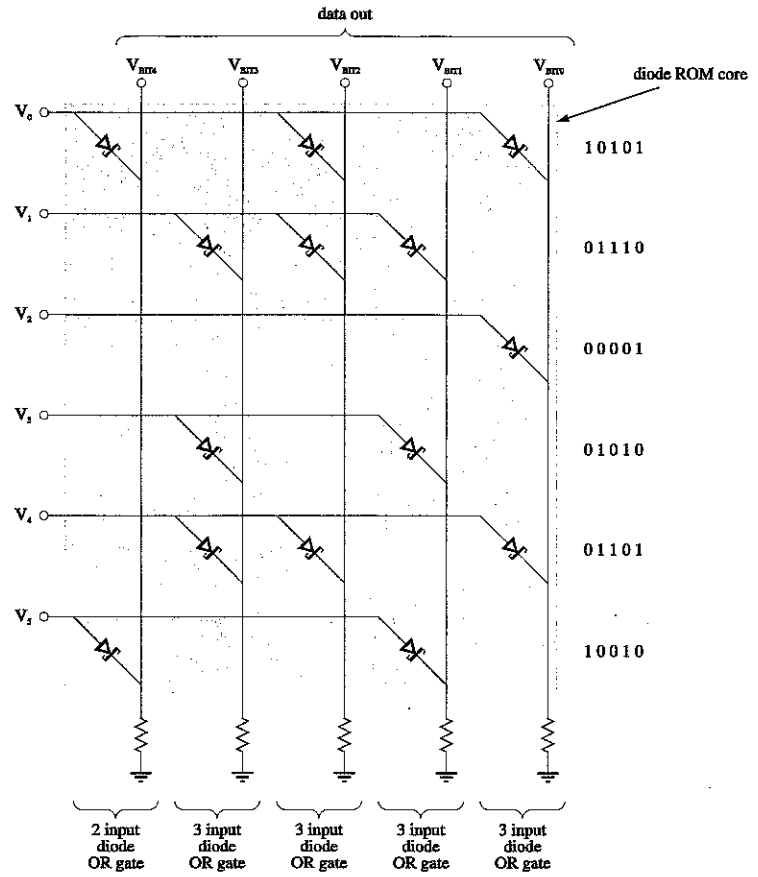



FIGURE 32.4 Diode ROM Cell of Example 32.1

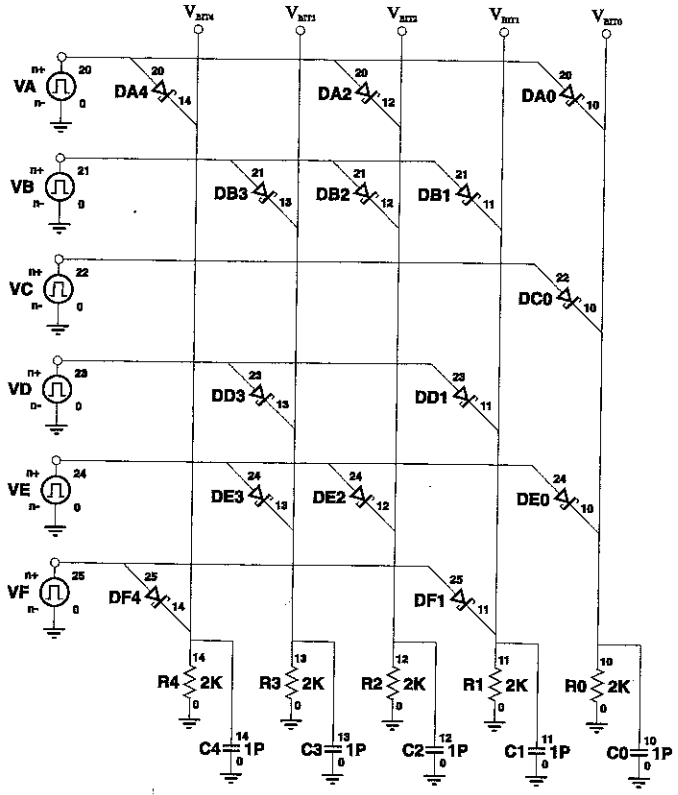


FIGURE 32.5 Diode ROM Cell of Figure 32.4 with Pull-down Resistors, Load Capacitors, and Appropriate SPICE Labelings

Figure 32.6a shows the piecewise linear input voltage stimulus which brings each input high one at a time. The resulting output waveforms shown in Figure 32.6b show that this diode ROM stores the binary values 10101_2, 01110_2, 00001_2, 01010_2, 01101_2, and 10010_2. These correspond to the decimal values 21_{10}, 14_{10}, 1_{10}, 10_{10}, 13_{10}, and 18_{10} asked for in Example 32.1. Thus, the design of the diode ROM in the previous example has been verified.

Example 32.3 ***Analyzing a Diode ROM Core***

Figure 32.7 shows a diode ROM cell that stores 16 six-bit values. Analyze this ROM core to determine the stored values.

Solution Examining each row of the ROM core of Figure 32.7 one at a time, the six-bit binary value stored for each individual input is determined (stated at right). A diode present between the input (row) line and data output bit (column) line represents a stored binary 1 and the absence of such a diode represents a stored logic 0.

The first row has a diode in only the V_{BIT1} column. Thus, the binary value 000010_2 is stored in the first row.

The second row has diodes placed in the V_{BIT1} and V_{BIT0} columns. This represents the binary value 000011_2.

Determining the binary value for each remaining row results in the binary values listed along the right side of Figure 32.7. As can be seen by examining these values, the diode ROM core of Figure 32.7 stores the first 16 prime numbers.

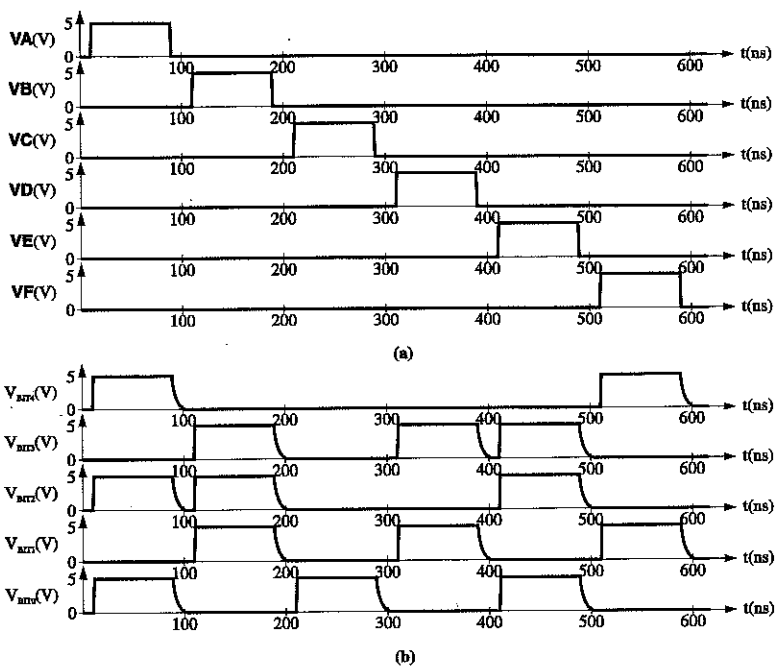


FIGURE 32.6 Results of Example 32.2 Diode ROM Cell SPICE Simulation: (a) Input stimulus, (b) Resulting output waveforms

32.2 BJT READ-ONLY MEMORIES

An alternative to the diode ROM circuits of the previous section is a BJT ROM circuit as shown in Figure 32.9. This circuit is essentially four of the BJT OR gates shown in Figure 32.8b placed in parallel. The six circuit inputs V_0 through V_5 are shared in various combinations as inputs to the constituent OR gates. The three input OR gate with output V_{BIT0} uses inputs V_2, V_4, and V_5. The two input OR gate with output V_{BIT1} uses inputs V_0 and V_3. The four input BJT OR gate with output V_{BIT2} uses the circuit inputs labeled V_1, V_2, V_3, and V_5. Finally, the two input OR gate with output labeled V_{BIT3} uses the circuit inputs V_4 and V_5. This circuit is a four bit, six address, BJT ROM cell.

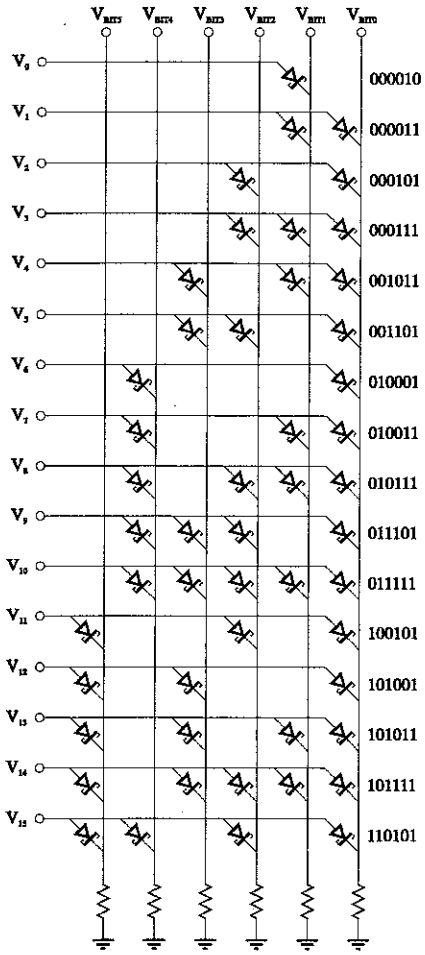


FIGURE 32.7 Diode ROM Cell of Example 32.3

Tips, Tricks, and Gimmicks

Resistor-Transistor Logic (RTL) OR Gate

The resistor-transistor logic (RTL) OR gate is shown in Figure 32.8a. This gate is described in section 5.7. Each input is connected to the base of a BJT through a resistor. The emitters of all BJTs are connected to a common emitter resistor providing output pull-down.

If all inputs are low [$< V_{BE}(FA)$], than all BJTs are cutoff and no current flows through the pull-down resistor. Hence,

$$I_{RE}(OL) = 0 \quad (\textit{all inputs low})$$

Thus, for all inputs low, the output is

$$V_{OL} = \textit{ground} = 0$$

If any input is high (assume a high input voltage is represented by the circuit supply voltage V_{CC}), then its corresponding BJT will be turned on. The output will then be the input voltage degraded by the corresponding BJT forward-active base-emitter turn on voltage, given by

$$V_{OH} = V_{IN}(high) - V_{BE}(FA) = V_{CC} - V_{BE}(FA)$$

This RTL OR gate provides the basis for a BJT ROM cell presented in the following section.

Tips, Tricks, and Gimmicks

An OR Gate is an OR Gate is an OR Gate

The resistor-transistor logic OR gate of Figure 32.8a has been redrawn in Figure 32.8b with the input base resistors removed and the BJTs drawn vertically stacked. This is still an OR gate and will be utilized in the following section drawn in this manner.

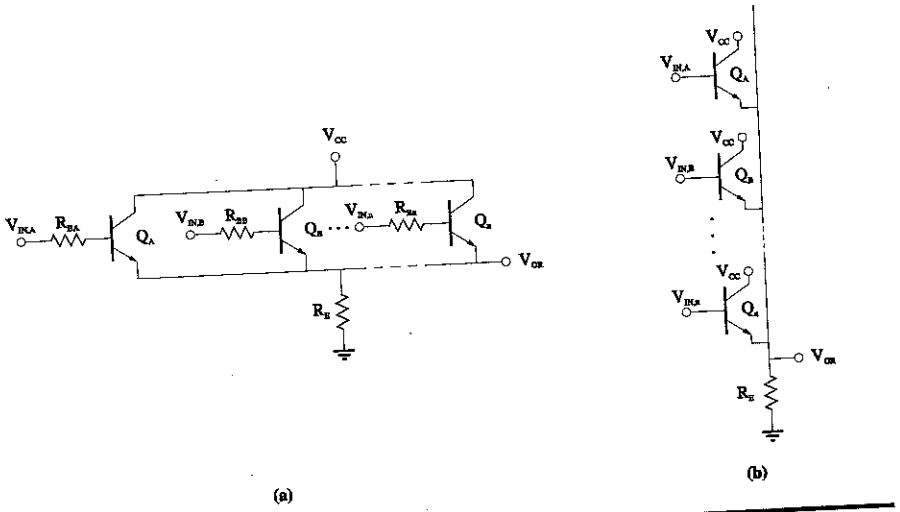


FIGURE 32.8 (a) Resistor-transistor OR gate, (b) Redrawn without input base resistors and BJTs stacked vertically

Operation of BJT ROM Circuit

To operate the circuit of Figure 32.9 so that the binary values stored by this circuitry can be read, a single circuit input (one of V_0 through V_5) should be high with all remaining inputs low. This results in each of the parallel OR gates having at most one of its inputs high and possibly no high inputs.

V_0 high, all other inputs low
If V_0 of Figure 32.9 is high and all other inputs are low, then only the OR gate with output labeled V_{BIT1} has a high input. Thus, the logic levels at the outputs are 0, 0, 1, and 0.

V_1 high, all other inputs low
With input V_1 high and all other inputs low, only the OR gate with output V_{BIT2} would have a high input. The output BIT lines would then have logic values of 0, 1, 0, and 0.

V_2 high, all other inputs low
With the V_2 input high and all other inputs low, the OR gates with outputs V_{BIT0} and V_{BIT2} both have high inputs. This results in out BIT lines with logic values of 0, 1, 0, and 1.

V_3 high, all other inputs low
With input V_3 high and all other inputs low, the OR gates with output labeled V_{BIT2} and V_{BIT1} have high inputs. The resulting BIT line outputs have logic levels of 0, 1, 1, and 0.

V_4 high, all other inputs low
With V_4 high and all other inputs low, the OR gates with outputs V_{BIT3} and V_{BIT0} have high inputs. The output BIT lines will therefore have logic values of 1, 0, 0, and 1.

V_5 high, all other inputs low
With the V_5 input high and all other inputs low, OR gates with output labels V_{BIT3}, V_{BIT2}, and V_{BIT0} have high inputs. The resulting output logic levels are 1, 1, 0, and 1.

No Inputs High
It should be noted that if none of the inputs V_0 through V_5 are high, then none of the four OR gates

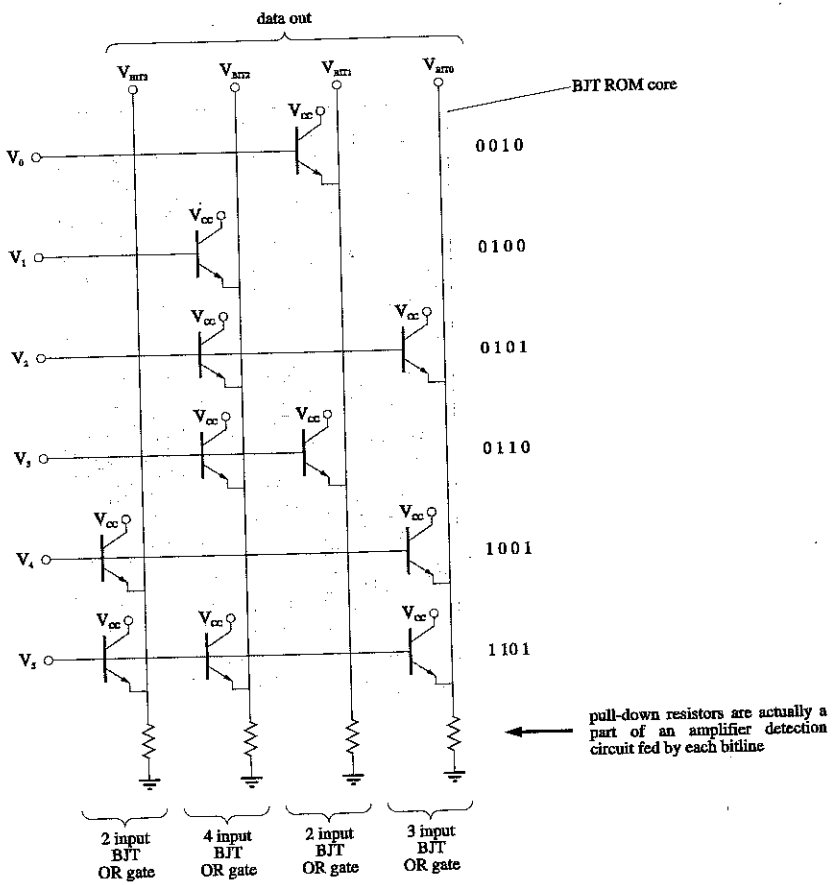


FIGURE 32.9 BJT ROM Cell

has high input and all output BIT lines are at logic level 0.

Utilization of BJT ROM Table

The previous sub-sections showed that bringing each of the circuit inputs high one at a time results in outputs of 2_{10} (0010_2), 4_{10} (0100_2), 5_{10} (0101_2), 6_{10} (0110_2), 9_{10} (1001_2), and 13_{10} (1101_2). Figure 32.10a shows input waveform stimuli to the BJT ROM circuit of Figure 32.9, where each input is brought high one at a time. The resulting output waveforms shown in Figure 32.10b verify the analyses of the previous sub-sections.

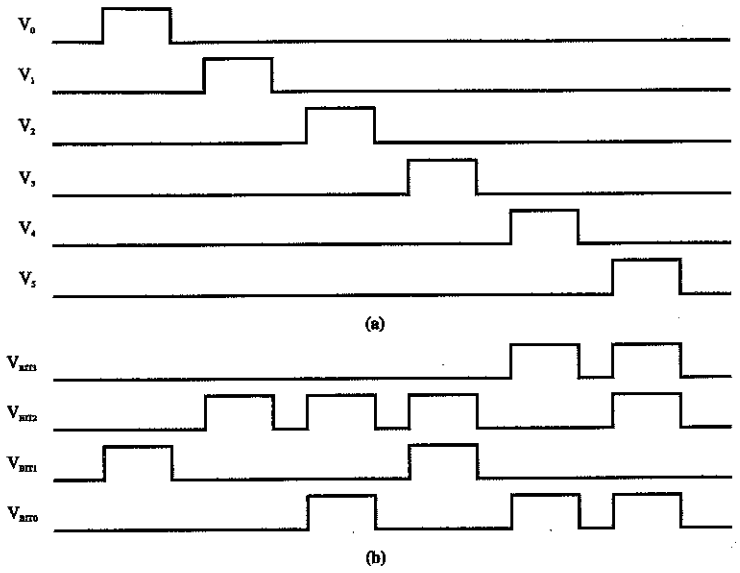


FIGURE 32.10 Addressing Each Row of the Figure 32.9 BJT ROM Cell: (a) Input stimuli: each input brought high one at a time, (b) Resulting outputs

Design of a BJT ROM Circuit: *Presence of a BJT Results in a Logic High*

BJT ROM circuits such as the one exemplified in Figure 32.9 can have any number of output bits with any *stored values* as desired. Storage of a logic 0 or 1 is realized as follows

> *placement of the base-emitter junction of an emitter-follower BJT between an input row line and data output column line results in a stored logic 1—absence of a BJT represents a logic 0*

The portion of the ROM circuit containing the BJTs is referred to as the **ROM core.**

Pull-Down Resistors Are Part of an Amplifier Sub-Circuit

As was the case with the diode ROM circuit of the previous section, the pull-down resistors of the OR gates are actually a part of a sense amplifier circuit used to read the data out value from each BIT line.

Example 32.4 ***BJT ROM Circuit Design***

Design a five bit BJT ROM circuit that stores the decimal values 20, 7, 9, 22, 6, and 24. Draw the BJT ROM core for this circuit.

Solution Since a BJT ROM circuit stores binary values, the decimal values of this example must first be converted to binary as in the following table:

Input	Decimal Value	Binary Equivalent
V_0	20_{10}	10100_2
V_1	7_{10}	00111_2
V_2	9_{10}	01001_2
V_3	22_{10}	10110_2
V_4	6_{10}	00110_2
V_5	24_{10}	11000_2

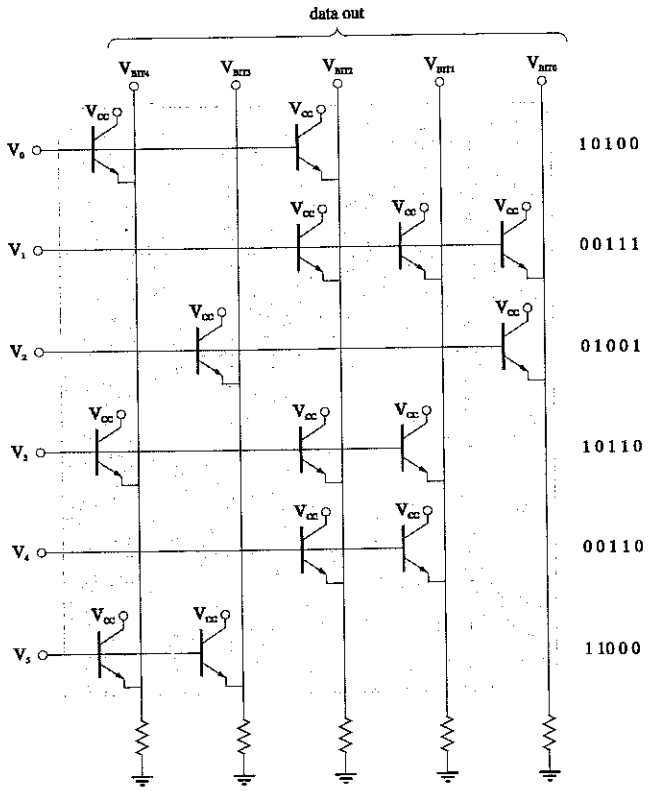


FIGURE 32.11 BJT ROM Cell of Example 32.4

The BJT ROM core needed to store these binary values is made up of five parallel BJT OR gates sharing various combinations of six circuit inputs. Such a five bit BJT ROM core with six addresses is shown in Figure 32.11. The base-emitter junction of a BJT is placed between the input row line and bit column line in each location where a logic 1 should be stored. Absence of a BJT always stores a logic 0. The SPICE simulation of the following example verifies proper design of this ROM cell and generates output waveform patterns for each input brought high one at a time.

Example 32.5 ***SPICE Simulation of BJT ROM Cell***

Perform a SPICE simulation on the BJT ROM cell designed in the previous example to verify that it has stored the desired values.

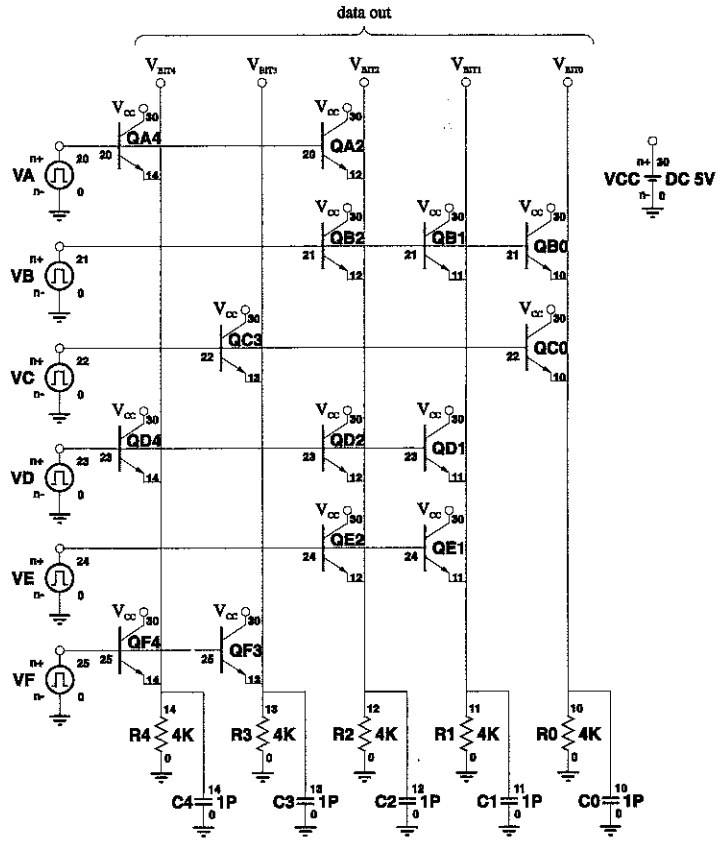


FIGURE 32.12 BJT ROM Cell of Figure 32.11 with Pull-down Resistors, Capacitive Loads, and Appropriate SPICE Labelings

Solution Figure 32.12 shows the BJT ROM cell of the previous example with pull-down resistors, load capacitances, piecewise linear voltage sources, and appropriate SPICE labelings. The SPICE input CIRcuit file corresponding to this circuit is

```
* BJT ROM Cell
* 5 Bits, 6 Addresses
.OPTIONS NOECHO NOPAGE NOMOD
+ LIMPTS=300
VCC 30 0 DC 5V
```