ELSEVIER

Sensors and Actuators A 66 (1998) 218–224

SENSORS AND ACTUATORS A PHYSICAL

An integrated thermopile structure with high responsivity using any standard CMOS process

Tayfun Akin [a,b,*], Zeynel Olgun [a], Orhan Akar [b], Haluk Kulah [a]

[a] Department of Electrical and Electronics Engineering, Middle East Technical University, TR-06531 Ankara, Turkey

[b] TUBITAK-BILTEN, Middle East Technical University, TR-06531 Ankara, Turkey

Abstract

This paper reports a new thermopile structure using n-poly/p$^+$-active layers that are available in any CMOS technology. The thermopile structures are obtained by post-etching of the fabricated and bonded chips. P$^+$-active layers are placed in n-well regions, which are protected from etching by the electrochemical etch-stop technique in a TMAH solution. The n-well regions are then removed using a short EDP etching to reduce the thermal conductivity of the suspended structures, improving the responsivity significantly. The characterization results show that Seebeck coefficients of the n-poly and p$^+$-active layers are -320 ± 15 and 430 ± 20 μV K^{-1}, respectively, resulting in a total Seebeck coefficient of 750 ± 35 μV K^{-1}. A two-arm bridge thermopile test structure results in a responsivity and a detectivity of 49.8 V W^{-1} and 5.75×10^6 cm Hz$^{1/2}$ W^{-1}, respectively, in vacuum when the n-well is removed. © 1998 Elsevier Science S.A. All rights reserved

Keywords: Thermopiles; Infrared sensors; CMOS integration

1. Introduction

Thermopile-type infrared and thermal detectors are used in a number of applications, including infrared spectroscopy, radiometry, security systems and many consumer products. Although they do not provide vision-quality images as in the case of quantum detectors, thermopiles are still attractive for many low-cost commercial and industrial applications, mainly because they do not need cooling for operation and the process technologies are relatively simple.

There have been a number of studies to implement thermopile structures using various conductors, but recently, efforts have been concentrated on implementing them on CMOS-processed wafers and chips with a post-etching process [1–6]. The main advantage of this is the possibility of integrating electronic circuitry with the sensor. Post-etching can be done either from the backside of the wafer with a backside patterning step [1,4] or from the frontside of the wafer without the need for any lithography step [1–3,6,7].

A number of thermopile structures using various layers available in CMOS technology have been presented up to now [1–6]. The most popular one, which is easy to implement, uses the n-poly and aluminium layers that are available in any CMOS process [1,2]. However, use of a p-type material instead of Al almost doubles the total Seebeck coefficient. A possible p-type layer is p-doped polysilicon, and thermopile structures using n-poly/p-poly thermocouples have successfully been implemented [4]. However, the p-doped poly layer is not available in most standard CMOS processes. One other alternative is to use the p$^+$-active layer that is available in every CMOS process. This layer was previously used to implement Al/p$^+$-active thermocouple structures in an n-epilayer [5]. However, this structure does not benefit from the n-poly layer to increase the overall Seebeck coefficient. Another performance reduction comes from the fact that p$^+$-active layers are placed in a thick n-epilayer, which increases the thermal conductivity of the suspended structure, reducing the responsivity of the thermocouple substantially. Recently, a thermopile with n-poly/p$^+$-active layers was implemented with a very high performance; however, the structure was obtained by a custom CMOS process in addition to backside lithography and etching [6], i.e., it is not possible to implement the same structure using a commercial CMOS process.

This paper reports a new thermopile structure with n-poly/p$^+$-active thermocouples implemented using front-end bulk etching in packaged CMOS chips [8]. This structure can be obtained in any standard CMOS technology and provides high responsivity, Seebeck coefficient and detectivity.

* Corresponding author. Tel.: +90-312-210-2369; Fax: +90-312-210-1261; E-mail: tayfun-akin@metu.edu.tr

0924-4247/98/$19.00 © 1998 Elsevier Science S.A. All rights reserved
PII S0924-4247(98)00038-7

2. Thermopile structure

Fig. 1 shows a perspective view of the thermopile with n-poly/p$^+$-active thermocouples. This structure can be implemented in any CMOS process on packaged chips; thermally isolated structures are obtained using frontside bulk etching in tetramethylammonium hydroxide (TMAH) combined with electrochemical etch-stop. Fig. 2 shows a cross-sectional and a top view of the thermopile with n-poly/p$^+$-active thermocouples. Fig. 2(a) shows the cross section of the chip after fabrication in any CMOS foundry. Fig. 2(b) shows the structure after the p-substrate layer under the n-well is etched away; here the etching of the n-well is prevented using the electrochemical etch-stop in a TMAH mixture [9].

After the undercutting of n-well regions, the structure can be used as a thermopile provided that the n-well is reverse biased with respect to the p$^+$-active layer. However, the thickness of the n-well layer is about 3–4 μm in 1.2 μm CMOS technologies, and the thermal conductivity of this relatively low-doped layer is close to that of monocrystalline silicon, which is about 156 W m^{-1} K^{-1}. This is a very high value and increases the thermal conductance between the hot and cold junctions, decreasing the responsivity. The reduction of the thickness of the n-well layer, and preferably its total elimination, improves the responsivity and detectivity significantly. Fig. 2(c) and (d) shows the cross section and the top view of the final n-poly/p$^+$-active thermopile structure after the removal of the n-well.

3. Post-etching details

There are two etching steps to obtain the n-poly/p$^+$-active thermopile structures: first, removal of the p-substrate under the n-well using front-end bulk etching, and then, removal of the n-well. The front-end bulk etching can be done in various anisotropic etchants, like ethylenediamine–pyrocatechol–water (EDP), KOH, or TMAH. In this study, TMAH is chosen, since it is safer and easy to handle compared to the other etchants.

During front-end bulk etching, etching of the aluminium pads needs to be prevented. There are various methods to decrease the etch rate of aluminium in TMAH solutions [9–11]. In this study, the etching is done in a 10% TMAH solution. In order to decrease the aluminium etch rate, 36 g l^{-1} of silicon is dissolved in the solution. Silicon-saturated solution reduces the aluminium etch rate by both decreasing the pH of the solution and forming aluminosilicate at the

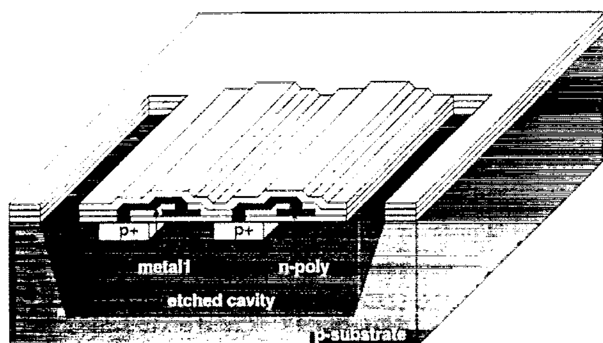

Fig. 1. Perspective view of the thermopile with n-poly/p$^+$-active thermocouples.

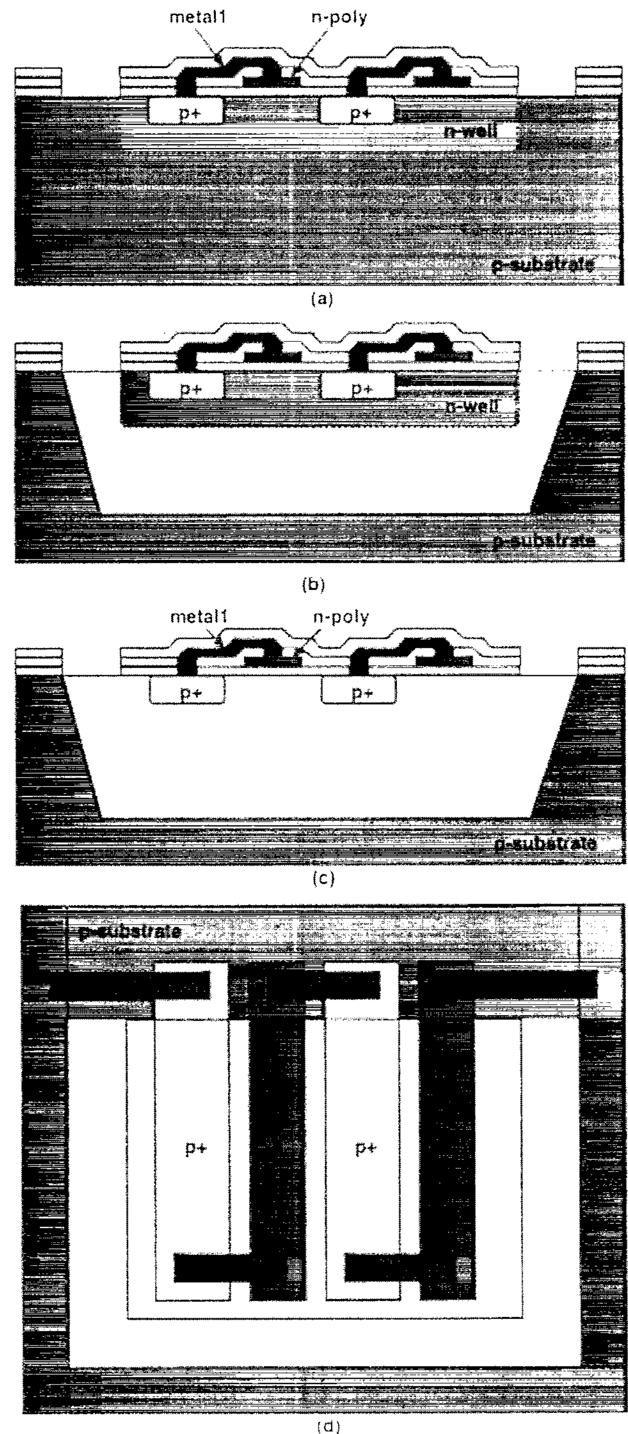

Fig. 2. Cross section of the thermopile: (a) after fabrication in a CMOS foundry; (b) after front-end bulk etching with electrochemical etch-stop on the n-well; (c) after removal of the n-well in EDP or TMAH; (d) top view of the thermopile.

surface of the aluminium pads [9]. This low weight percent TMAH mixture is supposed to provide a high silicon etch rate; however, hillock formation also occurs in low weight percent TMAH, decreasing the etch rate. The addition of ammonium peroxydisulfate to the solution reduces the hillock formation, decreasing the undercut time of the structures [9]. It should be noted here that it is very important to dissolve the ammonium peroxydisulfate fully in the solution, otherwise, undissolved chemical sticks to the bond wires and destroys the pads underneath them.

During this front-end bulk etching, etching of the n-well regions is prevented by using a potentiostat to force −0.5 V to the n-well with respect to a silver/silver chloride (Ag/AgCl) reference electrode. Platinum is used as the counter electrode, and the open-circuit potential for p-doped silicon, i.e., a −1.66 V bias voltage, is applied to the p-substrate with respect to the reference electrode. This type of biasing is called four-electrode biasing [12], and a good etch-stop is achieved with this technique. It should be noted that a small amount of p-substrate is also left under the n-well, increasing the thermal conductance of the suspended structure. However, this does not create any problem if the thin p-substrate layer and n-well are etched away with a subsequent dipping in EDP or TMAH, as explained below.

The second etch step is used to remove the n-well under the p^+-active layer to decrease the thermal conductance of the suspended structure. During this etch, it is important to prevent the etching of the p^+-active layer. According to our measurements and calculations, the p^+-active layer thickness is about 0.3 μm, and the doping level is about 3×10^{19} cm^{-3}, which is at the limit of boron etch-stop in EDP and TMAH [15,16]. Therefore, it is possible to remove the n-well with a short etching in EDP or TMAH without removing the p^+-active layer. In fact, it was possible to remove n-well in a 10 min EDP etch, while the p^+-active layer was preserved in our process. In processes where an etch-stop cannot be achieved due to the low doping level of the p^+-active layer, the pulsed potential anodization technique can be used to protect the p^+-active layer [13].

This 10 min EDP etching is critical for the aluminium pads if standard F-type EDP mixture is used because of its fast aluminium etch rate [18]. However, we have used S-type EDP mixture (1000 ml ethylenediamine, 160 g pyrocatechol, 133 ml water and 6 g pyrazine) at 95°C [18], which has an aluminium etching rate of about 0.18 μm h^{-1} and a silicon etch rate of 30–35 μm h^{-1} [19]. With S-type EDP mixture, it is possible to etch CMOS-fabricated chips for about 2–4 h, depending on the aluminium thickness of the process. However, only a 10 min etching is enough to remove the n-well and protecting p^+-active layer. It should be noted that some care should be taken while rinsing the chip after this short EDP etch to protect the p^+-active lines at the corner regions.

These two etching steps provide n-poly/p^+-active thermopile structures without an n-well. Fig. 3 shows an SEM photograph of the n-poly/p^+-active thermopile after removal of the n-well. Fig. 4 shows a photograph of the bottom of the suspended thermopile structure after the n-well is removed. Note that the picture clearly shows n-poly and p^+-active thermocouple layers. Here also note that the suspended structure is broken to take the picture of the layers and hot-junction contacts of the thermopile.

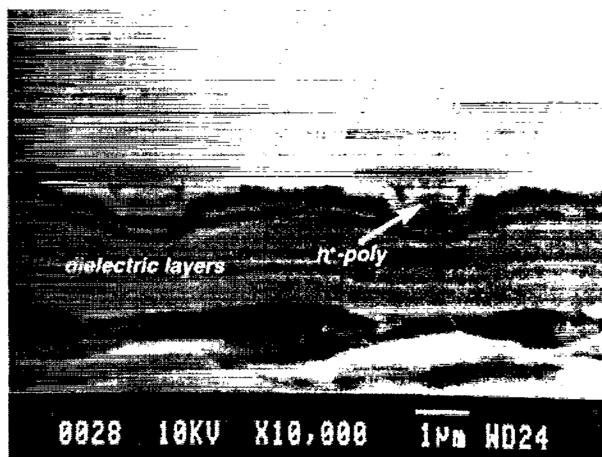

Fig. 3. SEM photograph of the cross section of the n-poly/p^+-active thermopile after the removal of the n-well.

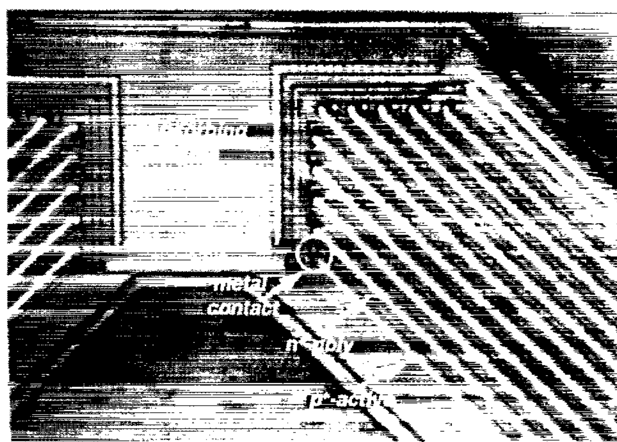

Fig. 4. Photograph of the bottom of the suspended thermopile structure after the removal of the n-well, clearly showing the n-poly and p^+-active thermocouple layers and hot contacts. Note that the suspended structure was broken and flipped upside down to take the picture of its bottom side.

4. Testing and characterization

A test chip has been prepared to determine the thermal characteristics of various layers in the ORBIT HP 1.2 μm process and compare them with the values obtained for the AMS 1.2 μm CMOS process [2,3]. The chip contains three thermopile structures and a number of test structures (similar to the ones in Ref. [3]) to determine the thermal characteristics of the various layers, including the thermal conductivity (κ) and Seebeck coefficient (α).

The TCR value of the polysilicon layer is measured using an n-well/p^+-diffusion diode that is thermally isolated from the p-substrate using the electrochemical etch-stop technique

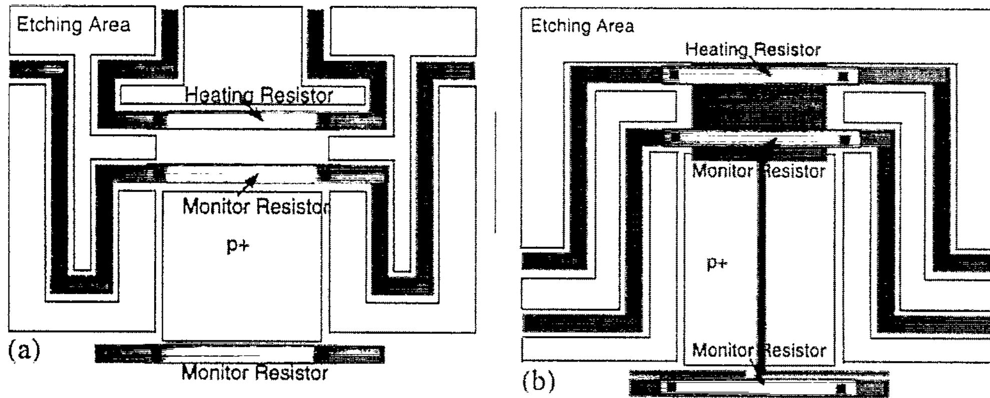

Fig. 5. Schematic top views of the test structures for (a) thermal conductivity; (b) Seebeck coefficient measurements.

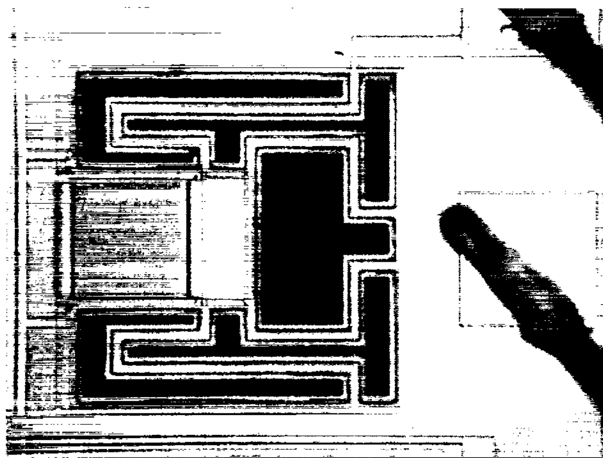

Fig. 6. Photograph of the test structure used for thermal conductivity measurements.

mentioned above. On top of this suspended diode, a heater poly resistance and a monitor poly resistor are placed. After heating the suspended structure with the heater resistor, the temperature of the suspended structure is measured using the diode, while the resistance change in the monitor resistor is also measured. With this test, the TCR of the poly resistance was measured to be 2.1×10^{-3} K^{-1}. After finding the TCR of the polysilicon layer, the thermal sheet resistance and Seebeck coefficients of the various layers were measured.

Fig. 5 shows schematic top views of the test structures used to determine the thermal conductivity and Seebeck coefficients of various layers in the MOSIS HP 1.2 μm process [3,14,17]. In both of the structures there are three heater/monitor resistors. One of the tip resistances is used to heat the tip, while the other one is used to measure the tip temperature. These two resistors are covered with a rectangular metal to distribute the heat emitted from the heater resistor equally on the tip. A third resistor is used to monitor the rim temperature. By monitoring the changes in resistance values and using the TCR value determined above, the temperature differences between the tip and rim are calculated to determine the thermal conductivity and Seebeck coefficients. Fig. 6 shows a photograph of the test structure used for thermal conductivity measurement of the gate polysilicon layer in the MOSIS HP 1.2 μm CMOS process.

Table 1 lists the measured and calculated thermal parameters of the various layers in the MOSIS HP 1.2 μm CMOS process. Due to confidentiality, the exact thickness and doping values of the layers in this process could not be obtained. This has prevented us from determining the thermal parameters of some of the other layers. However, considering other 1.2 μm CMOS processes, we have assumed certain thickness and doping values for various layers in calculating the thermal characteristics of the MOSIS process. The Seebeck coefficient of the gate poly was measured as -320 μV K^{-1}, which is about 2.7 times higher than the value measured for the poly-gate layer of the AMS 1.2 μm CMOS process, i.e., -120 μV K^{-1} [2,3]. However, the thermal conductivity of the gate poly layer in the AMS process is about 30 W m^{-1} K^{-1} [3], which is better than the 54 W m^{-1} K^{-1} that is obtained for the gate poly of the ORBIT process. It is important to note that the Seebeck coefficient of the p^+-active layer is about 430 μV K^{-1}, which is higher than that of the p-poly

Table 1
Measured and calculated electrical resistivity (ρ), thermal conductivity (κ), Seebeck coefficient (α), sheet resistance (R_{sheet}) and thickness (t) of various layers in an ORBIT HP 1.2 μm CMOS process

Layer	ρ (Ω cm)	κ (W m^{-1} K^{-1})	α (μV K^{-1})	R_{sheet} (Ω/square)	t (μm)
n-poly	0.48×10^{-3}	54 ± 1	-320 ± 15	24	0.2
p^+ diffusion	3.6×10^{-3}	75 [a]	430 ± 20	120	0.3
n^+ diffusion	2.1×10^{-3}		-325 ± 15	70	0.3
Total SiO_2	–	7 ± 0.5	–	–	2.2

[a] Estimated value.

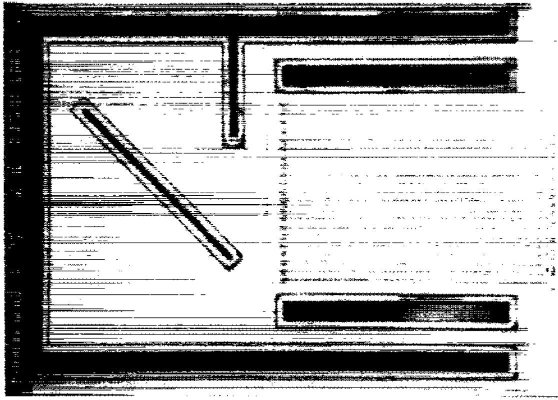

Fig. 7. Photograph of the cantilever-type thermopile with 21 n-poly/p$^+$-active thermocouples. The thermopile measures an area of 406 μm × 275 μm.

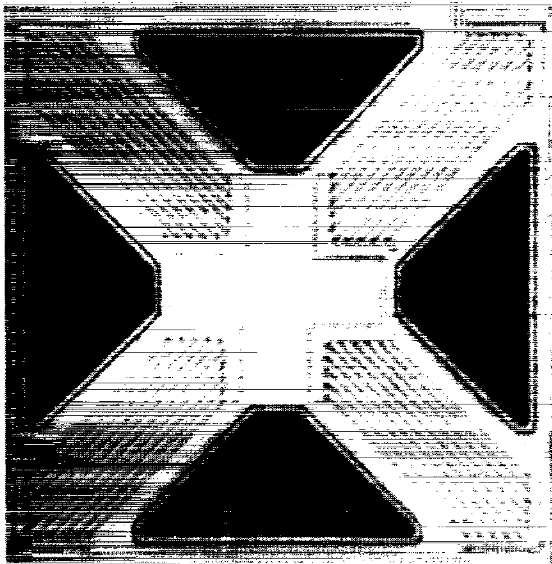

Fig. 8. Photograph of the four-arm bridge-type thermopile with 40 n-poly/p$^+$-active thermocouples. The thermopile measures an area of 325 μm × 325 μm.

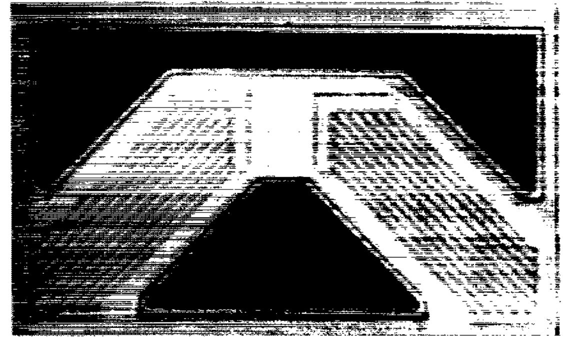

Fig. 9. Photograph of the two-arm bridge-type thermopile with 20 n-poly/p$^+$-active thermocouples. The thermopile measures an area of 325 μm × 180 μm.

layer reported in Ref. [3] (190 μV K^{-1} for the AMS process and 330 μV K^{-1} for the EM process). Besides, a p-poly layer is not available in most CMOS processes. Therefore, the n-poly/p$^+$-active thermocouple structure provides the highest Seebeck coefficient value, 750 μV K^{-1}, i.e., it is the best combination that can be implemented in the CMOS processes without the non-standard p-poly layer.

This test chip also includes three thermopile structures, namely, four-arm bridge, two-arm bridge and cantilever structures. Figs. 7–9 show pictures of these thermopiles, and Tables 2–4 summarize some of their characteristics. The cantilever-type structure provides the highest responsivity considering the measurements when an n-well along with a small amount of p-substrate is present under it. The two-arm bridge structure results in slightly higher responsivity than the four-arm bridge, even though two-arm bridge occupies about half of the area that the four-arm bridge occupies. When the n-well is removed the responsivity of the two-arm bridge increases four times, resulting in a responsivity of 49.8 V W^{-1} in vacuum. The detectivity of the two-arm bridge structure is calculated to be 5.75×10^6 cm $Hz^{1/2}$ W^{-1}, assuming all the power is dropped into the absorbing area. It should be noted here that the responsivity of the detector is expected to

Table 2
Descriptions of the thermopiles in the test chip

Structure	Number of thermocouples	Thermopile resistance (kΩ)	Thermopile size (μm^2)	Absorbing area (μm^2)
4-arm bridge	40	500	325×325	13.6×10^3
2-arm bridge	20	250	325×180	5.6×10^3
Cantilever	21	365	406×275	40×10^3

Table 3
Measured responsivity values (R) of the thermopiles

Structure	R (V W^{-1}) with n-well in air	R (V W^{-1}) with n-well in vacuum	R (V W^{-1}) without n-well in air	R (V W^{-1}) without n-well in vacuum
4-arm bridge	10.2	10.6	39.2	42.4
2-arm bridge	11.7	12.2	44.4	49.8
Cantilever	20.1	20.9 [a]	76.3 [a]	85.6 [a]

[a] Estimated values.

Table 4
Measured detectivity values (D^*) of the thermopiles

Structure	D^* (cm $Hz^{1/2}$ W^{-1}) with n-well in air	D^* (cm $Hz^{1/2}$ W^{-1}) with n-well in vacuum	D^* (cm $Hz^{1/2}$ W^{-1}) without n-well in air	D^* (cm $Hz^{1/2}$ W^{-1}) without n-well in vacuum
4-arm bridge	1.30×10^6	1.36×10^6	5.00×10^6	5.42×10^6
2-arm bridge	1.36×10^6	1.41×10^6	5.15×10^6	5.75×10^6
Cantilever	5.15×10^6	5.35×10^6 [a]	1.95×10^7 [a]	2.19×10^7 [a]

[a] Estimated values.

increase about 14 times according to theoretical calculations when the n-well is removed. However, it only increased four times according to measurements. The same ratio was also observed for the four-arm bridge structure. We think this is partially due to the fact that the simulations were done using the estimated thermal parameters, considering other 1.2 μm CMOS processes. However, the measured thermal parameters were different from the expected values, especially that of silicon dioxide.

The responsivity of the cantilever-type thermopile could not be measured after removing the n-well due to a layout problem. However, by extracting the results obtained from two-arm and four-arm bridge structures, the cantilever structure is expected to provide a responsivity and a detectivity of 85.6 V W^{-1} and 2.19×10^7 cm $Hz^{1/2}$ W^{-1}, respectively, in vacuum when the n-well is removed.

These results show that the cantilever-type thermopile could provide higher responsivity compared with two-arm and four-arm bridge structures. Also, thermopiles made with n-poly/p^+-active layers provide the highest Seebeck-coefficient combination that can be implemented in any standard CMOS process without a non-standard p-poly layer.

5. Conclusions

This paper reports a new thermopile structure using n-poly/p^+-active layers that are available in any CMOS technology. The thermopile structure is obtained with a two-step post-etching of fabricated and bonded chips. In the first step, a frontside bulk etching in TMAH is performed to obtain suspended structures, while the n-well regions that house the p^+-active layers are protected with the electrochemical etch-stop technique. The n-well regions are then removed using a short EDP etching to reduce the thermal conductivity of the suspended structures, improving the responsivity significantly. A test chip was implemented to verify this and to characterize the thermal parameters of various layers in a commercial 1.2 μm CMOS process. Seebeck coefficients of the n-poly and p^+-active layers are measured to be -320 ± 15 and $+430\pm20$ μV K^{-1}, respectively, resulting in a total Seebeck coefficient of 750 ± 35 μV K^{-1}. This is the highest total Seebeck-coefficient combination that can be obtained in any foundry-based standard CMOS process. The test chip contains three thermopile structures. One of these is a two-arm bridge structure, and it provides a responsivity and a detectivity of 49.8 V W^{-1} and 5.75×10^6 cm $Hz^{1/2}$ W^{-1}, respectively, in vacuum when the n-well is removed. We believe that the thermopile structures with n-poly/p^+-active thermocouples described here will provide even higher responsivity and detectivity with optimization of the thermopile design.

Acknowledgements

This research is an extension of the TU-MICROSYSTEMS project, which is sponsored by NATO's Scientific Affairs Division in the framework of the Science for Stability Programme. It is also partially supported by the NSF International grant (ref: INT-9602182), which is provided to Professor Khalil Najafi of the University of Michigan for US–Turkey Cooperative Research on solid-state sensors. The authors would like to thank Professor Najafi, Mr James C.C. Liu and Mr Namik Kemal Kocaman for their help in realization of this study. They would also like to thank Professor G.T.A. Kovacs, Dr E.H. Klaassen and R.J. Reay for their valuable suggestions in electrochemical etch-stop of the packaged chips.

References

[1] A.D. Oliver, W.G. Baer, K.D. Wise, A bulk micromachined 1024-element uncooled infrared imager, Tech. Digest, 8th Int. Conf. Solid-State Sensors and Actuators (Transducers '95/Eurosensors IX), Stockholm, Sweden, 25–29 June, 1995, pp. 636–639.

[2] H. Baltes, O. Paul, Thermal sensors fabricated by CMOS and micromachining, Sensors Mater. 8 (6) (1996) 409–421 MYU Tokyo.

[3] O. Paul, M. Von Arx, H. Baltes, Process-dependent thermophysical properties of CMOS IC thin films, Tech. Digest, 8th Int. Conf. Solid-State Sensors and Actuators (Transducers '95/Eurosensors IX), Stockholm, Sweden, 25–29 June, 1995, pp. 178–181.

[4] R. Lenggenhager, H. Baltes, Improved thermoelectric infrared sensor using double poly CMOS technology, Tech. Digest, 7th Int. Conf. Solid-State Sensors and Actuators (Transducers '93), Yokohoma, Japan, 7–10 June, 1993, pp. 1008–1011.

[5] A.W. Van Herwaarden, D.C. Van Duyn, B.W. Van Oudheusden, P.M. Sarro, Integrated thermopile sensors, Sensors and Actuators A21–A23 (1989) 621–630.
[6] M. Müller, W. Budde, R. Gottfried, A. Hubel, R. Jahne, H. Kuck, A thermoelectric infrared radiation sensor with monolithically integrated amplifier stage and temperature sensor, Sensors and Actuators A 54 (1996) 601–605.
[7] M. Parameswaran, H. Baltes, L. Ristic, A. Dhaded, A. Robinson, A new approach for the fabrication of micromechanical structures, Sensors and Actuators 19 (1989) 289–307.
[8] Z. Olgun, O. Akar, H. Kulah, T. Akin, An integrated thermopile structure with high responsivity and detectivity in any standard CMOS technology, Tech. Digest, 9th Int. Conf. Solid-State Sensors and Actuators (Transducers '97), Chicago, IL, USA, 16–19 June, 1997, pp. 1263–1266.
[9] E.H. Klaassen, R.J. Reay, C. Storment, J. Audy, P. Henry, A.P. Brokaw, G.T.A. Kovacs, Micromachined thermally isolated circuits, Tech. Digest, Solid-State Sensors and Actuators Workshop, Hilton Head, SC, USA, June, 1996, pp. 127–131.
[10] O. Tabata, pH controlled TMAH etchants for silicon micromachining, Sensors and Actuators A 53 (1996) 335–339.
[11] U. Schnakenberg, W. Benecke, P. Lange, TMAHW etchants for silicon micromachining, Proc. 6th Int. Conf. Solid-State Sensors and Actuators (Transducers '91), San Francisco, CA, 24–28 June, 1991, pp. 815–818.
[12] B. Kloeck, S.D. Collins, N.F. de Rooij, R. Smith, Study of electrochemical etch-stop for high-precision thickness control of silicon membranes, IEEE Trans. Electron Devices 36 (4) (1989) 663–669.
[13] S.S. Wang, V.M. McNeil, M.A. Schmidt, An etch-stop utilizing selective etching of N-type silicon by pulsed potential anodization, J. Micromechanical Syst. 1 (4) (1992) 187–192.
[14] P. Van Gerwen, T. Slater, J.B. Chevrier, K. Baert, R. Mertens, Thin-film boron-doped polycrystalline $silicon_{70\%}$–$germanium_{30\%}$ for thermopiles, Sensors and Actuators A 53 (1996) 325–329.
[15] E. Steinsland, M. Nese, A. Hanneborg, R.W. Bernstein, H. Sandmo, G. Kittilsland, Boron etch-stop in TMAH solutions, Sensors and Actuators A 54 (1996) 728–732.
[16] C. Acero, J. Esteve, Chr. Burrer, A. Gotz, Electrochemical etch-stop characterization of TMAH:IPA solutions, Sensors and Actuators A 46–47 (1995) 22–26.
[17] M. Von Arx, O. Paul, H. Baltes, Test structures to measure the Seebeck coefficient of CMOS IC polysilicon, IEEE Trans. Semicond. Manuf. 10 (2) (1997) 201–208.
[18] A. Reismann, M. Berkenblit, S.A. Chan, F.B. Kaufmann, D.C. Green, The controlled etching of silicon in catalyzed ethylenediamine–pyrocatechol–water solutions, J. Electrochem. Soc. 126 (1979) 1406–1415.
[19] R. Lenggenhager, CMOS thermoelectric infrared sensors, Ph.D. Dissertation, ETH, Zurich, Switzerland, 1994.

Biographies

Tayfun Akin was born in Van, Turkey, in 1966. He received the B.S. degree in electrical engineering with high honours from Middle East Technical University, Ankara, in 1987 and went to the USA in 1987 for his graduate studies with a graduate fellowship provided by the NATO Science Scholarship Program through the Scientific and Technical Research Council of Turkey (TUBITAK). He received the M.S. degree in 1989 and the Ph.D. degree in 1994 in electrical engineering, both from the University of Michigan, Ann Arbor. From 1994 to 1995, he was employed as a research fellow in the Department of Electrical Engineering and Computer Science at the University of Michigan. Since 1995, he has been employed as an assistant professor in the Department of Electrical and Electronics Engineering at Middle East Technical University, Ankara, Turkey, and as a consultant at TUBITAK Information Technologies and Electronics Research Institute (TUBITAK-BILTEN). His research interests include analog and digital integrated circuit design, silicon-based integrated microsensors and transducers, microelectromechanical systems (MEMS), infrared detectors and implantable microtelemetry systems and transducers for biomedical applications. Dr Akin was the winner of the First Prize in the Experienced Analog/Digital Mixed-Signal Design Category at the 1994 Student VLSI Circuit Design Contest organized and sponsored by Mentor Graphics, Texas Instruments, Hewlett-Packard, Sun Microsystems and Electronic Design Magazine. In 1996, he received the Research and Encouragement Award, given by Professor Dr. Mustafa N. Parlar Education and Research Foundation for 'his original work in microelectronics and microsensors'.

Zeynel Olgun was born in Aydin, Turkey, in 1973. He received the B.S. degree in electronics engineering from Hacettepe University, Ankara, Turkey, in 1995. Currently, he is pursuing the M.Sc. degree in electrical engineering in the Department of Electrical and Electronics Engineering at Middle East Technical University (METU). Since 1996, he has been employed as a research assistant in the Department of Electrical and Electronics Engineering at METU. His research interests include the design and characterization of CMOS thermopile structures and the implementation of readout electronic interface circuitry for silicon micromachined pressure sensors.

Orhan Akar was born in Samsun, Turkey, in 1972. He received his B.S. degree in electronics and communication engineering from Istanbul Technical University in 1994. Currently, he is pursuing the M.Sc. degree in electrical engineering in the Department of Electrical and Electronics Engineering of METU. Since 1996, he has been employed as a research engineer in TUBITAK-BILTEN. His present research interests include the implementation of MEMS, silicon micromachining and capacitive silicon pressure sensors.

Haluk Kulah was born in Ankara, Turkey, in 1975. He received the B.S. degree in electrical engineering from METU, Ankara, Turkey, in 1996. Currently, he is pursuing the M.Sc. degree in electrical engineering at METU in the area of VLSI design. Since 1996, he has been employed as a research assistant in the Department of Electrical and Electronics Engineering at METU. His research interests include infrared focal plane arrays for night vision applications, analog interface circuits for integrated sensors, MEMS and analog and digital circuit design.