A Bulk-Micromachined Fully Differential MEMS Accelerometer With Split Interdigitated Fingers

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***Abstract*— This paper proposes a novel bulk-micromachined MEMS accelerometer employing split interdigitated sense fingers that provide a fully differential signal interface, where the accelerometer can be fabricated by a modified silicon-on-glass process using a silicon-on-insulator (SOI) wafer. The accelerometer combines the feasibility of fabricating large mass and high aspect ratio structures using bulk-micromachining together with the highly sensitive split interdigitated sense finger triplets that are connected with multilayer metal interconnects on an SOI-glass bonded wafer. The fabricated accelerometer is packaged for system level tests with a fourth-order Σ−Δ readout circuitry to evaluate its performance. The measurement results show that the accelerometer achieves a bias instability of 50 μg and a velocity random walk of 11.5 $\mu g/\sqrt{Hz}$. The accelerometer operates in a range of ±5 g with a nonlinearity of 1140 ppm**

***Index Terms*— Accelerometer, bulk-micromachining, fully-differential detection, split interdigitated fingers.**

I. Introduction

REQUIREMENTS on high end industrial and tactical grade accelerometers in defense and industrial applications are constantly increasing with each passing day. Variations in applications makes accelerometers differ in terms of their sensing mechanism using capacitive [1]–[6], opto-mechanical [7], piezoelectric [8], resonant [9], and piezoresistive [10] methods. MEMS capacitive accelerometers are good candidates for this purpose because of their large scale fabrication capability and reliable features, such as being less prone to temperature variations and easy integration with the electronics. State-of-the-art examples of surface and bulk-micromachined MEMS accelerometers using interdigitated fingers for parallel plate capacitive detection based on gap change exist in the literature [1]–[6], and their common feature is the detection of the acceleration in a fully-differential way. However, because of their inherent nature, surface and bulk-micromachined accelerometers using interdigitated fingers for parallel capacitive detection have certain problems for high performance applications. For example, the fully-differential accelerometers fabricated with Back-End-of-Line (BEOL) processes suffer from buckling problems generated from internal stress of the multi layered metal and dielectric thin films [1], [2]. Besides, they cannot achieve small noise values since the mechanical noise of the accelerometers are inversely proportional to the total proof-mass thickness, which is limited to a few metal and dielectric layers [1], [2]. Another problem of the surface-micromachined accelerometers is their low capacitive sensitivity due to their smaller structural layer. On the other hand, bulk-micromachined accelerometers with silicon proof-mass provide high aspect ratio structures without any buckling [3]. In addition, bulk-micromachined accelerometers have thicker structural layers providing high capacitive sensitivity for the interdigitated finger parallel plate detection, but their gap sizes increased due to the process limitation reducing the advantage of having thicker structural layer for higher sensitivity. This sensitivity depends on the feasible aspect ratios of the gaps. Due to the fabrication difficulty, the current bulk-micromachined accelerometers are implemented with conventional interdigitated fingers. An improvement on the sensitivity of accelerometers can be achieved by implementing the fingers in "split" interdigitated finger configurations, which is easily implemented in surface-micromachined devices. The advantage of having "split" interdigitated fingers was also shown in bulk-micromachined accelerometers with having glass [4] and silicon [5] proof-masses. However, glass as a proof-mass increases process complexity [4]. In addition, using glass as proof-mass results in a smaller mass, as glass is a less dense material than silicon; but small proof masses result in increased mechanical noise. The other approach using the silicon proof-mass in [5] also uses an interdigitated fingers that can be defined as "split" interdigitated fingers, as isolated silicon features anchored to the buried-oxide (BOX) layer. However, in this approach, the accelerometer has small anchor areas, requiring a support provided by polysilicon bridges for a better structural integrity. In addition, this structure uses the silicon handle layer as the supporting substrate, increasing parasitic capacitances of the features located on top of the BOX layer [5].

This work presents a new approach for a bulk-micromachined silicon fully-differential accelerometer that incorporates the high sensitivity "split" interdigitated fingers. The accelerometer provides a high sensitivity and a high signal-to-noise ratio not only due to the low noise of the large silicon proof-mass and the doubled sensitivity of split interdigitated fingers compared to standard comb-type fingers

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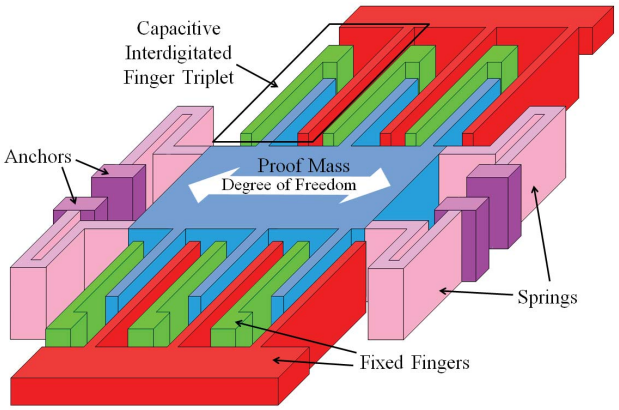

Fig. 1. Capacitive fully differential accelerometer design with split interdigitated finger triplets including inner and outer fixed finger sets.

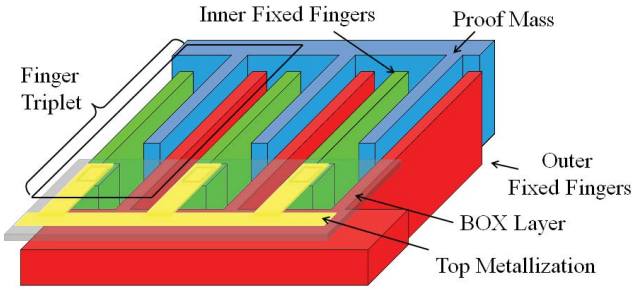

Fig. 2. Contacts from the detached inner finger of the split interdigitated finger triplets are taken from vias through the buried-oxide of the SOI wafer. The contact areas with the silicon are designed to be 10 μm $\times$ 20 μm.

laid in the identical footprint, but also due to the immunity of the fully-differential interface to any common mode noise.

II. Device Design

Fig. 1 shows the generic design of the accelerometer. The proof mass of the accelerometer, which is implemented by the device layer of an SOI wafer, is anchored to a glass substrate by springs and is allowed to move along an in-plane axis. Finger arrays of the accelerometer rest at the sides composed of capacitive split interdigitated finger triplets, which include inner and outer fixed finger sets and proof mass fingers.

The limited anchor area of the inner set fingers prevents taking contacts from the glass side in bulk-micromachined accelerometers. Therefore, carrying contacts through the BOX layer of the SOI wafer is preferred as the appropriate method for the fabrication. Fig. 2 illustrates how electrical connections are made to the inner set of split interdigitated fingers. The BOX layer of the SOI wafer is patterned to form a mechanical bridge on the top surfaces of inner and outer fixed fingers as well as to open the contact windows of detached inner fingers having an area of 10 μm $\times$ 20 μm. On top of the BOX layer, electrical connections of inner fixed fingers are provided with the top metallization. Formed top metallization carries electrical connection of inner fixed fingers to the glass surface via a silicon feed through.

TABLE I
Design Parameters of the Accelerometer

Mass of the proof mass	3.80×10^{-7} Kg
Sensor area	3800 μm $\times$ 2800 μm
Resonant frequency	3135 Hz
Spring Constant	116 N/m
Proof mass thickness	35 μm
Sense finger length	155 μm
Sensing gap	3.00 μm
Sense capacitance	10.0 pF
Capacitance change @ $\pm$5 V bias	80.0 fF
Mechanical Noise	1.8 μg/vHz

III. Fabrication Process and Results

The fabrication of fully-differential accelerometers is based on the modified Silicon-on-Glass (M-SOG) process developed at METU-MEMS Center [11]. The M-SOG process differs from a previous SOG process in the way that MEMS structures are defined before the anodic bonding of the SOI wafer to the glass substrate. This provides the fabrication of micro structures much closer to the design values. The use of SOI wafers allows the selection of optimum proof mass thicknesses with desired electrical properties. In addition, the BOX layer of the SOI wafer not only provides a superior etch stop, but also permits the formation of cross-over electrical connections by isolating the top metal routings from the silicon device layer at the bottom. This study uses an SOI wafer with a 35 μm highly boron doped ($\sim 10^{19}$ cm^{-3}) silicon device layer and a 2 μm-thick BOX layer.

Table 1 shows some of the mechanical design parameters of the accelerometer. The widths of the fixed and moving fingers are chosen conservatively to be 5 μm and 7 μm, respectively. The size of the capacitive gaps is chosen as 3 μm to have a reasonable processing yield. The accelerometer is intended to be working in an operation range of $\pm$16 g.

A. Fabrication Process

A seven-mask process is carried out to fabricate the fully-differential accelerometer. Dry etch techniques are preferred instead of wet etch techniques since the anchor areas of the inner fixed fingers are very small to be exposed to wet oxide etchants. Fig. 3 shows the fabrication steps of the fully-differential accelerometer. The glass substrate is first prepared by wet etching in HF to form the recesses and the anchor points, followed by patterning the deposited Cr/Au layer for the pad metallization (Fig. 3(a)).

The patterned metal on the glass wafer also carries the interconnections of all the inner fixed silicon fingers to their shared bond pad. In the preparation of the device layer, the deep-reactive-ion-etching method (DRIE) is used to obtain high-aspect ratio structures while using the BOX layer as the etch-stop layer (Fig. 3(b)). After that, the glass and SOI wafers are anodically bonded to each other in a vacuum environment (Fig. 3(c)) [12]. The handle layer of the bonded wafer is removed to reach BOX layer from the back side of the SOI wafer (Fig. 3(d)). Reactive-ion-etching (RIE) is then used

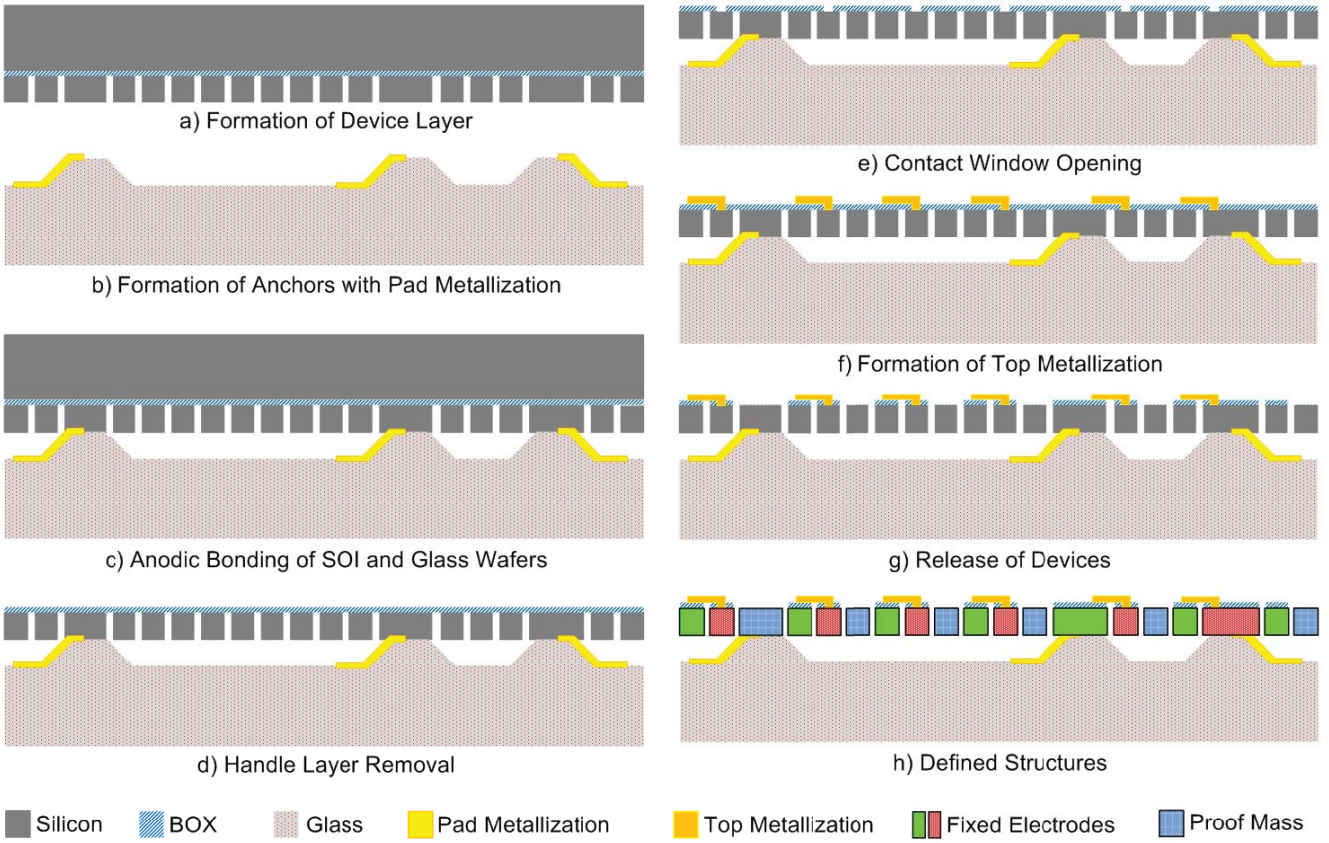

Fig. 3. (a-g) Fabrication steps of the fully differential accelerometer are given and (h) the defined structures sharing the same electrical potential are grouped with same color, where contacts of both fixed fingers and proof-mass are carried onto the glass substrate though the silicon feedthroughs.

to open the contact windows in the 2 μm-thick BOX layer (Fig. 3(e)).

In this step, dry etch is preferred instead of wet etch due to better-controlled etch. Afterwards, Cr/Au metal layers are sputtered and patterned for the formation of top metal routings (Fig. 3(f)).

This process allows achieving split interdigitated finger configurations. The top metal routings reach to the inner set of split interdigitated fingers from the top and merge them on the BOX layer. Top metal interconnects are transferred to the glass surface by using a silicon feedthrough located outside the finger sets. Then successive RIE and DRIE processes are carried out to provide access to the pads located on the glass wafer. Finally, a timed RIE process is performed to etch the BOX layer over the suspended devices, which are then released (Fig. 3(g)).

B. Fabrication Results

Fig. 4 shows a fabricated accelerometer with the finger triplets, and Fig. 5 shows the wiring on the glass. The inner set fingers in every triplet are successfully connected to each other with the top metallization on the BOX layer. No crack is visible on the BOX of the SOI wafer. Thus, an additional supportive layer is defined on small anchored inner fixed fingers. The fabricated capacitive gap size has increased from its design value of 3.00 μm to 3.85 μm due to the lithography and DRIE process tolerances. The gap size is determined according to the mid-plane estimations by averaging the gap lengths measured during the post-lithography inspections of the SOI wafer and post-process SEM measurements of the devices.

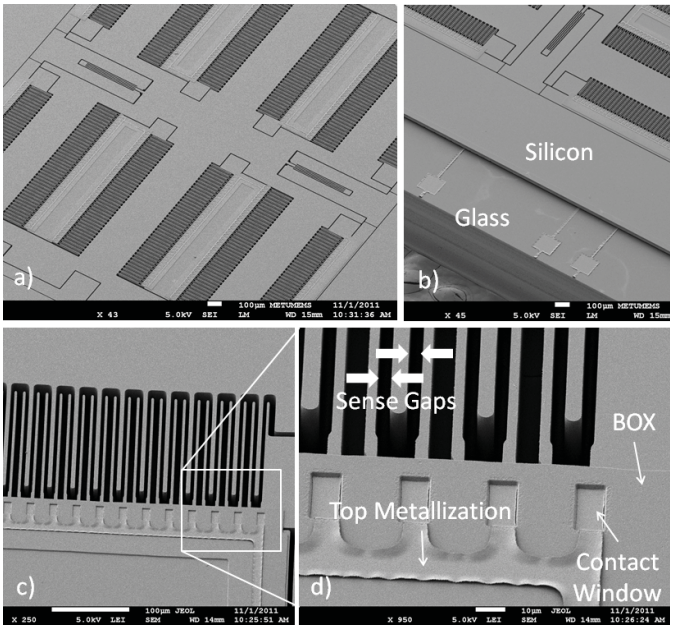

Fig. 4. SEM images of the fabricated accelerometer: (a) general view of the accelerometer, (b) pads belonging to proof mass and fixed electrodes of left side of the accelerometer, and (c, d) close-up views of capacitive finger triplets and constituent layers.

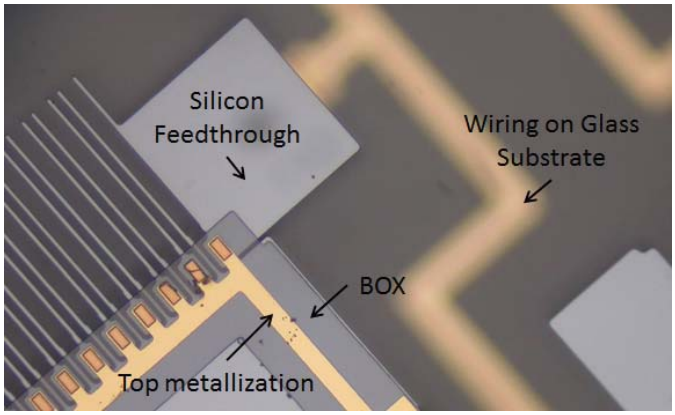

Fig. 5. Top metallization merges the contact of inner fixed fingers over the BOX layer and connects them to the silicon feedthough which carries the connection onto the glass substrate.

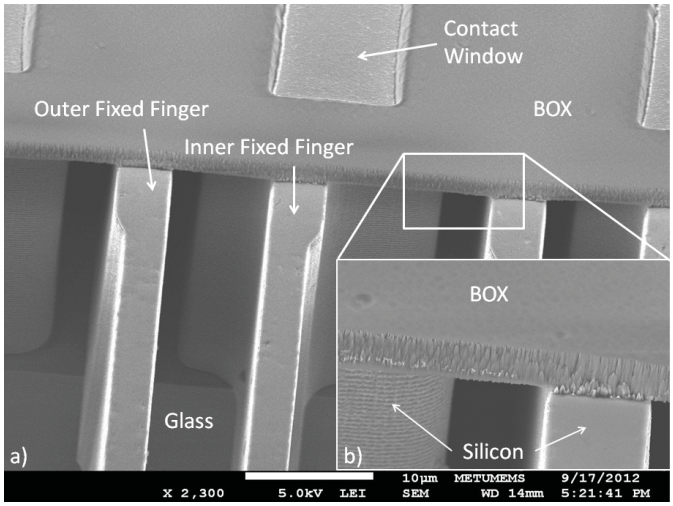

Fig. 6. (a) Split interdigitated fingers are sandwiched between the glass and BOX Layer and (b) etched sidewalls of Silicon and BOX are showing the differences of DRIE and RIE processes.

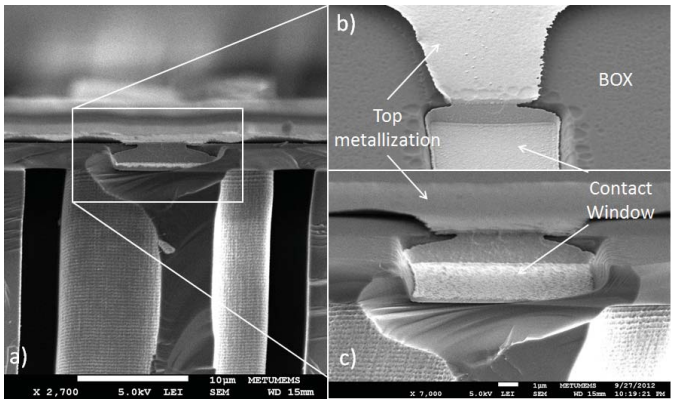

Fig. 7. (a) Cross-sectional SEM image shows the interface between the silicon inner fixed finger-end. (b) and (c) Top metallization carries the connection to the embedded contact window inside the BOX layer stepping down a height of 2 μm. Note that bucking on the top metallization is due to the Oxyen plasma removal of the PR, where Cr adhesive layer is not resilient to plasma etching.

Contact resistance measurement takes place between the proof mass pad and pads of the fixed electrodes. Contact resistances to the inner fixed fingers are measured about 1 kΩ, while resistances of the outer fixed fingers are found to be varying between 220 Ω. Better contact resistances seen at the outer fingers are due to the anodic bonding, while only Cr/Au sputtering takes place for the formation of top metallization on the contact window. The wafer is then subjected to thermal annealing at different temperatures (150 °C, 200 °C, 250 °C) from 30 minutes to 1 hour in order to improve the contact resistances seen at the inner fixed fingers; however, no significant improvement has been observed. In the latter runs, top metallization formation is improved by inserting a short BHF etching step before the metal deposition to remove the native oxide on the silicon surface. The short BHF etch prevents the native oxide behaving as a diffusion barrier, and in turn contact resistance measurements of inner fixed fingers resulted in a resistance of 500 Ω.

Fig. 6 shows the fabricated split intedigitated finger triplets sandwiched between glass substrate and BOX layer. Fig. 7 shows the cross-sectional image of the interface monitoring the contact window and its interface between the silicon and top metallization. At this image poor sidewall coverage over the contact window is visible which can be associated to the over-etching of Cr/Au layers; though this does not pose a problem for the yield. Besides sidewall coverage can be improved by decreasing the steepness caused by the RIE recipe.

IV. Characterization

A. Device Level Tests

Device level tests are performed by obtaining the C-V curve measurement results of the fabricated accelerometers. C-V measurements take place between the electrode(s) and the proof-mass by applying a DC bias to the stator electrode(s) to generate an electrostatic force, and other electrodes are grounded to prevent parasitic capacitances. The generated force pulls the proof-mass towards to electrodes, which results in an increasing change in the capacitance. The tests comprise single electrode measurements as well as multiple electrode measurements which are configured to constitute front-end of the system intended to make the accelerometer work with both half and full-bridge configured read-outs. Fig. 8 shows the test configurations for both cases. Fig. 9 shows the measured C-V curves for single electrode configuration in Fig. 8(a).

A capacitance change of about 70 fF within $\pm$5 V voltage sweep is obtained. Also contact resistances between the proof-mass and the pads are measured. The result of resistance measurements are 510 Ω, 505 Ω, 462 Ω, and 204 Ω for electrodes 1, 2, 3, and 4, respectively.

Fig. 10 shows the I-V curve belonging to the top metallization that is connected to the pad 2. The measurement is done by recording the current with respect to the applied voltage ranging from 10 mV to 2 V. Probing is made between the pad 2 and one of the top metallization that has an electrical connection to the pad 2. The slope of the curve corresponds to a resistance of 405 Ω, which is close to measured contact resistance between the proof-mass and pad 2

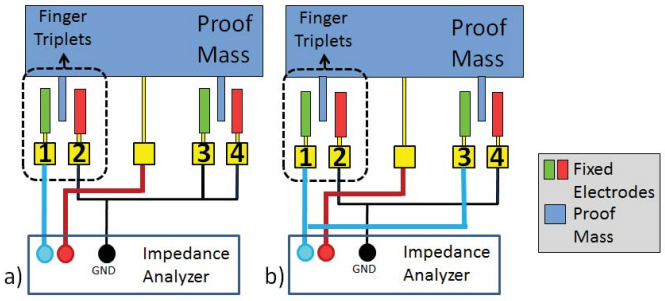

Fig. 8. a) Single and b) multiple electrode test set-up configurations, which will be used for constructing the full and half bridged front-ends, respectively.

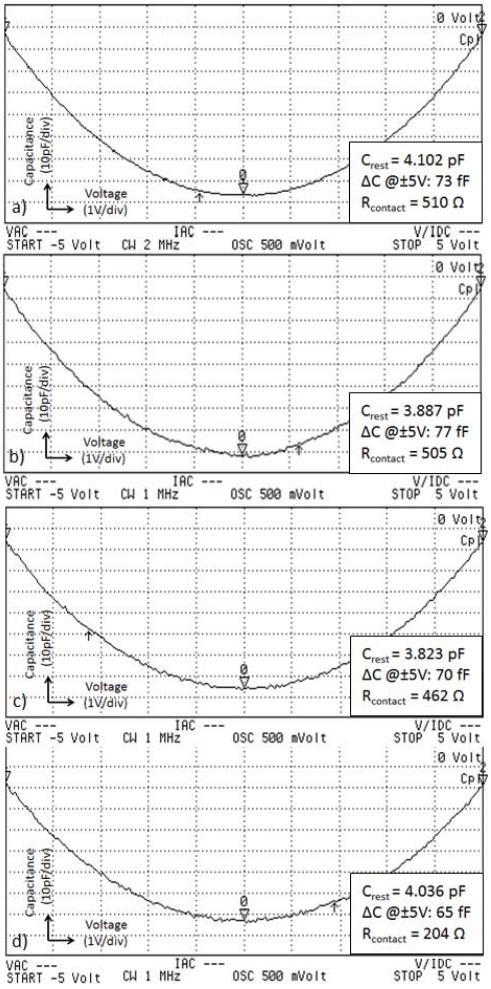

Fig. 9. C-V curve measurements of an accelerometer intended to construct a full-bridge front-end is made. Each single electrode results in a capacitance change about 70 fF at ± 5 V. Internal capacitances of the accelerometer are measured as a) 4.102 pF, b) 3.887 pF, c) 3.823 pF, and d) 4.036 pF, with an error of ±1 fF, for electrodes 1, 2, 3, and 4, respectively. In addition to that contact resistances are measured to be 510 Ω, 505 Ω, 462 Ω, and 204 Ω for electrodes 1, 2, 3, and 4, respectively.

of the accelerometer. Fig. 11 shows the pull-in hysteresis of the accelerometer measured according to the multi-electrode configuration (Fig. 8(b)). The accelerometer enters pull-in at 9.2 V and leaves pull-in at 4.5 V.

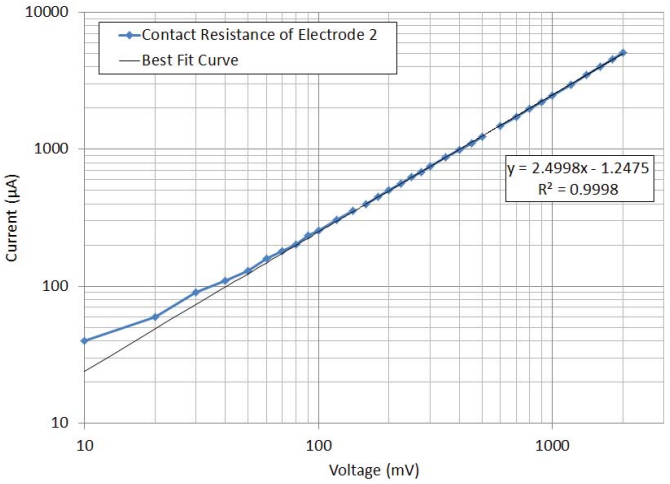

Fig. 10. The I-V curve of the top metallization connected to the pad 2 is plotted. The slope of the curve corresponds to an ohmic resistance of 405 Ω, which is close to the contact resistance given at Fig. 9(b), which is measured between the pad 2 and proof-mass.

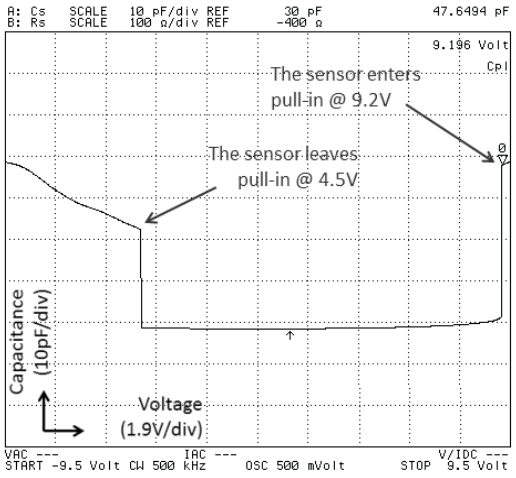

Fig. 11. In the multiple electrode configuration pull-in hysteresis of the accelerometer is extracted, where the accelerometer goes in pull-in at 9.1 V and out at 4.5 V.

B. System Level Tests

System level tests are performed by integrating the accelerometer with two different 4th order Σ-Δ CMOS readout chips CMOS-1 and CMOS-2. The CMOS-1 provides a half-bridge front-end with 10 pF reference capacitances [13], and the CMOS-2 provides a full-bridge front-end similar to [3] providing only half of the rest capacitances, and in turn avoiding the use of reference capacitances. Dividing the accelerometer's capacitance results in a reduced operation range but provides better scale factor linearity due to a better matching between the bridge capacitances. The CMOS-2 also incorporates a serial-to-parallel interface in order to adjust non-adjustable chip parameters in CMOS-1 for the stable operation conditions.

Fig. 12 shows the inside of the accelerometer package with the fully-differential front-end signal interface (Fig. 12(a)). The front-end includes the charge integrating amplifier preceded by the fully-differential half-bridge that is composed

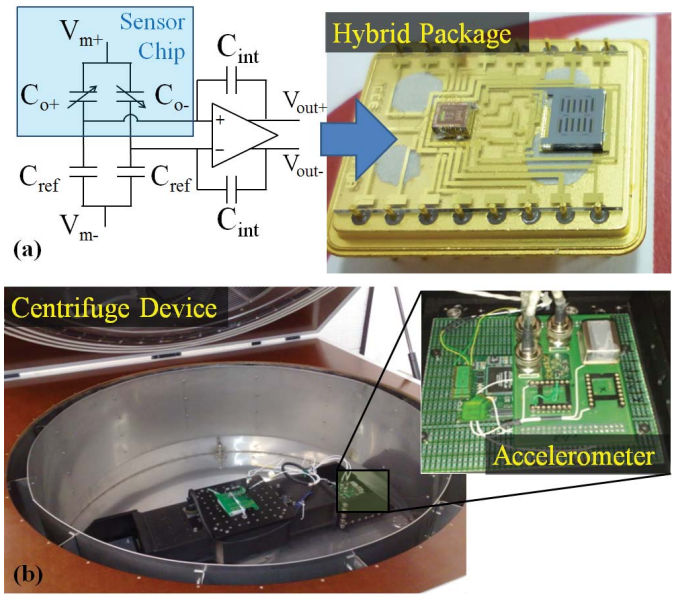

Fig. 12. The accelerometer is (a) hybrid integrated with a fourth-order Σ-Δ readout circuitry and (b) tested with a centrifuge test set-up.

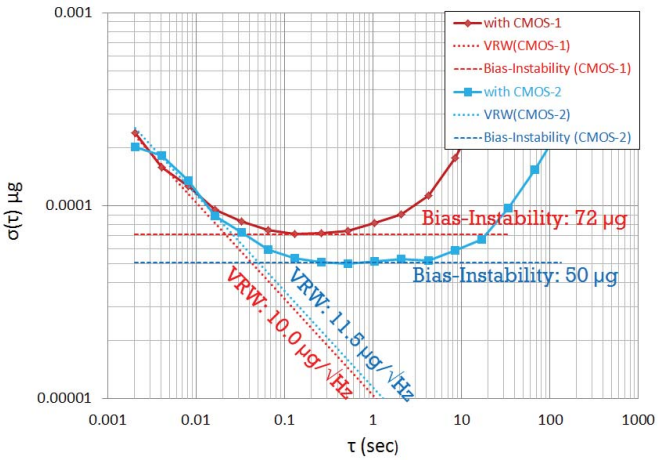

Fig. 13. The accelerometer achieves a bias-instability of 72 μg and a VRW of 10 μg/$\sqrt{}$Hz using CMOS-1; but with CMOS-2 it achieves a VRW of 11.5 μg/$\sqrt{}$Hz and a bias-instability of 50 μg.

of a combination of internal capacitances of the accelerometer and 10 pF on-chip reference capacitances. Operation range tests are conducted inside a centrifuge device set-up which is capable of measuring accelerations up to 20 g (Fig. 12(b)) in one direction. Therefore, accelerometer has to be flipped in the reverse direction to measure the acceleration response in the opposite direction.

C. Noise Test

The noise test is made under the conditions of zero acceleration. Acquired raw data is divided by the scale-factor and processed out using the "Allan Variance" method to plot the deviation (σ) vs. time (τ) graph, where the deviation is calculated from square root of the double-sided PSD of the filtered accelerometer data. The $-1/2$ slope on the plotted data corresponds to the velocity random walk (VRW) noise. The VRW can be multiplied by $\sqrt{2}$ to find the white noise density of the system, since noise-sources of an accelerometer system defined for single-sided PSD. The method also shows how much the accelerometer drifts in bias over the operation time. From the plot the bias-instability of the accelerometer is defined at the point where the slope is zero.

Fig. 13 shows the comparison of the conducted noise tests with CMOS-1 and CMOS-2 choosing an integration capacitance of 1 pF for the closed-loop operation. The first test is made by using the CMOS-1 providing the half-bridge front-end [13], where internal capacitances are set to 8 pF using the hybrid package. In this configuration, VRW and bias-instability of the accelerometer are measured as 10 μg/$\sqrt{}$Hz and 72 μg, respectively.

The latter noise test is performed with the full-bridge configuration using CMOS-2 by separating the accelerometer capacitance values to 4.1 pF and 3.9 pF. A similar VRW value of 11.5 μg/$\sqrt{}$Hz is obtained; but a small improvement is observed in terms of bias-instability from 72 μg to 50 μg. The measured noise value is much higher than the estimated mechanical noise of the accelerometer given in "Table I". According to (1) the closed-loop system's overall noise is dominated by the electronic component, since the correlation between the two noise sources is zero [6].

$$n_{system} \cong \sqrt{n_{mechanical}^2 + n_{electronic}^2} \tag{1}$$

D. Centrifuge Tests

The centrifuge tests are performed to determine the operation range of the accelerometer as well as the non-linearity. Both accelerometers are subjected to the centrifuge test. An operation range of $\pm$20 g is measured with the first read-out CMOS-1 indicating that closed-loop operation is not functional due to low loop-gain when an integration capacitance of 10 pF is chosen. Therefore, the loop-gain is increased for a closed-loop operation by changing the integration capacitance from 10 pF to 1 pF. The 1 pF is the value where best noise performance is obtained; however no significant contribution exists to the non-linearity. Fig. 14 shows the comparison of both residual non-linearity values for the same operation range.

The residual non-linearity is defined as the difference between the measured digital output data of the centrifuge test device and the linear least squares best fit; but it is measured separately for the positive and negative accelerations since an offset in the bias exists due to the misalignment of the accelerometer to the package.

According to the results, the accelerometer achieves a closed-loop operation range of $\pm$10 g with CMOS-1, and it is less than the intended $\pm$ 16 g. The reduction in the range is due to the small sensitivity, which is due to the larger gap than intended in the fabrication. The test with 10 pF integration capacitance resulted in a non-linearity of 24 823 ppm, while the tests with 1 pF integration capacitance resulted in a non linearity of 42 026 ppm. In comparison non-linearity is at the order of tens of thousands ppm levels, and does not improve by changing the integration capacitance.

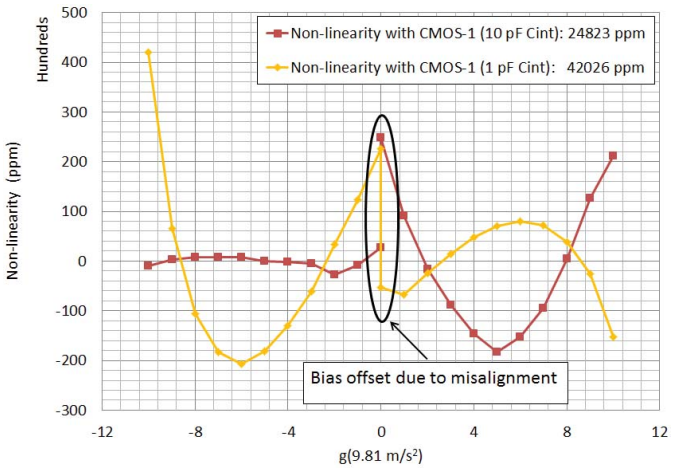

Fig. 14. Centrifuge test of the accelerometer with CMOS-1 results in an operation range of ±10 g and a non-linearity of 24 823 ppm for the operation with 10 pF C_{int} and 42026 ppm with 1 pF C_{int}.

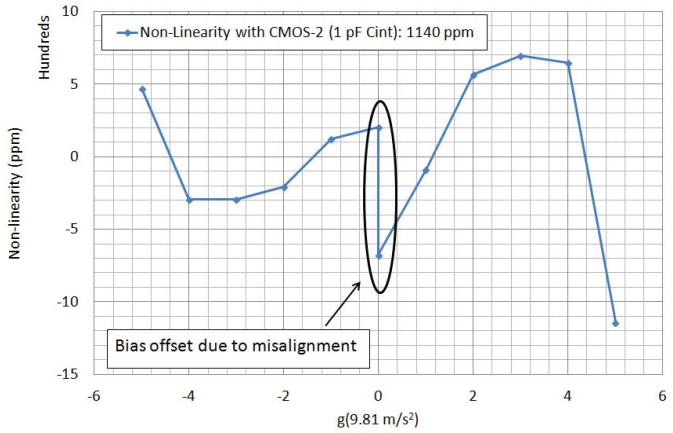

Fig. 15. Centrifuge test of the accelerometer with CMOS-2 results in an operation range of ±5 g and a nonlinearity of 1140 ppm for the operation with 1 pF C_{int}.

TABLE II
MEASURED PERFORMANCE RESULTS OF THE FULLY-DIFFERENTIAL ACCELEROMETER

	With CMOS-1	With CMOS-2
Operation range (g)	±10	±5
VRW (µg/vHz)	10.0	11.5
Bias instability (μg)	72	50
Non-linearity (ppm)	42 026	1140

On the other hand, test with CMOS-2 resulted in a non-linearity of 1140 ppm, which is at least 40 times better than the one tested with CMOS-1 for the same integration capacitance. In return, operation range of the accelerometer is halved to ±5 g since the rest capacitances are wired accordingly to form a full-bridge signal interface. Fig. 15 shows the non-linearity of the accelerometer tested with 1 pF integration capacitance. On the left side where negative accelerations are present, non-linearity is 470 ppm and smaller than the offset coming from the mounting of the accelerometer. Table 2 summarizes the performance results of the accelerometer.

V. CONCLUSION

A bulk-micromachined fully-differential accelerometer has been demonstrated employing split interdigitated fingers, which are fabricated with an SOI wafer on a glass substrate. The buried-oxide layer of the SOI wafer is used for isolation between the differential signals paths of inner and outer fixed finger sets as well as a means for additional mechanical support.

The tests with full-bridge configured read-out CMOS-2 presents a better performance than the half-bridge configured CMOS-1 especially in terms of non-linearity. Test with CMOS-1 resulted in a non-linearity of 42 026 ppm, while test with CMOS-2 resulted in a non-linearity of 1140 ppm. Noise floor of the accelerometer does not change with the signal interface; but bias-instability can also be improved further with the full-bridge configuration from 72 μg to 50 μg. The only drawback is the halved operation range from ±10 g to ±5 g.

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