A Monolithic Phased Array Using 3-bit Distributed RF MEMS Phase Shifters

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***Abstract*—This paper presents a novel electronically scanning phased-array antenna with 128 switches monolithically implemented using RF microelectromechanical systems (MEMS) technology. The structure, which is designed at 15 GHz, consists of four linearly placed microstrip patch antennas, 3-bit distributed RF MEMS low-loss phase shifters, and a corporate feed network. MEMS switches and high-Q metal–air–metal capacitors are employed as loading elements in the phase shifter. The system is fabricated monolithically using an in-house surface micromachining process on a glass substrate and occupies an area of 6 cm $\times$ 5 cm. The measurement results show that the phase shifter can provide nearly 20°/50°/95° phase shifts and their combinations at the expense of 1.5-dB average insertion loss at 15 GHz for eight combinations. It is also shown by measurements that the main beam can be steered to required directions by suitable settings of the RF MEMS phase shifters.**

***Index Terms*—Microelectromechanical systems (MEMS), micromachining, microwave, phased array, phase shifter.**

I. Introduction

OVER THE past decade, RF microelectromechanical systems (MEMS) technology has offered solutions for the implementation of novel components and systems [1], [2]. This technology promises to solve many limitations of other technologies, especially for high-frequency applications. RF MEMS enables the realization of reconfigurable components such as switches, capacitors, and phase shifters with low insertion loss, low power consumption, and high linearity compared to the conventional techniques. One of the important components of the RF MEMS technology is to implement RF MEMS phase shifters for phased-array applications that require better performance than the arrays with conventional phase shifters in terms of losses and size.

Phased arrays consist of multiple stationary radiating elements each of which are fed by tunable phase or time-delay control units to steer the beam [3], [4]. Phased arrays are generally implemented using separately produced components such as a feed network, phase shifters, and antennas. Hybrid connection of these components not only increases the system size, but also introduces parasitic effects, packaging cost, and losses. In order to eliminate these drawbacks, there is a need to produce these components on the same substrate, forming a monolithic phased array, which is possible with the enabling RF MEMS technology [5], [6].

This paper presents a novel monolithic electronically scanning array using the RF MEMS technology. The phased-array system in this study is designed to operate at 15 GHz, and it employs 3-bit distributed MEMS transmission line (DMTL) type phase shifters. These phase shifters are monolithically integrated with the feed network and four linearly placed microstrip patch antennas on the same substrate [6]. The use of MEMS phase shifters in a phased array offers some advantages. First, MEMS phase shifters have low-loss performance with nearly zero dc power consumption compared to semiconductor-based counterparts [7], [8]. Moreover, MEMS phase shifters are suitable for monolithic phased-array designs with their reduced cost and volume compared to semiconductor- and ferrite-based counterparts. The phase shifters in the phased array presented in this study are used to obtain various combinations of progressive phase shift in the excitation of radiating elements to steer the beam. In this study, phase-shifter performance is improved using high-Q metal–air–metal (MAM) capacitors in addition to MEMS switches. Furthermore, the system losses and size are reduced by implementing the RF MEMS phase shifters in a phased array monolithically manufactured by micromachining technology. To the authors' knowledge, this study is one of the first few monolithically fabricated electronically scanning phased-array systems employing a large amount of RF MEMS components reported in the literature [5], [6]. Section II gives the configuration of the electronically scanning array, while Section III presents the design, implementation, and measurement results of the low-loss MEMS phase shifter used in the phased array. Section IV provides the fabrication and measurement results of the array, which is followed by conclusions in Section V.

II. Phased-Array Structure

The phased array proposed in this paper is composed of four microstrip patch antennas, a corporate feed network, and four RF MEMS phase shifters. The operation frequency is selected as 15 GHz to be able fit the entire system into a single 500-μm-thick 4-in glass substrate ($\varepsilon_r = 4.6, \tan\delta = 0.005$). The total size of the system is approximately 6 cm $\times$ 5 cm. The device is fabricated using the surface micromachining process developed at the Middle East Technical University (METU), Ankara, Turkey. Fig. 1 presents a layout and photograph of

Manuscript received April 26, 2007; revised October 4, 2007. This work was supported by The Scientific and Technical Research Council of Turkey (TUBITAK-EEEAG-104E041), by the Turkish State Planning Organization (DPT), and by the AMICOM (Advanced MEMS For RF and Millimeter Wave Communications) Network of Excellence under the 6th Framework Program of the European Union.

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Digital Object Identifier 10.1109/TMTT.2007.914377

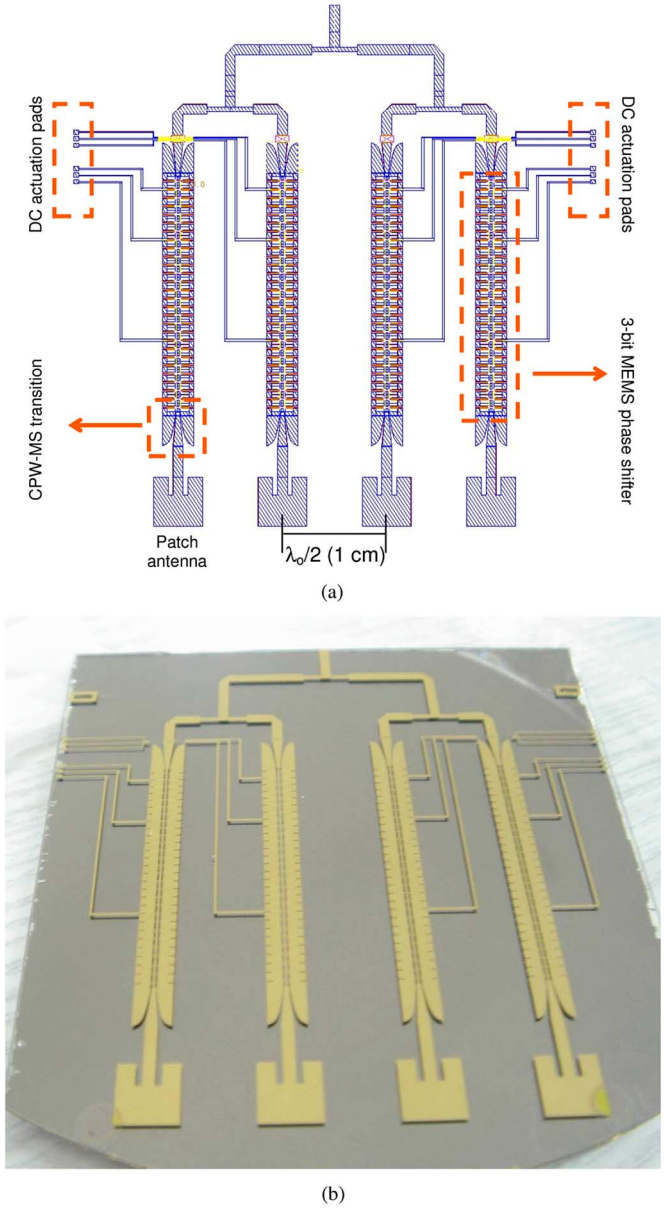


Fig. 1. Proposed monolithically integrated phased array. (a) Layout drawing and (b) photograph of the fabricated device. The device is fabricated using an in-house surface micromachining process. The total chip size is approximately 6 cm × 5 cm.

the monolithically integrated phased array. Microstrip patch antennas having dimensions of 4.65 mm × 4.65 mm are equally spaced by $\lambda_o/2$ (1 cm) distance from each other's phase center. A corporate feed network, which is composed of 70 Ω ∼ $\lambda_o/4$ (2.2 mm) transformers, is optimized at around 15 GHz. The width of 50- and 70-Ω lines are 0.95 and 0.43 mm. Tapered lines with low return loss are required for the transitions from microstrip lines to conductor backed coplanar waveguide (CB-CPW) since RF MEMS phase shifters are implemented on CB-CPW. These phase shifters are designed to provide progressive phase shifts of 45°/90°/180° and their combinations at 15 GHz. When both the array factor and element pattern are taken into account, the 3-dB beamwidth of the array is 25°, and the main beam can be rotated to approximately 12° and 24° for progressive phase shifts of 45° and 90°, respectively. Progressive phase shifts of 135° and 180° can also be provided by the phase shifter; however, the main beam cannot be steered to the corresponding scan angles due to the element pattern.

III. Digital Phase Shifter Using MAM Capacitors

Most phase shifters currently being used in phased arrays are based on ferrite or semiconductor devices such as p-i-n diodes or field-effect transistor (FET) switches. Ferrite-based phase shifters are generally used in arrays where a low insertion loss is required (∼1 dB) and slow-switching time (150 μs) is permissible [9], [10]. However, these phase shifters are not suitable for the implementation of low-profile and low-weight phased arrays. FET-based phase shifters consume very low power, but they have a large amount of RF loss (4–6 dB at 12–18 GHz) [11]. p-i-n diode-based phase shifters consume more dc power and have slightly better performance compared to FET-based phase shifters [12], [13]. However, the semiconductor device-based phase shifter cannot compete with the loss performance of the MEMS-based phase shifter, which has been shown with various designs [1]. MEMS phase shifters are designed using switched line [7], [8] or distributed loaded line [14]–[19] approaches. Switched line phase shifters are implemented using MEMS switches on microstrip transmission lines. These phase shifters either require via-holes for series switch configuration, increasing the fabrication complexity [7], or radial stubs for shunt switch configuration, limiting the bandwidth of the phase shifter [8]. Among the MEMS phase shifters, the ones designed using distributed techniques, namely, DMTL, offer wideband and low-loss cascadable devices with a simple design and fabrication method on relatively low-permittivity substrates such as quartz ($\varepsilon_r = 3.8$) and glass ($\varepsilon_r = 4.6$). These low-permittivity substrates also allow the implementation of radiators monolithically integrated with the phase shifters. Therefore, the monolithic phased-array structure in this study employs a phase-shifter structure designed using distributed techniques.

The reason for low-loss characteristics of a MEMS phase shifter is that the MEMS switches used in the implementation of a DMTL have a very low series resistance (0.1–0.3 Ω) compared to solid-state devices [14]–[19]. The average loss of a typical 3-bit MEMS phase shifter is 1.2 dB at 13.6 GHz [17], which is a 3–4-dB improvement compared to designs using GaAs FET switches. This leads to an improvement of 6–8 dB in the insertion loss of a radar system. Therefore, one of the amplifier stages can be removed from the system, reducing both dc power consumption and manufacturing costs of the system.

A. Phase-Shifter Design

The digital phase shifter used in the system is composed of a periodically loaded high-impedance transmission line ($Z_o > 50\ \Omega$) with MEMS bridges in series with lumped capacitors forming a DMTL [15]. Fig. 2 shows a general view of the phase shifter and its unit cell. Fig. 3 gives the corresponding circuit model of the unit cell, which provides the required closed-form expressions. The unit cell has two states for the bridge: the up position and the down position. The total loading capacitance when the MEMS bridge is in the upstate position is the series combination of two capacitors: C_{bu} and C_s. As the bridge is

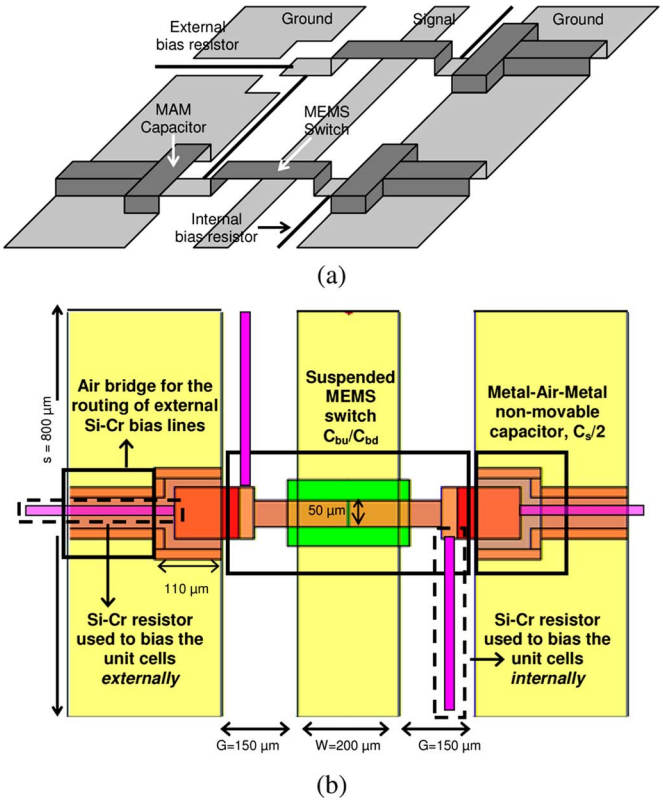


Fig. 2. (a) Phase-shifter structure. The air bridge on the external resistor is removed in the drawing for better visualization. (b) Top view of the unit cell of the phase shifter showing the dimension.

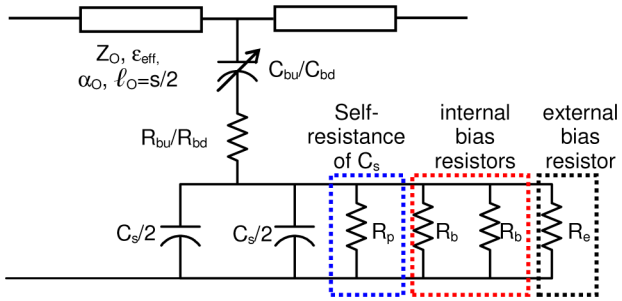


Fig. 3. Circuit model for the unit cell of the phase shifter.

actuated by applying a dc-bias voltage and collapsed on the dc isolation dielectric, the bridge capacitance increases by a factor of 60–70 theoretically, and the resulting loading capacitance seen by the line is simply reduced to C_s. These two states in the loading capacitance yields two distinct loaded characteristics impedance of DMTL, namely, Z_{lu} (upstate loaded characteristic impedance: 58 Ω) and Z_{ld} (downstate loaded characteristic impedance: 44 Ω), where an acceptable return loss for both states can be achieved [17]–[19]. The phase shift per unit section can be controlled with the change of the phase velocity due to the change in the loaded characteristic impedance as [17]:

$$\Delta\phi = \frac{s\omega Z_o\sqrt{\varepsilon_{\text{eff}}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \text{ rad/section} \qquad (1)$$

where ω is the frequency in radians, c is the free-space velocity, and Z_o and ε_{eff} is the characteristic impedance and effective dielectric constant of the unloaded transmission line, respectively. The periodicity, i.e., the total length of the unit cell, is defined as s, and it is optimized as 800 μm considering the Bragg frequency, f_B, which is the cutoff frequency observed in periodic structures when the guided wavelength is getting closer to the periodic spacing. The selection of $f_B = 35$ GHz as $f_B = 2.3f_o$ ($f_o = 15$ GHz) ensures the proper operation of the phase shifter as true-time delay at 15 GHz with acceptable return and insertion losses. The following equations can be solved to define the required capacitance values and periodicity. Equations (1)–(4) are based on the work of Hayden and Rebeiz [17] and Hung *et al.* [18], and are summarized here for completeness:

$$s = \frac{Z_{ld}c}{\pi f_B Z_o\sqrt{\varepsilon_{\text{eff}}}} \text{ meters} \qquad (2)$$

$$C_s = \frac{Z_o^2 - Z_{ld}^2}{\pi f_B Z_o^2 Z_{ld}} \text{ farads} \qquad (3)$$

$$C_{bu} = C_s\frac{Z_{ld}^2\left(Z_o^2 - Z_{ld}^2\right)}{Z_o^2\left(Z_{lu}^2 - Z_{ld}^2\right)} \text{ farads} \qquad (4)$$

The designed unit cell shown in Fig. 2(b) can provide nearly an 11.5° phase shift at 15 GHz, which is verified with Ansoft's High Frequency Structure Simulator (HFSS) simulations where C_{bu} (55 fF) and C_s (115 fF) are tuned to achieve the specified Z_{lu} and Z_{ld}. The nonmovable static capacitor C_s is realized as a MAM capacitor, which has a high-Q factor (>400 at 15 GHz) compared to metal–insulator–metal (MIM) capacitors [17]. The height of membranes in the MAM capacitor and the switch is 2 μm. The characteristic impedance of the unloaded transmission line is selected to be $Z_o = 77$ Ω (CB-CPW dimensions: $W = 200$ μm, $G = 150\mu$m). The attenuation constant α_o and the effective dielectric constant ε_{eff} of the unloaded line is found to be 20 dB/m and 2.8 at 15 GHz, respectively [20].

The overall 3-bit RF MEMS phase shifter employed in the system consists of three sections with a total of 28 unit cells within an area of 22.4 mm × 2.1 mm. The first section has four cells and is designed to have a phase shift of $\Delta\phi = 46.9°$. The second section has eight cells providing 90.4°, and the next 16 cells forms the third bit, which is designed to give 182.6° at 15 GHz.

The dominant loss mechanism of the phase shifter is the loss of the unloaded CB-CPW. However, the series resistance of the bridge and the Q factor of the C_s also play a significant role. To be more specific, in order to accurately model the loss of the structure, a series resistance of $R_{bu} = 1.5$ Ω in the upstate and $R_{bd} = 0.8$ Ω in the downstate is used, which is found by curve fitting. The Q factor of the static capacitor (C_s) is found to be 433 with a value of $R_p = 40$ k Ω. The high-Q values of MAM capacitors improve the loss performance of the phase shifter. However, the bias resistors have an adverse effect on the Q factor of the capacitors and the loss of the phase shifter, which is explained in Section III-B.

B. Effect of Bias Resistors

In order to actuate each section of the phase shifter separately, thin-film resistors are employed. Fig. 2(b) shows that Si–Cr bias lines are placed inside the gaps of CB-CPW extending from one bridge to the other to carry the dc actuation voltage. The con-

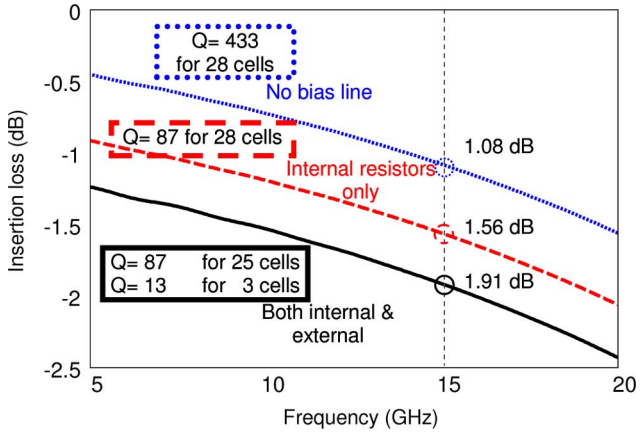


Fig. 4. Simulated insertion loss of the phase shifter, which is obtained from S_{21} when the ports of the structure are tuned as 44 $\Omega(Z_{ld})$.

ductivity of the Si–Cr layer is optimized during the fabrication process to have a low value ($\sigma_{\text{Si–Cr}} = 4300$ S/m), which is crucial in determining the loss of the structure. The return loss of the structure is not significantly affected by the presence of the bias resistors since the return loss is determined by the loaded line impedances Z_{ld} and Z_{lu}, which are only affected from the unloaded transmission line parameters and the loading capacitors C_{bu} and C_s. Fig. 4 shows the effect of the bias lines using the simulation results of insertion-loss characteristics. The designed phase shifter has an insertion loss of nearly 1.08 dB for the worst case (i.e., when all switches are down) if no bias lines are present. The insertion loss is calculated directly from S_{21} characteristics with the return loss removed by tuning the port impedance to 44 Ω, i.e., downstate loaded line impedance. The bias lines, which are placed inside the gaps of the CB-CPW, have an adverse effect on the insertion loss due to the decrease of the Q factor of the static capacitor C_s. The internal Si–Cr bias lines shown in Fig. 3 are shunt connected to the self resistance (R_p) of the static capacitor C_s, reducing the Q factor. Since each static capacitor sees two bias lines, the equivalent resistance of the capacitor C_s reduces to $R_p//(R_b/2)$ from R_p (40 kΩ) where R_b (internal bias resistor) is equal to 20 kΩ($\sigma_{\text{Si–Cr}} = 4300$ S/m, length $= 350$ μm, width $= 20$ μm, and thickness $= 0.2$ μm). The Q factor reduces accordingly to 87 from 433. The insertion loss of the entire structure, which is calculated as 1.08 dB without any bias lines, increases to 1.56 dB due to reduced Q factor of C_s. The external bias resistors that are placed underneath the air bridges on the ground depicted in Fig. 2 are used only for the three cells to actuate each bit separately. Due to the strong coupling between the ground plane and external bias resistor underneath, the external bias resistor is modeled with a smaller effective resistance $(R_e = 1.45$ kΩ). The Q factor of the static capacitor reduces accordingly to 13 for those three cells. The insertion loss of the structure is 1.91 dB, where the Q factor of three cells with external bias lines is 13 and the Q factor of the remaining 25 cells (out of 28) is 87.

C. Phase-Shifter Measurements

The phase shifters of the phased array are also fabricated separately on the same wafer for characterization purposes. They are measured using thru-reflect-line (TRL) calibration with a

TABLE I
SIMULATED AND MEASURED CIRCUIT PARAMETERS FOR THE UNIT CELL OF THE DMTL PHASE SHIFTER

Parameter	Simulated	Measured
C_{bu}	55 fF	50 fF
C_s	115 fF	71 fF
R_{bd}/R_{bu}	0.8 Ω/1.5 Ω	0.8 Ω/1.5 Ω
Z_O	77 Ω	77 Ω
ε_{eff}	2.76	2.76
α_O @ 15 GHz	20 dB/m	29 dB/m
R_p	40 kΩ	40 kΩ
R_b	20 kΩ	20 kΩ
R_e	1.45 kΩ	1.45 kΩ
C_{bd}	3 pF	1 pF
Z_{lu}	58 Ω	62.8 Ω
Z_{ld}	44 Ω	52.9 Ω
°/unit cell @ 15 GHz	11°	6°
Insertion Loss	1.91 dB	2.03 dB

port impedance of 77 Ω, where all eight states are measured by applying dc voltage with dc probes and bias tee. Actuation voltage of the phase shifters is measured to be 16 V. All the states have a return loss better than 10 dB with a worst case insertion loss of 2 dB at 15 GHz. The average insertion loss for eight states is 1.5 dB. Table I shows the simulated and measured circuit parameters for the unit cell. The bridge capacitance for the upstate (C_{bu}) can be fabricated very close to the designed value. However, the MAM capacitors (C_s) show a deviation compared to the simulated value. The measured downstate capacitance value is also degraded compared to simulated value due to the surface roughness [21]. Nevertheless, the measured downstate capacitance is high enough to have a virtual short circuit through the bridge. The MAM capacitors have a different mechanical design and are fixed on three sides to have a rigid structure that might result in an increase in the height due to the residual stress on the structural layer metal. Fig. 5 shows a 3-D plot of the surface profile data of the fabricated phase shifter obtained using a light-interferometer microscope. The bridge height is around 2 and 2.6 μm for the central bridge and MAM capacitor, respectively. The decrease of the MAM capacitances shifts the loaded line impedances Z_{lu} and Z_{ld}. The shift reduces °/unit cell performance of the measured phase shifter to 6° according to (1), which is 11° for the designed phase shifter. Fig. 6 shows the measured insertion phase characteristics for all the states of the phase shifter. The measured phase shifter provides approximately 20°/50°/95° phase shifts and their combinations.

Table II shows simulated and measured loss components at 15 GHz. The loaded line loss, which is defined when $R_{bd} = 0\,\Omega, R_p = R_b = R_f \to \infty$, is directly related to the unloaded line loss with a multiplicative factor of Z_o/Z_{ld}. The loaded line loss is increased in the measurements due to the increase of the attenuation constant (α_o) of the unloaded line. The Q factor losses are increased not only due to the decrease of the quality factor, but also due to the change of the loaded line impedance to 52.9 Ω from the designed value of 44 Ω. The Q factor of the MAM capacitors with internal bias resistors reduces to 53

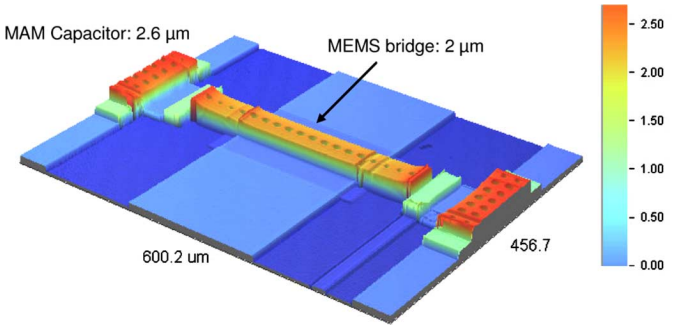


Fig. 5. Surface profiler view of the unit cell of the phase shifter obtained using an interferometer microscope.

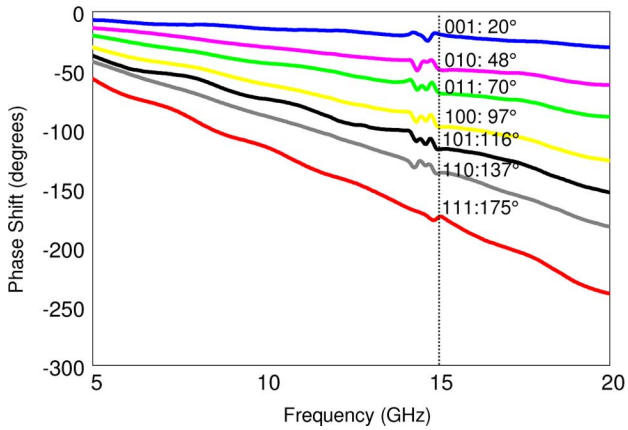


Fig. 6. Measured insertion phase-shift characteristics of the phase shifter for different states.

TABLE II
SIMULATED AND MEASURED LOSS COMPONENTS AT 15 GHz. LOADED LINE LOSS IS DEFINED WHEN $R_{bd} = 0\ \Omega, R_p = 40\ \text{k}\ \Omega, R_b = R_e \to \infty$

Parameter	Simulated	Measured
Loaded Line Loss	0.63 dB	0.83 dB
Bridge Resistance (R_{bd}) Loss	0.45 dB	0.21 dB
25 cells Q-factor Loss	0.43 dB	0.51 dB
3 cells Q-factor Loss	0.40 dB	0.48 dB
Total Loss	1.91 dB	2.03 dB

(simulated value: 87) due to the decrease of the capacitance value. The Q factor of the MAM capacitors having both internal and external resistors is equal to 8 (simulated value: 13). Fig. 7 shows the insertion-loss analysis for the measured structure illustrating the effect of Q-factor values of MAM capacitors. These cases are: 1) $Q = 433$ (no bias line present) for 28 cells; 2) $Q = 53$ for 28 cells; and 3) $Q = 53$ (for 25 cells) and $Q = 8$ (for three cells). The analysis also shows that if a conductivity of 2500 S/m is achieved, the worst case insertion loss can be reduced down to nearly 1.6 dB, where Q factors can be increased to 132 for 25 cells with internal bias resistors and to 22 for three cells with both internal and external resistors. The average insertion loss of the phase shifter would be approximately 1.3 dB, which is quite close to the reported losses of these types of MEMS phase shifters [17]. The conductivity

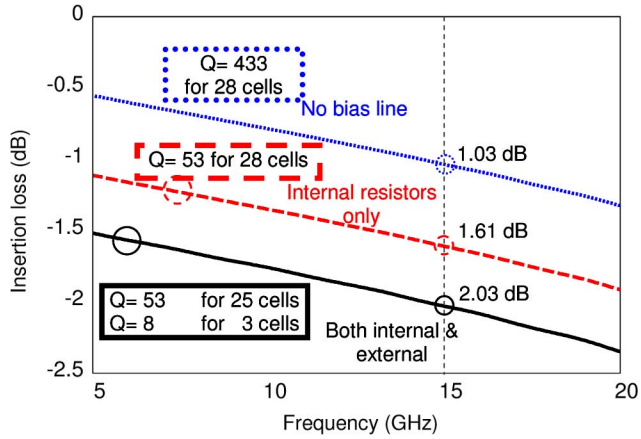


Fig. 7. Insertion loss of the phase shifter (extracted from measurement results), which is obtained from S_{21} when the ports of the structure are tuned as $52.9\ \Omega(Z_{ld})$.

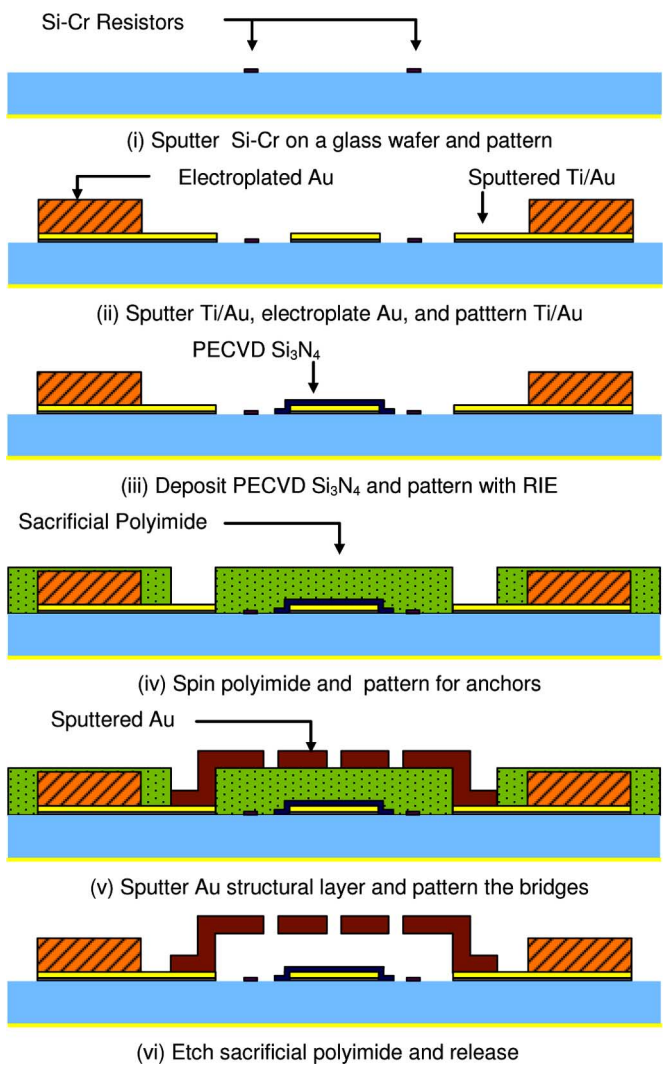
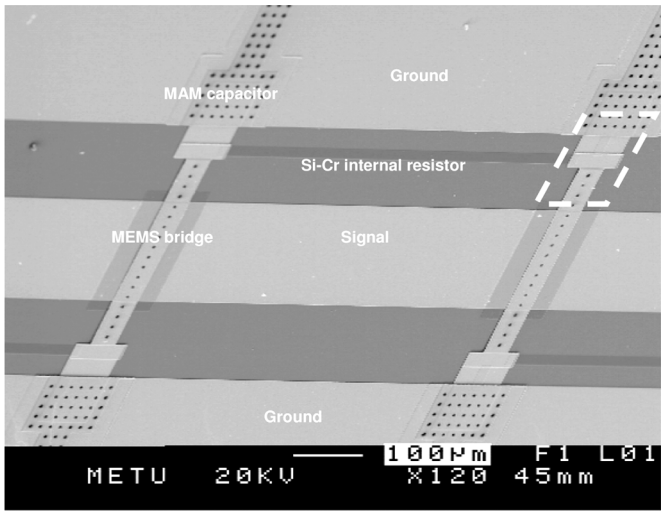
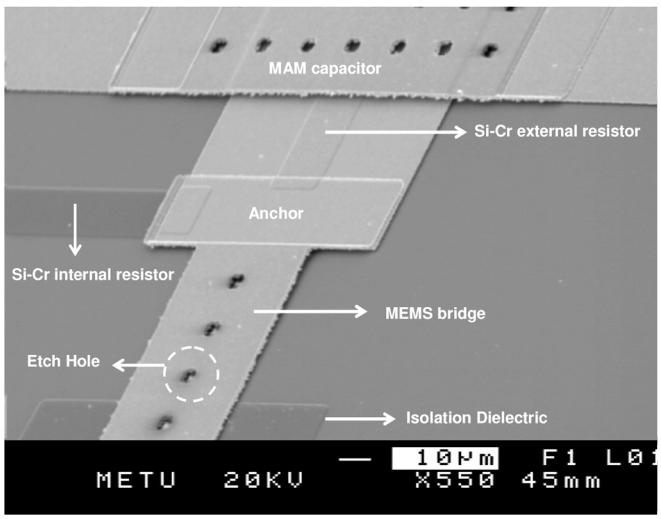


Fig. 8. Process flow used in the fabrication of the phased array.

value of the Si–Cr film depends on the chamber conditions of the sputter equipment and the gas flow during processing, and it can be reduced by process optimizations to further reduce the losses of the phase shifters, which is under progress.



(a)



(b)

Fig. 9. SEM photographs of the phase-shifter structure. (a) Two unit cells where Si–Cr internal resistors connecting the unit cells to carry dc signal can be seen. (b) Detailed view of the anchor region of the MEMS bridge where both external and internal resistors are attached. Etch holes on the suspended regions are used to improve the removal of sacrificial layer underneath those regions.

IV. Fabrication and Measurements of the Array

The phased array presented in this study is fabricated using the surface micromachining process developed at METU for implementation of various RF MEMS components on 500-μm-thick Pyrex 7740 glass substrates ($\varepsilon_r = 4.6, \tan\delta = 0.005$). The backside of the wafer is coated with a 100-Å/2-μm Ti/Au layer by sputtering for ground metallization of microstrips and CB-CPWs. Fig. 8(i)–(vi) shows the surface micromachining process. (i) The process begins with 2000-Å-thick Si-Cr resistive layer deposition by sputtering and patterning by wet etching. (ii) The next step is the sputtering of a 100/3000-Å-thick Ti/Au layer, which is required as the seed layer for electroplating of the base metallization. The base metallization layer is formed using a 2-μm-thick gold layer, which is electroplated inside the regions defined by the mold photoresist. The remaining Ti/Au seed layer is etched using wet etching with selective titanium and gold etchants. (iii)

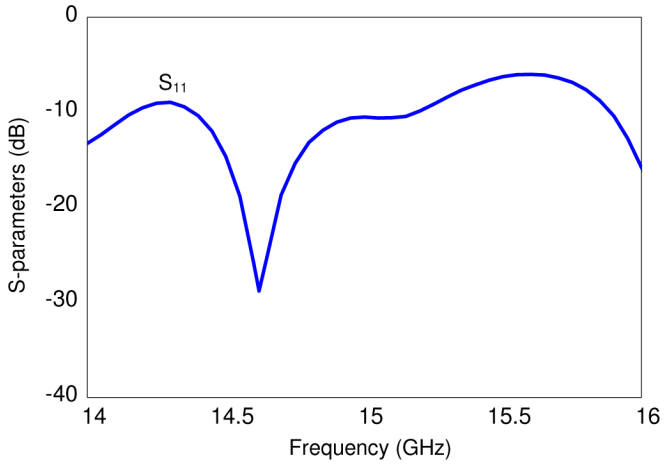


Fig. 10. Measured return loss of the monolithic phased array.

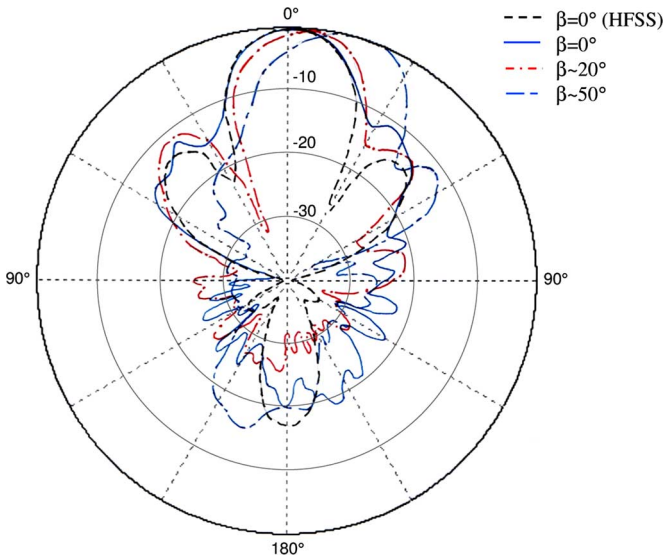


Fig. 11. Measured radiation pattern of the monolithic phased array for different progressive phase shifts.

A 3000-Å-thick Si_3N_4 layer is coated as the dc isolation layer using a plasma enhanced chemical vapor deposition technique (PECVD) and patterned using the reactive ion etching (RIE) technique. (iv) The next step is the spin coating of the photodefinable polyimide (PI 2737) as the 2-μm-thick sacrificial layer. (v) A 1-μm-thick gold layer is then sputter deposited and patterned as the structural layer. (vi) The sacrificial layer is wet etched in the $\mathrm{SVC} - 175$ photoresist stripper, rinsed in isopropyl alcohol, and dried in a supercritical point dryer. Fig. 9 shows the scanning electron microscrope (SEM) photographs of the phase shifters fabricated using the process flow described above. The radiation pattern measurements of the phased array are performed via an in-house anechoic chamber. In order to apply the dc voltages, the fabricated phased array is attached to a printed circuit board (PCB) card. There exist mechanical switches located at the back of the card in order not to affect the radiation characteristics. The dc connections to the phased array are obtained using wire bonds. Fig. 10 shows the reflection coefficient characteristics of the phased array. The measured resonant frequency of the system is at 14.62 GHz with a 10-dB

bandwidth of 6%, which is very close to the designed value of 15 GHz with a 10-dB bandwidth of 2.5% [6]. Fig. 11 gives the measured radiation patterns of the phased array for different phase-shifter settings. It is observed that the beam can be tilted by 4° and 14° when the progressive phase shifts are adjusted nearly 20° and 50°, respectively. These values are quite close to the expected amount of steering. The back-radiation levels around −15 dB are acceptable considering the PCB card and the mechanical switches attached to this card for dc biasing of MEMS phase shifters.

V. Conclusion

This paper has presented the design and implementation of a novel monolithic phased-array system with RF MEMS phase shifters. The phased-array system is fabricated using the micromachining process developed at METU. The system employs 3-bit DMTL-type RF MEMS phase shifters, which are composed of high-impedance transmission lines ($Z_o > 50\,\Omega$) loaded with MEMS bridges in series with MAM capacitors. The phase shifter can provide nearly 20°/50°/95° phase shifts and their combinations at the expense of 1.5-dB average insertion loss at 15 GHz, showing low-loss performance compared to semiconductor counterparts. The reduction of the losses in the phase-shifting elements of a phased array can be used to eliminate one of the amplification stages, decreasing both the system costs and dc power consumption. Radiation pattern measurements shows that the beam can be steered to the desired angles by the appropriate settings of MEMS phase shifters. This study shows that the use of RF MEMS phase shifters monolithically integrated with patch antennas and feed network can offer better performance phased arrays by reducing the dc power consumption, packaging costs, and the size of the system compared to arrays with ferrite- or semiconductor-based phase shifters. This study is one of the first that demonstrate the monolithic implementation of a phased array on a single substrate with an acceptable performance, which can be further improved by increasing the number of antenna elements. Such monolithically integrated MEMS-based phased arrays can be a good candidate in weight- and power-constrained applications such as fire-control radars and automotive radars.

Acknowledgment

The authors would like to thank to the Microelectronic Technologies staff of the Middle East Technical University, Ankara, Turkey, particularly O. S. Akar, for their support in the fabrication. The authors also thank M. Unlu and H. I. Atasoy for the process development and RF measurements.

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