The Matrix Converter Drive Performance Under Abnormal Input Voltage Conditions

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***Abstract*—The matrix converter (MC) is a direct frequency conversion device with high input power quality and regeneration capability. As a device without energy storage elements, it has higher power density than pulse-width modulation (PWM) inverter drives. However, for the same reason, the ac line side disturbances can degrade its performance and reliability. In this paper, the behavior of the MC drive under abnormal input line voltage conditions has been investigated. A technique to eliminate the input current distortion due to the input voltage unbalance has been developed and its feasibility proven via computer simulations and laboratory experiments. The power line failure behavior has also been investigated and the rapid restarting capability of the MC drive has been demonstrated via laboratory experiments.**

***Index Terms*—Current harmonics, matrix converter, power failure, PWM, voltage unbalance.**

I. Introduction

THE matrix converter (MC) is a direct frequency conversion device that generates variable magnitude variable frequency output voltage from the ac utility line. It has high power quality (sinusoidal currents with unity power factor) and it is fully regenerative. Fig. 1 shows the basic MC drive structure. Since it does not involve an intermediate dc voltage link and the associated large capacitive filter, an MC drive has higher power density than a pulse-width modulation (PWM) inverter drive.

The evolution of the MC technology has been taking place over the last two decades [1]–[3]. Due to the increasing importance of power quality and energy efficiency issues, the MC technology has recently attracted the power electronics industry and the progress has been further accelerated [4]. Control and modulation techniques that enhance both the ac line and motor load side performance have been well developed. As the prime hardware elements of the MC technology, efficient and compact bidirectional switches could be manufactured by integrating power transistors and diodes into a module. Via intelligent commutation techniques, the snubber circuit requirements have been significantly reduced and reliable operation could be achieved. As a result, the main obstacles toward realizing an industrial MC drive have been overcome and initial steps toward developing a commercial product have already been taken [4]. However, several performance and reliability issues of the MC still need to be addressed. In particular, the influence of input line voltage disturbances on both the load side performance and the input current is significant and undesirable. This paper addresses the ac line voltage disturbance related performance issues of the MC drive.

Since the MC is a direct frequency conversion device, the disturbances at the ac utility grid (line) side are immediately reflected to the load side. Line voltage source or impedance unbalances can result in unwanted input/output harmonic currents. Several techniques that reduce the influence of the input voltage unbalance on the load side of the MC drive have been reported [3], [9]. However, the proposed compensation methods do not consider the input current waveform quality.

In this paper, a technique that improves both the input current and output performance of the MC has been developed. Another important issue involves the ac grid power failure. Since the MC drive has no intermediate dc link and large capacitor associated with it, there is no stored energy in the MC. As a result, the utility line power loss results in immediate power loss to the load and renders the drive without ride-through capability. For the same reason, restarting (following a momentary line power failure) can be rapid and without large inrush currents. In this paper, the transients associated with the utility line loss and recovery conditions have been thoroughly investigated in the laboratory. The experimental results demonstrate that the drive safely turns off during these disturbances and rapidly restarts following the utility grid restoration.

The paper first reviews the MC control techniques. Second, it addresses the voltage unbalance problem. The problem is analyzed, a new technique developed and its feasibility is demonstrated via computer simulations and experimental results. Third, the power line loss behavior is experimentally investigated.

II. MC Classical PWM and Control Strategies

The literature on the matrix converter switching and control strategies is rich [1]–[3]. In this paper, the control method reported in [3] and [4] has been employed because of good input current control characteristics under balanced input voltage conditions. The technique will be described with the aid of the typical example of PWM pattern and line-to-line output voltages shown in Fig. 2 where switches $S13$ and $S23$ are off, $S33$ is on, and the remaining switches controlled over the carrier period T_s. The MC equivalent circuit corresponding to this case is

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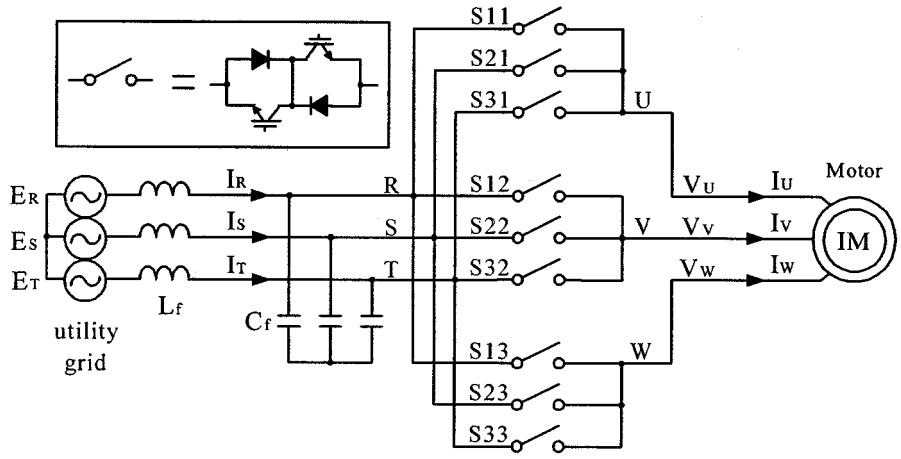


Fig. 1. Basic structure of a matrix converter drive.

illustrated in Fig. 3, where the induction motor is represented with a three-phase current source. Input phase voltages, E_R, E_S, and E_T are sorted and labeled as $E_{\max}$, E_{mid}, and $E_{\min}$, respectively, according to their value. The base voltage, E_{base}, is defined as the input phase voltage that has the highest absolute value. The output voltage references V_{U_ref}, V_{V_ref}, and V_{W_ref} are also sorted and labeled as $V_{\max}$, V_{mid}, and $V_{\min}$. The details of the sorting rules are described in [4].

In order to simplify the switch duty cycle calculations, the terms $dE_{\max}$, dE_{mid}, $dV_{\max}$, and dV_{mid} are introduced in the following:

$$dE_{\max} = E_{\max} - E_{\min} \tag{1}$$

$$dE_{\mathrm{mid}} = \left\{ \begin{array}{l} E_{\max} - E_{\mathrm{mid}}, \text{ if } E_{\mathrm{base}} = E_{\max} \\ E_{\mathrm{mid}} - E_{\min}, \text{ if } E_{\mathrm{base}} = E_{\min} \end{array} \right\} \tag{2}$$

$$dV_{\max} = V_{\max} - V_{\min} \tag{3}$$

$$dV_{\mathrm{mid}} = \left\{ \begin{array}{l} V_{\max} - V_{\mathrm{mid}}, \text{ if } E_{\mathrm{base}} = E_{\max} \\ V_{\mathrm{mid}} - V_{\min}, \text{ if } E_{\mathrm{base}} = E_{\min} \end{array} \right\}. \tag{4}$$

The desired line-to-line output voltage $dV_{\max}$ and dV_{mid} can be obtained if pulse pattern is such that

$$dV_{\max} = \frac{1}{T_S}\left[(T_{11}+T'_{11})dE_{\max} + (T_{21}+T'_{21})dE_{\mathrm{mid}}\right] \tag{5}$$

$$dV_{\mathrm{mid}} = \frac{1}{T_S}\left[(T_{12}+T'_{12})dE_{\max} + (T_{22}+T'_{22})dE_{\mathrm{mid}}\right]. \tag{6}$$

The above equations indicate the output v-s can be synthesized from the selected input line voltages. However, the switching sequence and the switch duty cycles are not fully constrained. Therefore, this flexibility of the control variables is utilized to distribute the load current segments to the input in a manner to obtain input currents with unity power factor and low harmonic distortion.

Fig. 2(c) and the circuit diagram of Fig. 3 aid describing the basic relations between input current and PWM pattern of MC. Neglecting the filter capacitor, the "R" phase current average value over T_s can be expressed as

$$I_{\max} = I_R \approx I_{Rout} = \frac{1}{T_S}\left[(T_{11}+T'_{11})Iu + (T_{12}+T'_{12})Iv\right] \tag{7}$$

where $(T_{11}+T'_{11})$ and $(T_{12}+T'_{12})$ are the on-times of switches $S11$ and $S12$, respectively, and $S13$ is off over T_s. Similarly, the "S" phase current can be obtained as

$$I_{\mathrm{mid}} = I_S \approx I_{Sout} = \frac{1}{T_S}\left[(T_{21}+T'_{21})Iu + (T_{22}+T'_{22})Iv\right]. \tag{8}$$

From (7) and (8), it can be seen that input currents I_R and I_S are functions of the on-times and output currents. Without additional constraints, the solutions for the on-times in (5) and (6) are not unique. The on-time ratios $(T_{21}+T'_{21})/(T_{11}+T'_{11})$ and $(T_{22}+T'_{22})/(T_{12}+T'_{12})$ can be arbitrarily determined (without loss of $dV_{\max}$ and dV_{mid} control). This degree of freedom can be used to control input currents. The current distribution factor α_i is defined as

$$\alpha_i = \frac{(T_{21}+T'_{21})}{(T_{11}+T'_{11})} = \frac{(T_{22}+T'_{22})}{(T_{12}+T'_{12})} \tag{9}$$

where two on-time ratios are set to same value to control ratio I_S/I_R by one control parameter α_i.

Subtituting (9) in (7) and (8), I_S is calculated as

$$I_S = \frac{\alpha_i(T_{11}+T'_{11})Iu + \alpha_i(T_{12}+T'_{12})Iv}{(T_{11}+T'_{11})Iu + (T_{12}+T'_{12})Iv} I_R = \alpha_i I_R. \tag{10}$$

Equation (10) shows that the ratio of the input currents can be controlled by α_i. With the input voltages being sinusoidal and balanced, setting α_i in (10) as E_S/E_R results in input phase currents that are sinusoidal and in phase with the input voltages (unity power factor condition). In Fig. 4, the shape of the auxiliary control variables and the current distribution factor for unity power factor operating condition are illustrated. Substituting α_i, (5) and (6) can be rearranged as

$$(T_{11}+T'_{11}) = \frac{dV_{\max}}{\alpha_i dE_{\mathrm{mid}} + dE_{\max}} T_S \tag{11}$$

$$(T_{12}+T'_{12}) = \frac{dV_{\mathrm{mid}}}{\alpha_i dE_{\mathrm{mid}} + dE_{\max}} T_S. \tag{12}$$

As shown in Fig. 2, the MC output voltage pulses are placed symmetrically over T_s to reduce output harmonic distortion. This symmetry condition can be described as

$$\frac{T_{31}}{T'_{31}} = \frac{T_{21}}{T'_{21}} = \frac{T_{32}}{T'_{32}} = \frac{T_{22}}{T'_{22}} = 1. \tag{13}$$

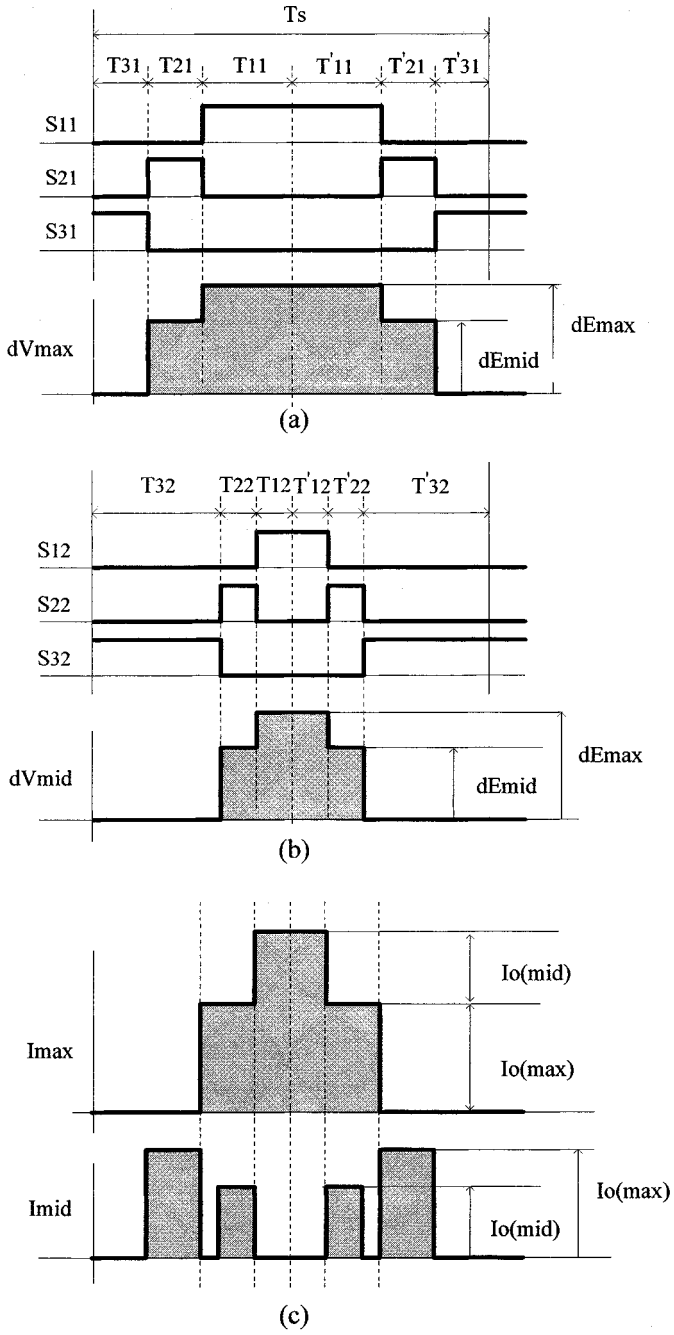


Fig. 2. PWM switching pattern and line-to-line output voltages. (a) $V_{\max}$ phase. (b) V_{mid} phase. (c) Two input currents.

Equation (10) is obtained for the pulse pattern shown in Fig. 2, and the input current relations can be generalized as

$$I_{\mathrm{mid}} = \left\{ \begin{array}{l} \alpha_i I_{\max},\ \text{if } E_{\min} = E_{\mathrm{base}} \\ \alpha_i I_{\min},\ \text{if } E_{\max} = E_{\mathrm{base}} \end{array} \right\}. \tag{14}$$

For a balanced utility grid, in order to obtain sinusoidal input currents with unity power factor, the current distribution factor is calculated as

$$\alpha_i = \left\{ \begin{array}{ll} \frac{E_{\mathrm{mid}}}{E_{\max}}, & \text{if } E_{\min} = E_{\mathrm{base}} \\ \frac{E_{\mathrm{mid}}}{E_{\min}}, & \text{if } E_{\max} = E_{\mathrm{base}} \end{array} \right\}. \tag{15}$$

From (11)–(13) and (15), all the on-time intervals can be obtained.

The control strategy described in this section has good input and output performance under balanced utility conditions. The unbalanced operation is investigated next.

III. Input Voltage Source Unbalance

A. Theoretical Background

An unbalanced three-phase voltage vector can be decomposed into the positive sequence and negative sequence balanced voltage vectors as

$$\vec{E}_{RST} = E_p e^{j(\omega t + \theta_P)} + E_n e^{-j(\omega t + \theta_n)} \tag{16}$$

where ω is the angular frequency of the system, E_p and θ_p are amplitude and phase of positive sequence voltage, and E_n and θ_n are amplitude and phase of negative sequence voltage, respectively. Neglecting the input LC filter losses, the relation between the input current vector $\vec{I}_{RST}$ and output power P_{out} can be expressed as

$$P_{out} \approx P_{in} = \frac{3}{2} \vec{E}_{RST} \cdot \vec{I}_{RST}. \tag{17}$$

In order to maintain performance on the load side of the MC drive, the input power must be same as the output power regardless of the input voltage unbalance. Assuming harmonic-free output power, the MC input power must also be harmonic-free. It can be inferred from (17) that appropriately selected unbalanced input currents can compensate for the influence of the unbalanced input voltages without deterioration of MC drive output performance. Various techniques have been reported for unbalanced operation of power converters [5]–[8]. A compensation technique that was formerly applied to the PWM voltage source converters (VSCs), is the basic idea employed in this paper [10]. The technique yields input currents with low harmonic distortion. The basic idea will be summarized next. The unbalanced input currents can be expressed as

$$\vec{I}_{RST} = I_p e^{j(\omega t + \phi_p)} + I_n e^{-j(\omega t + \phi_n)}. \tag{18}$$

Substituting (16) and (18) in (17), the output power can be calculated in

$$\begin{aligned} P_{out} =& \frac{3}{2} \mathrm{Re}\left[\vec{E}_{RST} \vec{I}^{\dagger}_{RST} \right] \\ =& \frac{3}{2} \mathrm{Re} \underbrace{\left[E_p I_p e^{j(\theta_p - \phi_P)} + E_n I_n e^{-j(\theta_n - \phi_n)} \right]}_{\text{dc term}} \\ &+ \frac{3}{2} \mathrm{Re} \underbrace{\left[E_p I_n e^{j(2\omega t + \theta_p + \phi_n)} + E_n I_p e^{-j(2\omega t + \theta_n + \phi_P)} \right]}_{2\omega \text{ac term}} \end{aligned} \tag{19}$$

where † denotes complex conjugate. P_{out} in (19) consists of a dc term and a 2ω ac term. Assuming that the load is at steady state and has no ripple at 2ω frequency, the 2ω term in (19) can be eliminated by injecting a negative sequence current $\vec{I}_n$. The positive sequence current $\vec{I}_p$ is regulated to meet the power

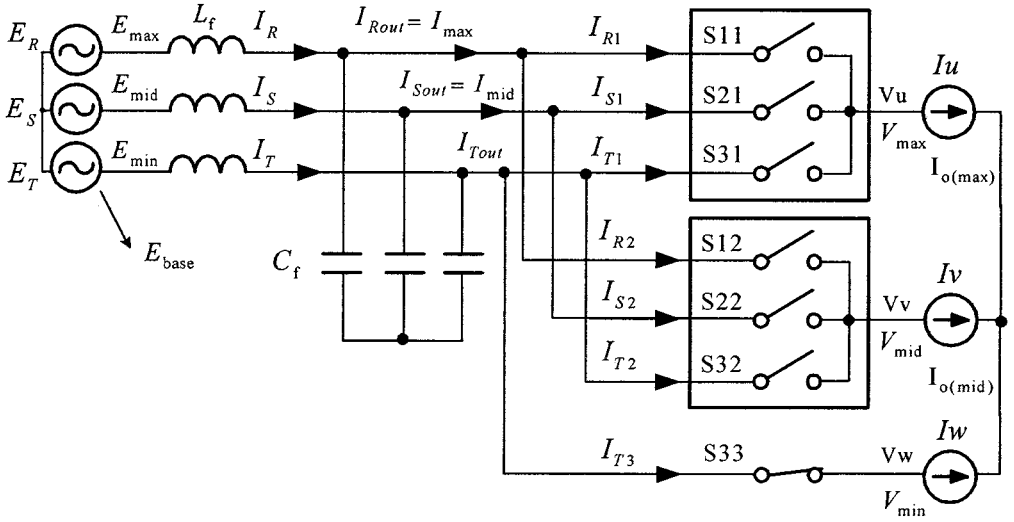


Fig. 3. MC drive equivalent circuit for the switching pattern of Fig. 2.

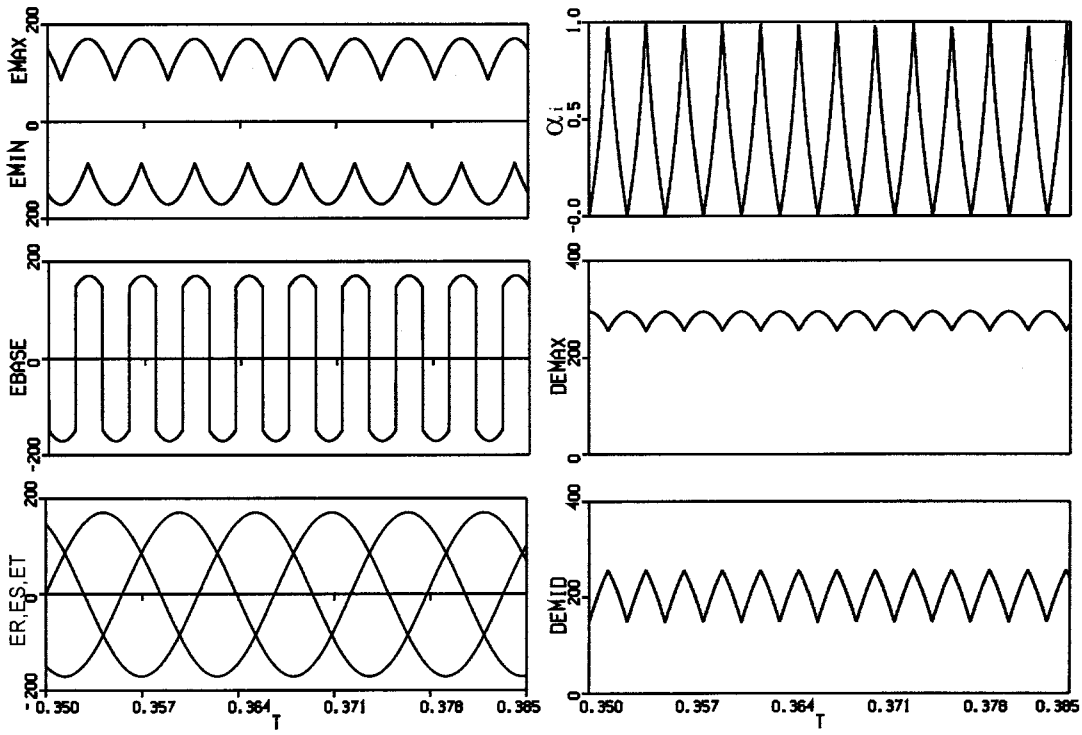


Fig. 4. Input current control variables under balanced grid voltage.

requirement of the load side. This negative sequence current can be calculated in

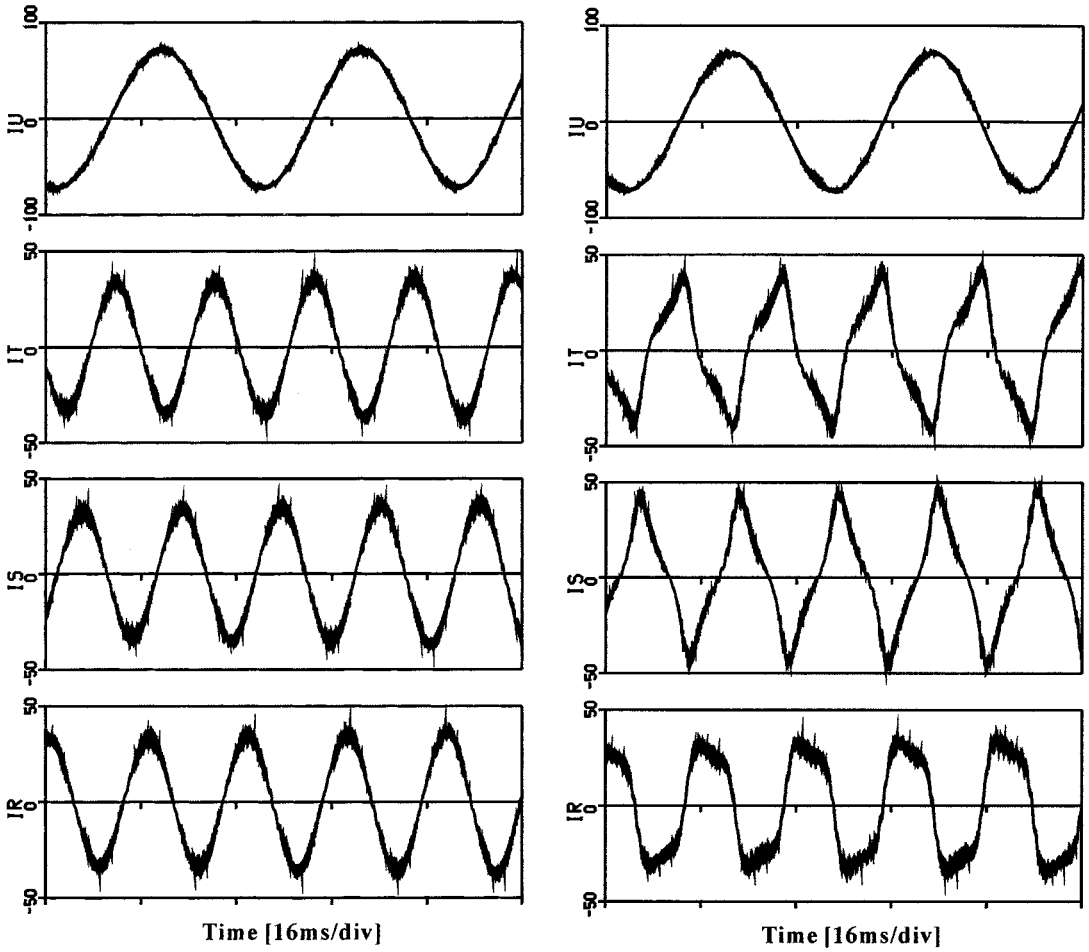
$$I_n = -\frac{E_n}{E_p} I_p \quad \text{and} \quad \phi_n = \theta_n - \theta_p + \phi_p. \tag{20}$$

In a PWM-VSC, the positive sequence current magnitude is controlled in a manner to maintain dc link voltage regulation. Since an MC drive does not involve a dc voltage link, this approach is irrelevant for the MC drive case. Therefore, the amplitude command of $\vec{I}_p$ in (18) is retained and its phase is selected to be the same as that of $\vec{E}_p$ ($\phi_p = \theta_p$) in order to obtain unity power factor

$$\vec{I}_p = I_p e^{j(\omega t + \phi_P)} = I_m e^{j(\omega t + \theta_P)} \tag{21}$$

where I_m is an arbitrary positive constant. Thus, the input current required to maintain the load power constant and the input power factor unity, can be obtained from (18), (20), and (21) as

$$\vec{I}^*_{RST} = I_m \left[e^{j(\omega t + \theta_P)} - \frac{E_n}{E_p} e^{-j(\omega t + \theta_n)} \right]. \tag{22}$$



(a) (b)

Fig. 5. Input and output currents under balanced and unbalanced grid voltage. (a) Balanced operation. (b) Unbalanced operation. From the bottom to the top (with vertical axes scales): R, S, T input phase currents (50 A/div), and U output phase current (100 A/div).

In (22), the star symbol emphasizes that the input current must be programmed to this value (via PWM control of the MC switches) in order to obtain low distortion input current. Note that in (22) the magnitude of the positive sequence component, I_m is not measured/calculated. As (20) indicates, the relative value of the negative sequence component to the positive sequence component should be programmed to satisfy (22). Therefore, the variable I_m has been declared as an arbitrary positive constant. Section II described the technique that utilizes the current distribution function and switch duty cycles for input current control under the balanced input voltage source condition. In the following, the problem with this technique under unbalanced input voltages is demonstrated and then a technique to improve the input performance is established.

B. Input Current Without Unbalance Compensation

Under unbalanced grid condition, utilizing the same current distribution function as in (15) results in the following input current function:

$$\vec{I}^{*}_{RST} = I_m \left[e^{j(\omega t+\theta_P)} + \frac{E_n}{E_p} e^{-j(\omega t+\theta_n)} \right]. \qquad (23)$$

Since (23) does not satisfy the constant load power condition, the input currents are distorted and they contain significant amount of harmonics. The PWM-VSC and active filters also exhibit similar behavior under voltage unbalance condition [7], [8]. The computer simulations in Fig. 5 show the input and output current control performance of the MC under balanced and unbalanced grid voltage with percent unbalance of 21%. The percent unbalance is defined as the E_n to E_p ratio and it is expressed in percentage. The PWM switching frequency is 5 kHz, and the control block is executed every 200 μs.

The waveforms show that during unbalance output current I_u is maintained sinusoidal. This is because the v-s requirements of the load are matched by the PWM strategy. On the other hand, while the input currents during balanced operation are sinusoidal [see Fig. 5(a)], they are highly distorted under voltage unbalance [see Fig. 5(b)] because α_i is obtained from (15) and this formula is developed with the balanced input voltage assumption. Therefore, this approach is inadequate for unbalanced operating conditions.

C. Input Current Control With Unbalance Compensation

Since the above method results in poor input performance under unbalance, the method will be modified to account for

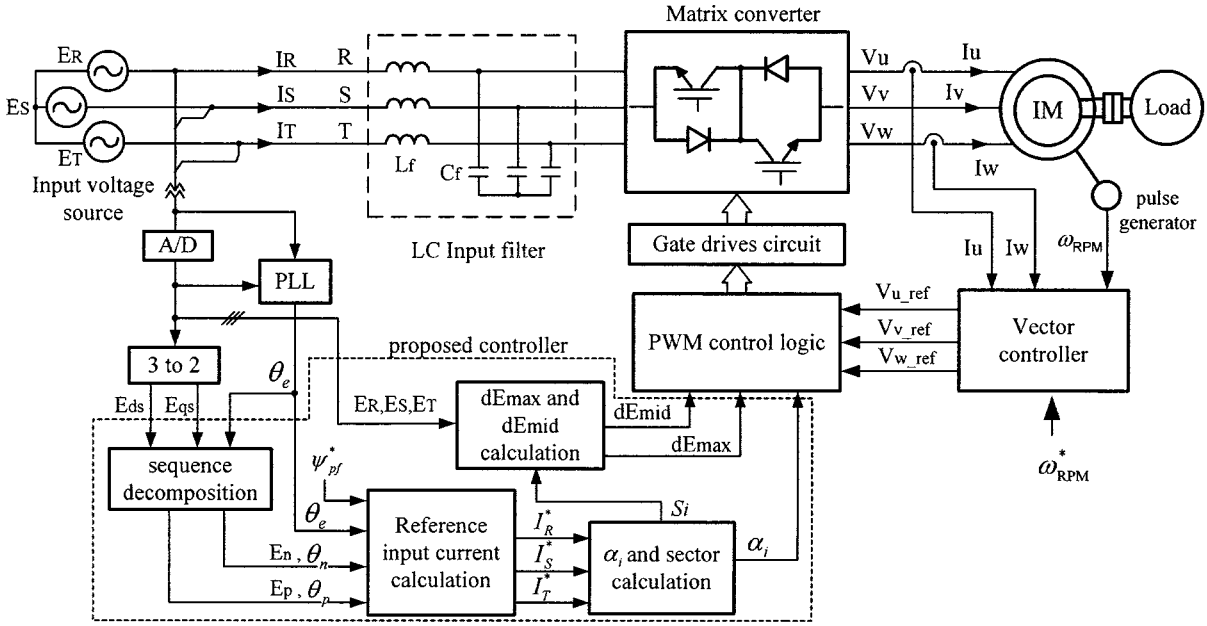


Fig. 6. MC system control block diagram with the unbalance compensating controller.

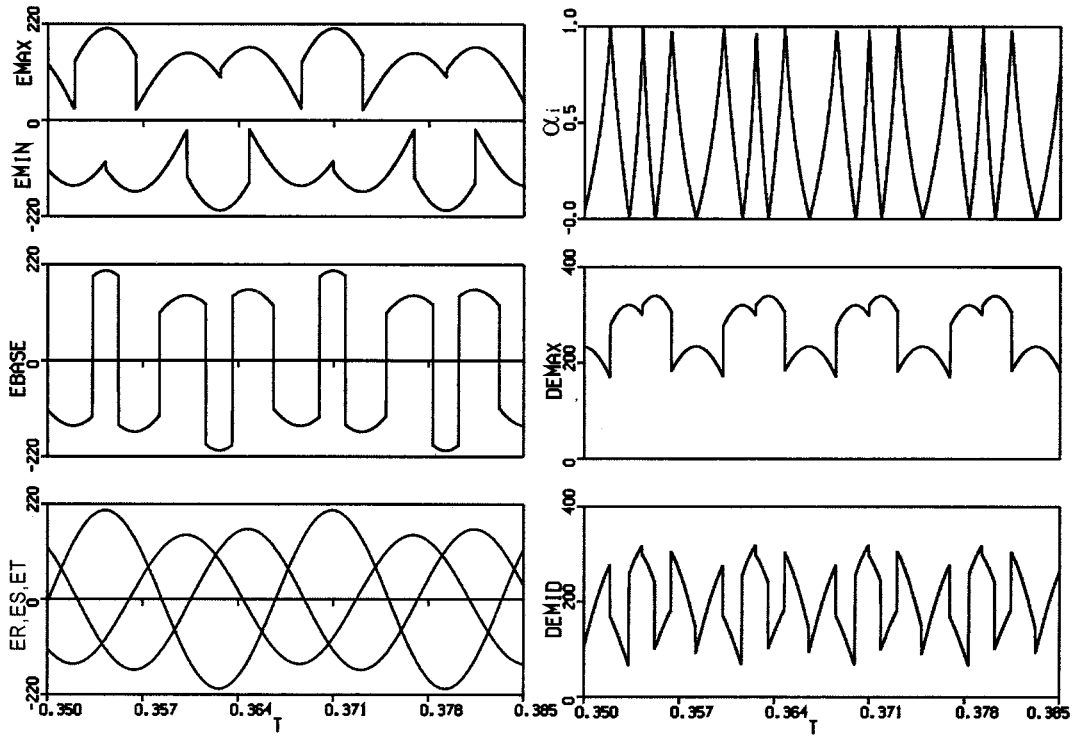


Fig. 7. Control variables under unbalanced grid voltage (proposed).

the unbalance. New definitions of α_i, $dE_{\max}$, and dE_{mid} are introduced as

$$\alpha_i = \left\{ \begin{array}{l} \frac{I^*_{\mathrm{mid}}}{I^*_{\max}}, \text{ if } I^*_{\min} = I^*_{\mathrm{base}} \\ \frac{I^*_{\mathrm{mid}}}{I^*_{\min}}, \text{ if } I^*_{\max} = I^*_{\mathrm{base}} \end{array} \right\} \quad (24)$$

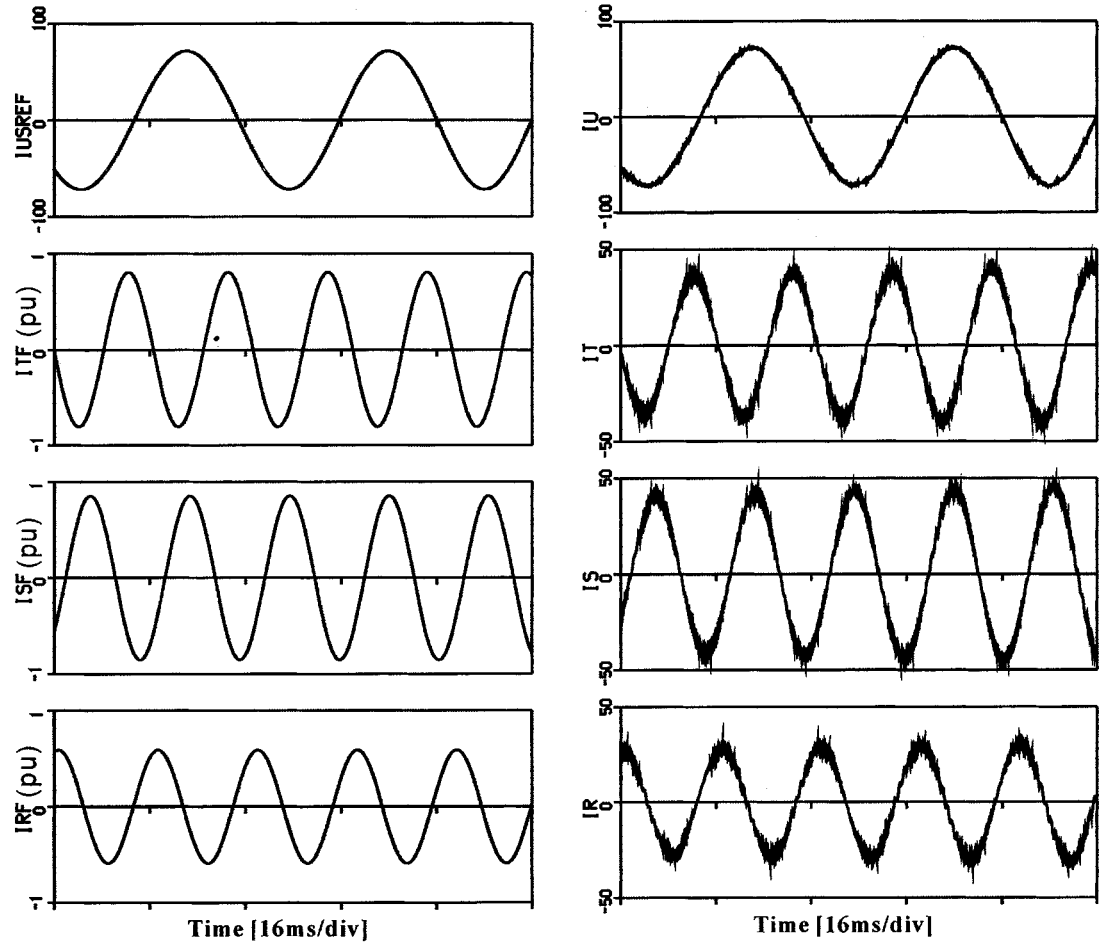
where $I^*_{\max}$, I^*_{mid}, and $I^*_{\min}$ are the reference input currents

$$dE_{\max} = E(I^*_{\max}) - E(I^*_{\min}) \quad (25)$$

$$dE_{\mathrm{mid}} = \left\{ \begin{array}{l} E(I^*_{\max}) - E(I^*_{\mathrm{mid}}), \text{ if } I^*_{\max} = I^*_{\mathrm{base}} \\ E(I^*_{\mathrm{mid}}) - E(I^*_{\min}), \text{ if } I^*_{\min} = I^*_{\mathrm{base}} \end{array} \right\} \quad (26)$$

where $E(I^*_{\max})$, $E(I^*_{\mathrm{mid}})$, and $E(I^*_{\min})$ are the input phase voltages corresponding to the reference current $I^*_{\max}$, I^*_{mid}, and $I^*_{\min}$, respectively.

Fig. 6 shows the MC system control block diagram employing the proposed method. The three phase input voltages are measured and transformed to the synchronous reference frames rotating at $+\theta_e$ and $-\theta_e$, respectively. The positive



(a) (b)

Fig. 8. Input and output currents with the proposed controller under unbalance. (a) Reference currents. (b) Real currents. Traces from the bottom to the top (with vertical axes scales): R, S, T input phase currents (1 p.u./div and 50 A/div), and U output phase current (100 A/div).

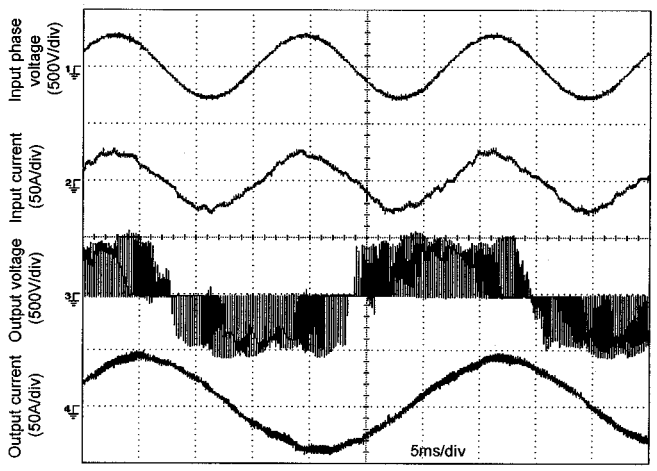


Fig. 9. The MC drive performance under voltage unbalance (no compensation). Traces from the bottom to top: output current, output voltage, input current, and input phase voltage.

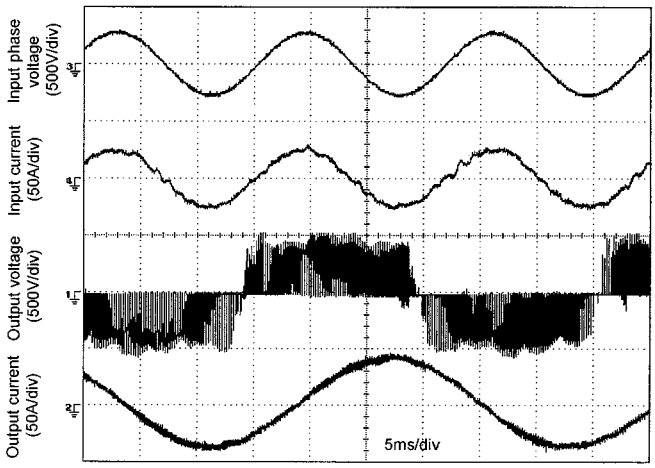


Fig. 10. The MC drive performance with the proposed controller under unbalance. Traces from the bottom to top: output current, output voltage, input current, and input phase voltage.

and negative sequence components $E_p e^{j\theta_P}$ and $E_n e^{-j\theta_n}$ are extracted by subsequent low-pass filters. References I_R^*, I_S^*, and I_T^* are obtained from (22), and phase shifted according to a phase-shift reference ψ_{pf}^* to control the power factor. The input current sector S_i is obtained from the current references to sort input voltage variables [4]. α_i is calculated from (24) where the sorting rule of I_R^*, I_S^*, and I_T^* into $I_{\max}^*$, I_{mid}^*, and $I_{\min}^*$ is same as that of the input voltage.

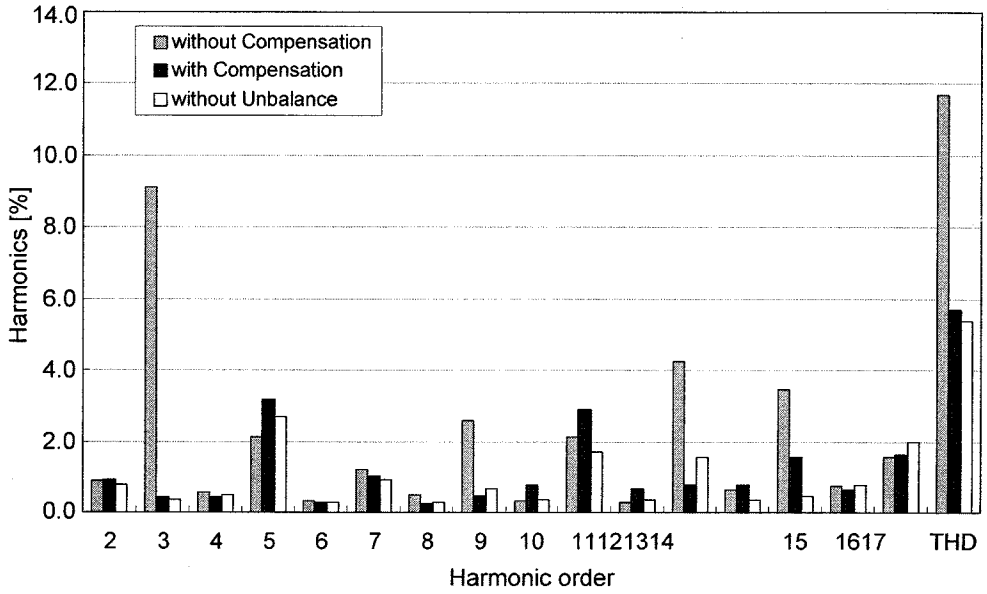


Fig. 11. Comparison of experimental input current harmonic spectrum.

Fig. 7 shows input current control variables with the proposed method under percent unbalance of 21%. Accounting for the unbalance, the current distribution factor is different from that of Fig. 4 that corresponds to the balanced case. Fig. 8 illustrates the computer simulated performance of 220 V, 11 kVA, matrix converter drive for this condition. The load is a 7.5 kW induction motor and the indirect field orientation control method is employed for torque regulation. The switching frequency is 5 kHz, and the sampling rate of the control block is 200 μs. The waveforms demonstrate the capability of the method to program sinusoidal input currents without loss of output current control capability. The harmonic content of the current will be discussed later.

Figs. 9 and 10 illustrate the experimental waveforms of the MC drive under unbalanced grid voltage with percent unbalance of 9.5%. A 220 V, 7.5 kW induction motor is operating at 900 r/min and with 100% of the rated torque. The switching frequency and sampling time are the same as those in the simulation.

Fig. 9 illustrates the performance of the MC drive without unbalance compensation. The input current waveform is distorted because of the voltage unbalance. Fig. 10 shows the performance of the MC drive with the proposed unbalance compensation. As the figure illustrates, input current waveform is improved compared with Fig. 9, and it is in phase with input phase voltage (i.e., unity power factor condition). However, the capacity of the control technique is limited. As Fig. 2(c) illustrates, the input currents are formed from the segments of the output currents. The MC input current pulses are filtered by the input capacitive filter and the lower frequency components (the average value) of these currents flow to the utility grid. With the load current magnitude and switch on time values being limited, it cannot be guaranteed that the currents follow the reference signal of (22). Therefore, high-order harmonic distortion could not be completely eliminated, but it has been reduced significantly compared to Fig. 9 while keeping good output current control characteristics.

In Fig. 11 the input current harmonic spectrum of the proposed method is compared with that of the uncompensated method. As the spectrum indicates, the third-order harmonic component is very large in the uncompensated system, and it implies that a 2ω frequency reactive power ripple exists in the system. Employing the proposed unbalance compensation technique, the third-order harmonic component is reduced from 9.1% to 0.4%. The input current total harmonic distortion (THD) of the proposed method is 5.7% while THD of the uncompensated method is 11.7%. The output current in both cases is sinusoidal and the output performance of the drive is satisfactory. Therefore, it can be concluded that the proposed technique improves the input power quality of the MC drive without output performance degradation.

IV. Grid Voltage Failure

Voltage sag—A momentary decrease in the grid voltage magnitude lasting between half cycle and several seconds—is the main cause of industrial system failures resulting in significant repair cost and process capacity loss. In this section, the behavior of the MC drive during and after a brief voltage sag condition is investigated. As the extreme case, the total grid voltage loss is considered.

Unlike the PWM-VSI drive, the MC drive has no dc link capacitor, and it has no capacitor charging time delay before operation. Thus, following a voltage sag condition, the MC drive can restart significantly faster. The MC drive is connected to a 200 V, 7.5 kW induction motor and operated in the vector control mode. The motor is operating at 1500 r/min and with 50% of rated torque.

In Fig. 12, the rapid restarting capability of the MC drive is demonstrated. In Fig. 12(a), a short voltage sag condition with

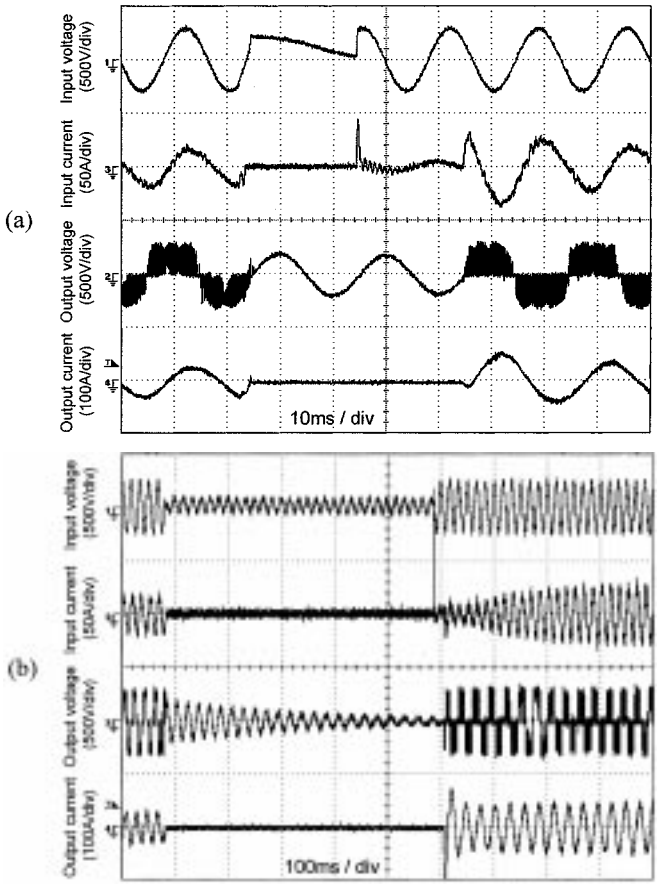


Fig. 12. MC drive performance during utility grid failure followed by restoration. (a) 20 ms power interruption. (b) 500 ms power interruption. Traces from the bottom to the top: output phase current and line voltage, input phase current and line voltage.

20 ms duration is tested. From the time that the line voltage is restored to the time that the MC drive becomes fully operational, approximately 20 ms elapsed. This time interval is required for input voltage synchronization. In Fig. 12(b), the grid voltage is interrupted for 500 ms. During this interruption, the power delivered to the load is also interrupted, as a consequence of the fact that the MC drive is an energy storage-less device. However, for the same reason, following the line voltage restoration, the MC drive rapidly resumes operation and delivers full power in 20 ms. The restarting time of the MC drive is substantially shorter than that of inverter drives which have dc link capacitors with charging time intervals in the order of several hundred milliseconds.

V. Conclusions

The matrix converter drive performance under abnormal input line voltage conditions has been investigated. An input voltage unbalance compensation technique that improves the input current waveform quality without output performance degradation has been developed and its feasibility demonstrated via detailed computer simulations and experimental results. The power line loss and recovery behavior of the drive has been experimentally investigated. Rapid restarting capability of the drive has been demonstrated. As a result, over a wide operating range and under abnormal input conditions, high performance could be obtained both at the input and output of the drive. Therefore, the feasibility of the matrix converter drive as a future generation drive with high input power quality has been proven.

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