A Modified C-Dump Converter for Variable-Reluctance Machines

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Abstract—**This paper describes a new type of converter for variable-reluctance machine (VRM) drives. In this converter topology, the energy extracted from an offgoing phase is stored in a dump capacitor. The energy stored is consequently used to either quickly turn on the next ongoing phase or energize the conducting phase frequently during the conduction interval instead of being returned to the supply as for a conventional *C*-dump circuit. Since the additional switch used to pass the energy to the *C*-dump capacitor is switched under a relatively low-voltage condition and its switching frequency is relatively low, the rating of the additional switch is modest. The major advantage of this converter is that it uses a low-switching device / phase ratio while achieving better performance characteristics than the other topologies.**

I. Introduction

ALTHOUGH VR machines only recently have been studied in depth, their operating principle has been well known as early as conventional induction and synchronous machines. The operating principle of these machines is such that the phase inductance is designed to vary almost linearly with the rotor angle. To develop torque, carefully programmed current pulses are sequentially injected to the phases during the varying inductance interval. Hence, it is necessary to extract accurate rotor position information for successful operation. Regardless of the phase current flow direction, motoring torque is produced during the increasing inductance interval and generating torque during the decreasing inductance interval. Assuming that mutual coupling between the phases does not exist and that the phase inductance is linear, the developed torque in the nth phase is given by

$$T_{en} = \frac{1}{2} i_n^2 \frac{dL_n}{d\theta_{re}} \tag{1}$$

where L_n is the inductance of the nth phase, and i_n is the current of the nth phase, and θ_{re} is the electrical rotor angle. The total torque is then equal to the sum of the n contributions from the n phases

$$T_e = \sum_1^n T_{en}. \tag{2}$$

The freedom in choosing the current flow direction makes it possible to use a unipolar converter to drive the VRM, thereby reducing the converter cost because of the reduced switch requirement and improving the reliability of the drive because of the inherent shoot-through fault immunity.

The most conventional VRM, (the switched reluctance machine (SRM) shown in Fig. 1) has a doubly salient laminated structure that is very simple and robust. The rotor does not have any windings or conductors. As the rotor spins, the inductance of the phase windings of a machine varies between the minimum inductance (unalignment) and maximum inductance (alignment) with respect to the rotor angle as shown in Fig. 2(a). Due to the highly nonlinear magnetic behavior of the machine, the phase inductance is dependent on the current level as well as the rotor position. There is also a speed-dependent back emf that becomes very large at and above the base speed and dominates the behavior of the drive. Although the machine has a simple structure, the behavior of its electromagnetic is obviously nontrivial. However, the linear inductance SRM model along with back emf proportional to the machine speed is very helpful in exploring the behavior of this type of drive.

For the low-speed operating mode, the back emf can be ignored, compared with the dc bus voltage, and the machine can be assumed as current fed. Current-fed operation is obtained by means of a current-regulated PWM technique. With a proper converter and controller, the phase current waveform should be programmed to be close to a square waveform in order to minimize torque pulsations (see Fig. 2(b)). For medium-speed range, the back emf increases and limits the rapid current buildup. To compensate for this loss, the ongoing phase is excited in advance as shown in Fig. 2(c). As the machine runs at speeds close to and above the base speed, the back emf becomes comparable with and even larger than the supply voltage that the phase current buildup becomes impossible without very large advance angle techniques. As shown in Fig. 2(d), the phase winding must now be excited well in advance, whereas its inductance is small in order to buildup sufficient current for a commanded torque. In this mode, the phase winding is voltage fed, and hence, this technique is called the pulse dropping mode. It is

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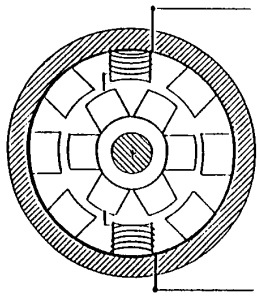

Fig. 1. Idealized representation of eight-pole stator six-pole rotor switched reluctance motor.

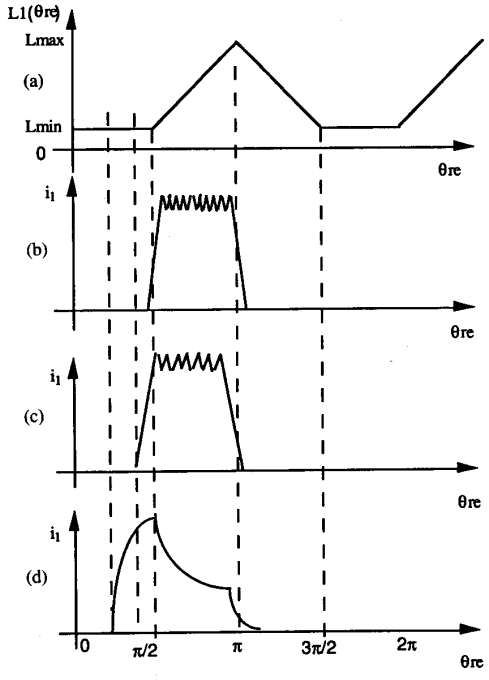

Fig. 2. (a) Linear phase inductance waveform of a four-phase VRM; (b) typical phase current waveform at low speed; (c) typical phase current waveform at medium speed; (d) typical phase current waveform at high speed.

clear that any suitable power electronic converter and controller for this type of drive system must maintain the capability to program the current pulses for the VRM accurately.

II. An Overview of VRM Converter Topologies

The cost and performance of the VRM drive are highly dependent on the converter topology used to drive the VRM. Ever since the promising features of the VRM drives have been realized, developments in the converter topologies have proceeded in parallel with the machine design. Since that time, there have been many converter topologies invented, and unlike the conventional inverter driven induction machine drive, the VRM drives have not been standardized as yet. In addition, in contrast with induction motor drives (which almost always employ a PWM voltage link inverter), the optimum converter concept for VRM drives appears to be much more application dependent.

Ideally, the VRM converter must meet the following requirements: 1) capability to program a commanded current pulse very quickly and accurately for good drive performance, 2) as low a converter power VA rating as possible for a given drive rating for low cost, 3) reliability and robustness, 4) low switch/phase ratio, 5) high efficiency, and 6) low noise and torque pulsation. Only if all of these conditions are met can VRM drives become comparable with the conventional inverter-driven induction machine drive and other variable-speed drives that are available.

Numerous converter topologies invented to date have become popular and used in a variety of applications. These configurations include the asymmetric bridge converter, bifilar winding configuration, split supply configuration, *H*-bridge configuration, common switch configuration, and *C*-dump converter, all of which are shown in Fig. 3.

The asymmetric bridge converter has full current pulse programming capability, that is, the converter is capable of applying the full supply voltage V_s across the winding in either polarity for the purpose turning the current in each phase both on and off. However, the converter suffers from high switch/phase ratio and, therefore, is expensive because the two switches per phase and the associated drive circuitry add to the expense of the drive.

The bifilar winding configuration meets the minimum switch requirement with one switch/phase ratio; however, the voltage spikes resulting from imperfect magnetic coupling increase the switch voltage ratings to $2V_s$ and even higher. In addition, the copper losses associated with the auxiliary windings are unacceptably high for many applications.

The split supply converter topology also meets the minimum switch requirement. However, in this case, the phase number must be even, and the converter does not tolerate a phase unbalance or fault in any phase because any such fault results in voltage buildup in the capacitor banks. In addition, the dc bus voltage utilization is poor because only $1/2V_s$ is utilized.

The H-bridge topology meets the minimum switch requirement. However, it is suitable for four or multiples of four-phase machines, and it also utilizes only half the dc supply voltage. In this topology, two phases are always on at a time, whereas only one of the two phases are contributing to motoring torque production at any instant. Therefore, the degradation of the output torque is obvious.

The common switch configuration only requires one more switch in addition to the minimum switch requirement. However, it does not tolerate phase overlapping, and therefore, its capability is very limited, particularly for the single-pulse mode.

The *C*-dump configuration [1] also requires only one

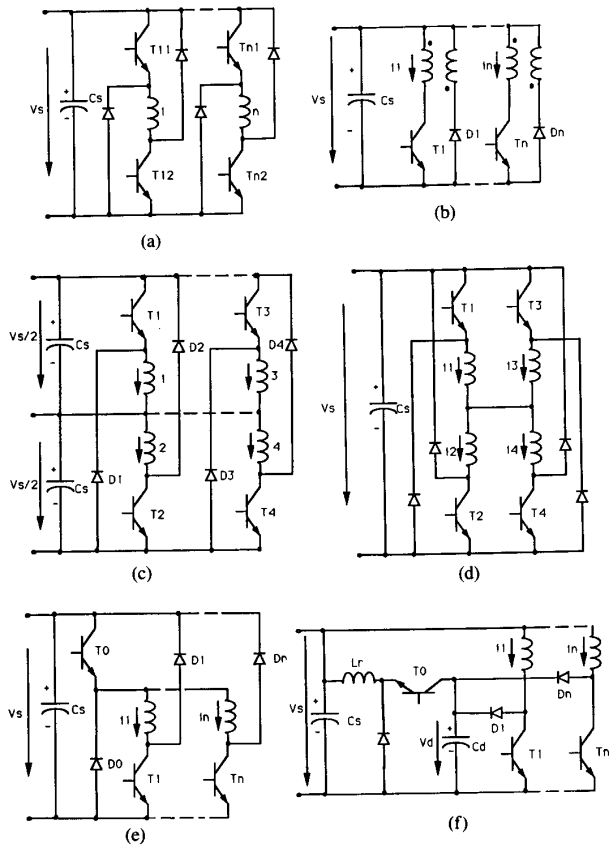

Fig. 3. Popular VRM converter topologies: (a) Asymmetric bridge converter; (b) bifilar winding configuration; (c) split supply converter; (d) *H*-bridge converter; (e) common switch converter; (f) *C*-dump converter.

additional switch to the one switch/phase requirement. The converter utilizes a capacitor to dump the energy of an offgoing phase and a chopper operating with buck principle to discharge the capacitor. The capacitor voltage is generally maintained at $2V_s$ in order to supply $-V_s$ to the offgoing phase. The converter also has full capability to program the current pulse during both turn on and turn off, and high efficiency operation results. The drawbacks of this converter are the high switching device voltage ratings, the expense of the additional switch, the dump capacitor and inductor, and the losses associated with the reactive elements.

To open new application fields to the VRM drives, it is clearly necessary to both improve the drive performance and lower the cost. These goals can be achieved either by improvements in the machine design or innovations in the converter configuration. The ultimate answer in converter design may be a resonant-type converter configuration or modifications to the well-known topologies as well. This paper deals with one such example, that is, a suggested improvement in the *C*-dump configuration.

III. The Modified *C*-Dump Converter

The new converter topology shown in Fig. 4 is derived from the *C*-dump converter topology by eliminating the inductor of the buck converter. The energy is again dumped into the capacitor but is directly utilized by the next phase rather than being returned to the dc supply as in the conventional *C*-dump configuration. Since the *C*-dump capacitor voltage is in the range of $2V_s$, its proper utilization significantly improves the drive performance. Specifically, with a higher voltage, less time is needed to build up the current in the ongoing phase, particularly over the high-speed range, where an advance angle firing of the switches is necessary. Reduction in the advance angle will clearly also improve the drive efficiency since less current is required to flow during the interval when the phase is not producing torque.

It can be noted that the converter is also capable of freewheeling, which improves the power rating of the rectifier side and allows for a flat-topped current waveform to be programmed. However, this mode of operation is dependent on whether or not the capacitor voltage is above the reference value. Therefore, it is necessary that complex control mechanisms be used to realize this benefit.

The capability of the converter to turn off an offgoing phase is the same as the conventional *C*-dump converter, that is, reverse biasing the offgoing phase with V_s voltage for fast current decay. Therefore, this modified *C*-dump converter topology also possesses full capability to program a commanded current pulse.

It can be noted from Fig. 4 that the main switches in this topology have a $2V_s$ rating as in the conventional *C*-dump converter. The additional switch operates at much lower frequencies than the main switches and performs capacitive switching. Therefore, it has a much lower rating and lower losses. There is a tradeoff between the switching frequency of this switch, the capacitor size, and voltage hysteresis band of the capacitor. Although the capability of the converter is as good as the *C*-dump converter, this converter has higher efficiency and costs less.

The conditioning diode *D*0 of the converter avoids the energy reversal from the dump capacitor back to the supply. However, the voltage drop across this diode may be a major drawback for very low-voltage applications such as automotive applications that utilize the 12-V battery supply.

In addition, in the single-pulse mode at high speed, where the current cannot reach the desired value due to the motor back emf, current buildup even with $2V_s$ is not always possible because there is not sufficient energy dumped into the capacitor. Hence, only once in every few pulses can current buildup with $2V_s$ be achieved.

The dump capacitor voltage regulation, advance angle calculation, and all these control matters make the system complex; however, the availability of the low-cost microprocessors solve this problem to a great extent.

IV. Simulations and Test Results

In this section, the simulation of a linear inductance SRM model along with the modified *C*-dump converter topology is studied. Although the linear model is not

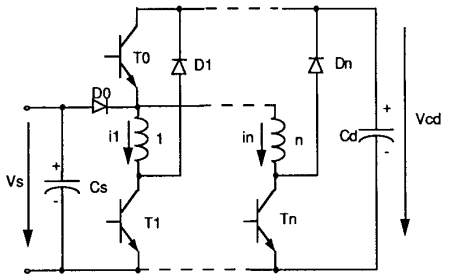

Fig. 4. Modified *C*-dump converter.

sufficient for accurate torque prediction, it is sufficiently accurate to estimate the converter capability. The simulations were made for an idealized version of a four-phase Oulton SRM. The dc bus voltage is assumed to be 400 V, the dump capacitor size is assumed to be 1.5 mF, and the machine base speed is 1500 r/min. The drive was simulated for 0.1 and 0.66 Wb as well as Wb cases where Wb is the base speed. The simulation results are shown in Figs. 5–7.

For the low-speed range, the converter operates in a current chopping mode. The current waveform is very close to a square wave. The current buildup and decay are very rapid, which is similar to the conventional *C*-dump converter.

For the medium-speed range, turn on of the phases in advance is necessary to compensate for the back emf. However, it is possible to speed up the turn on by turning on *T*0, allowing the dump capacitor voltage to appear across the motor phases. The fast current decay allows for improvement in the turn-off angle and therefore improves the conduction interval. As shown in Fig. 6, at the instants that the capacitor voltage is sufficiently high, the phase current waveform is more flat topped than at the other instants. As a result, the drive produces a higher torque than for the equivalent *C*-dump converter.

At base speed and above, the back emf dominates the system behavior, and the drive goes to the so-called single pulse mode. In this mode, the phases are turned on well in advance to buildup the necessary current. Unfortunately, it is not always possible to build up the phase current with a value of $2V_s$ because the dumped energy to the capacitor is not sufficient to serve this purpose. However, this is possible at least once every few cycles. The only requirement is to program the processor to count for the capacitor voltage level when calculating the advance angle. Although substantial torque improvement is not possible in this mode, an efficiency enhancement can still be realized.

To confirm the simulation results, a modified *C*-dump-type converter that utilizes power BJT's as switches was built for a 10-hp, 8/6-pole Oulton drive SRM. The controller of the drive was Motorola DSP56000 digital signal processor based. The drive was tested at no load for both 400 and 750 r/min. To vary the speed, the dc bus voltage level was adjusted, and the phase current reference value

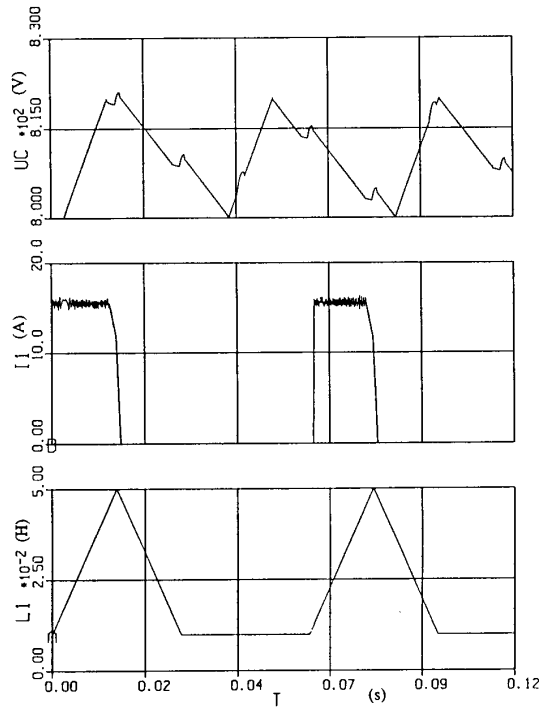

Fig. 5. Modified *C*-dump converter simulation for low speed operation.

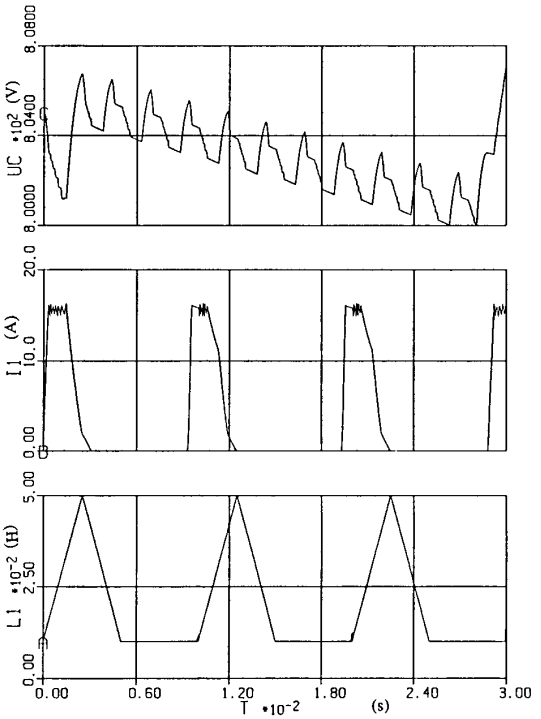

Fig. 6. Simulation of VRM drive operation with modified *C*-dump converter operation at medium speed.

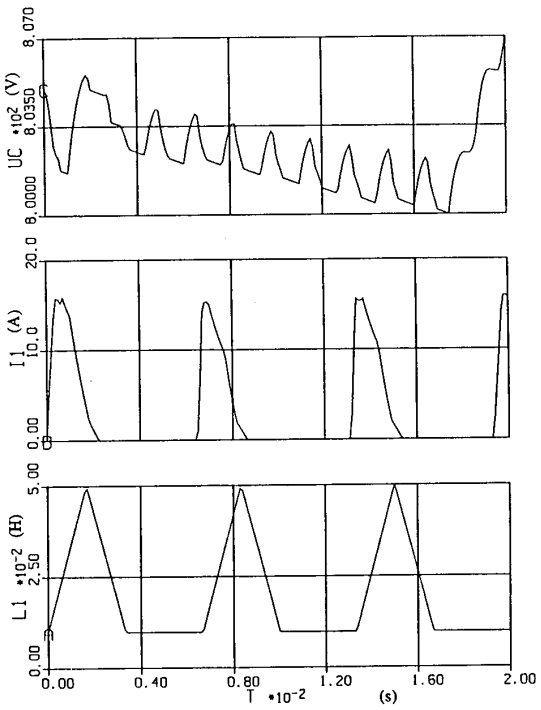

Fig. 7. Computer simulations for base speed operating mode.

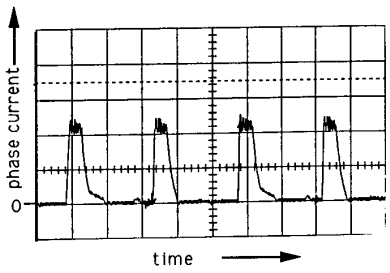

Fig. 8. Experiment phase current waveform at low-speed operation: 400 r/min, 2 A/div, 10 ms/div, V_s = 50 V, V_{cd} = 100 V.

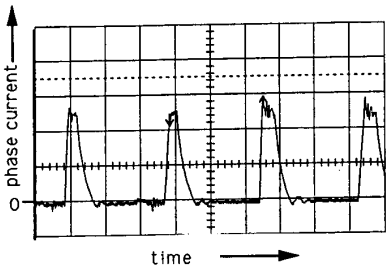

Fig. 9. Experimental phase current waveform at medium-speed operation: 750 r/min, 2 A/div, 5 ms/div, V_s = 60 V, V_{cd} = 120 V.

was held at 5 A in both cases. During both tests, the *C*-dump capacitor voltage was twice the dc bus voltage. The phase current waveform shown in Fig. 8 confirms the fast current build-up and commutation capability of the converter at 400 r/min (i.e., low speed). The phase current builds up with $2V_s$ and turns off with reverse applied V_s. At 750 r/min (i.e., medium speed), as shown in Fig. 9, both the current buildup and current commutation are relatively slower than the previous case due to the shorter time interval available and the increasing back emf. The test and simulation results agree well in both cases. The losses of the converter are primarily the switching losses due to the high switching frequency that is limited to 5 kHz by the controller. At base speed and above, the drive is expected to lose some of its current build-up and current commutation capability due to the increasing back emf and shorter time interval available.

V. Conclusions

This paper has presented a new type of converter for VRM drives, which introduces modifications to the conventional *C*-dump converter configuration. The modified *C*-dump configuration has full current pulse programming capability and better efficiency as well as lower cost. Except for high speed, current buildup in each phase is achieved by applying $2V_s$ as opposed to the usual V_s or $V_s/2$ that is common with other types of converters. Current turnoff is always forced with the full negative dc link voltage $-V_s$. The only losses of this converter are the switching losses, and therefore, the converter is highly efficient. This configuration is well suited to microprocessor-based high-performance VRM drive applications.

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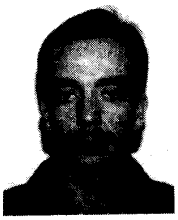

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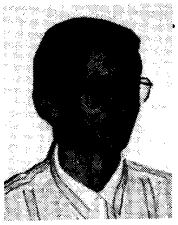

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Dr. Lipo has maintained a deep research interest in power electronics and ac drives for over 25 years. He has received 11 patents and has 13 IEEE prize paper awards for his work, including co-recipient of the Best Paper Award in the IEEE Industry Applications Society Transactions for 1984. In 1986, he received the Outstanding Achievement Award from the IEEE Industry Applications Society for his contributions to the field of ac drives, and in 1990, he received the William E. Newell Award of the IEEE Power Electronics Society for contributions to field of power electronics.